Tunneling mechanism in a (Ga,Mn)As/GaAs-based spin Esaki diode investigated by bias-dependent shot noise measurements

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Electron transport across a tunneling barrier is governed by intricate and diverse causes such as interface conditions, material properties, and device geometries. Here, by measuring the shot noise, we investigate electron transport in a (Ga,Mn)As/GaAs-based spin Esaki diode junction over a wide range of bias voltage. The asymmetric electronic band profile across the junction allows us to tune the types of tunneling process. By changing the bias voltage in a single device, we successively address the conventional direct tunneling, the excess current conduction through the mid-gap localized states, and the thermal excitation current conduction. These observations lead to a proper comparison of the bias dependent Fano factors. While the Fano factor is unity for the direct tunneling, it is pronouncedly reduced in the excess current region. Thus, we have succeeded in evaluating several types of conduction process with the Fano factor in a single junction.

I. INTRODUCTION

Shot noise is a useful probe for investigating transport phenomena of mesoscopic devices [1]. It is caused by the electron partition process under a finite bias condition, where the current spectral density can be described as $S_I = 2eIF$. Here, e is the elementary charge, I is the time-averaged current, and F is a dimensionless quantity called the Fano factor. It shows a universal value in some ideal situations: $F = 1/3$ for a diffusive mesoscopic conductor [2], $F = 1/2$ for a dirty interface [3], and $F = 1/4$ for a chaotic cavity [4]. In a classical tunnel barrier, the tunneling is well described by a Poissonian process with $F = 1$ [5–7]. The actual Fano factor, however, often deviates from 1 in the presence of the excess current through localized states (LSs). It is, therefore, of fundamental significance as well as of technical interest to systematically understand the Fano factors in electron transport.

In thin tunneling barriers with LSs, a resonant tunneling is dominant at low temperature where electrons adiabatically transport via a single localized state [8]. A theoretical work predicted a universal case $F = 3/4$ when LSs are randomly distributed around the center of a tunnel barrier [9]. As this ideal situation is not easy to achieve experimentally, F usually ranges from 1/2 to 1 depending on the symmetry of the coupling to both leads and the Coulomb interaction [9–16]. In addition, $F > 1$ was reported for the case of strong Coulomb interaction [17,18], and $F < 1/2$ s observed in the presence of leaky barriers [19,20]. When the tunnel barrier is thick, multiple hopping through the LS network becomes dominant [21]. In this case, F decreases from unity, depending on the number of hopping events (N), the network structure, and dimensionality [22–28]. In a simple one-dimensional network with N identical barriers, theory gives $F = 1/N$ [22]. Thus, tunneling is strongly affected by the material properties, the number of LSs, their spatial distributions, and device geometries.

The Esaki diode [29] is an ideal system for investigating such transport phenomena in a single device. This is because the type of tunneling process can be systematically tuned by changing the bias voltage in a single device: direct tunneling occurs at nearly zero or negative bias, a negative differential resistance is realized at a finite positive bias, and a thermal excitation current develops at large positive bias. In addition, actual devices are affected by the excess current flow through LSs formed by doping or defects [30]. In the case of a (Ga,Mn)As/GaAs-based spin Esaki diode, it has been well studied that the LSs affect the tunneling process [31–40]. A theoretical work where the exchange energy of (Ga,Mn)As and the impurity band are taken into account successfully reproduced the *I-V* characteristics of the spin Esaki diode [41].

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This motivates us to think that investigating shot noise in a (Ga,Mn)As/GaAs-based spin Esaki diode provides considerable insight into the mechanism of electron transport through LSs and the spin transport in the spin Esaki diode [42,43].

In this article, we report shot noise properties of (Ga,Mn)As/GaAs-based spin Esaki diode junctions. To investigate the electron transport mechanisms in detail, we measured the shot noise over a wide bias voltage range. We found that the Fano factor shows unity ($F = 1$) around zero-bias (direct tunneling) and at large positive bias (thermal diffusion), while it is reduced ($0.87 < F < 1$) for bias values in the region of negative differential resistance and at large negative bias. We argue that the observed noise reduction originates from the excess current via LSs in the tunnel barrier. We also measured the shot noise in a series circuit of two adjacent junctions to verify the influence of the spin accumulation in the GaAs. As a result, we determined that the influence of the spin accumulation on the shot noise was negligibly small in this configuration and the obtained results were well explained based on the measured shot noise in the single junction.

This paper is organized as follows: In Sec. II A, sample fabrication and a typical *I-V* characteristic of our sample are provided. In Sec. II B, the measurement setup and the analysis method are described in detail. Section III is devoted to the experimental results and discussion. In Sec. III A, we focus on the results of a single spin Esaki diode junction. The bias voltage dependence of the Fano factor and its origins are discussed. In Sec. III B, we show the results of two junctions connected in series. The consistency with the single junction case is discussed. In Sec. IV, we conclude our study.

II. EXPERIMENTS

A. Sample and *I-V* characteristic

Our device has a lateral spin valve structure [44–47], consisting of the *p*-type (Ga,Mn)As ferromagnetic electrode and *n*-GaAs channel, which form a spin Esaki diode as shown in Fig. 1(a). Such a spin valve structure is important not only for the realization of all-semiconductor spin current devices, but also from the viewpoint of fundamental physics exploring spin injection into a two-dimensional electron system [35–37], control of nuclear spins [38,39], and shot noise associated with spin accumulation [40]. In this study, we focus on transport properties of the spin Esaki diode junction itself.

The detail of the sample fabrication is as follows. The epitaxial multilayer stack has been grown on a (001) GaAs substrate by a molecular beam epitaxy. It consists of a GaAs buffer, an AlGaAs/GaAs superlattice, a 1 μm *n*-GaAs channel, a 15-nm GaAs with linearly graded doping $n \to n^+$ ($n = 2 \times 10^{16}$cm^{-3} and $n^+ = 5 \times 10^{18}$cm^{-3}), an 8 nm n^+- GaAs, a 2.2 nm low-temperature (LT)-grown AlGaAs, and a 50-nm LT-grown (Ga$_{0.945}$Mn$_{0.055}$)As. As shown in the right panel of Fig. 1(a), due to the large difference in concentration of dopants, the depletion layer forms almost entirely on the GaAs side. The dopants and defects caused by the LT growth are considered to form LSs.

The wafer was patterned into 50-μm wide mesas along the [110] direction by standard photolithography and wet
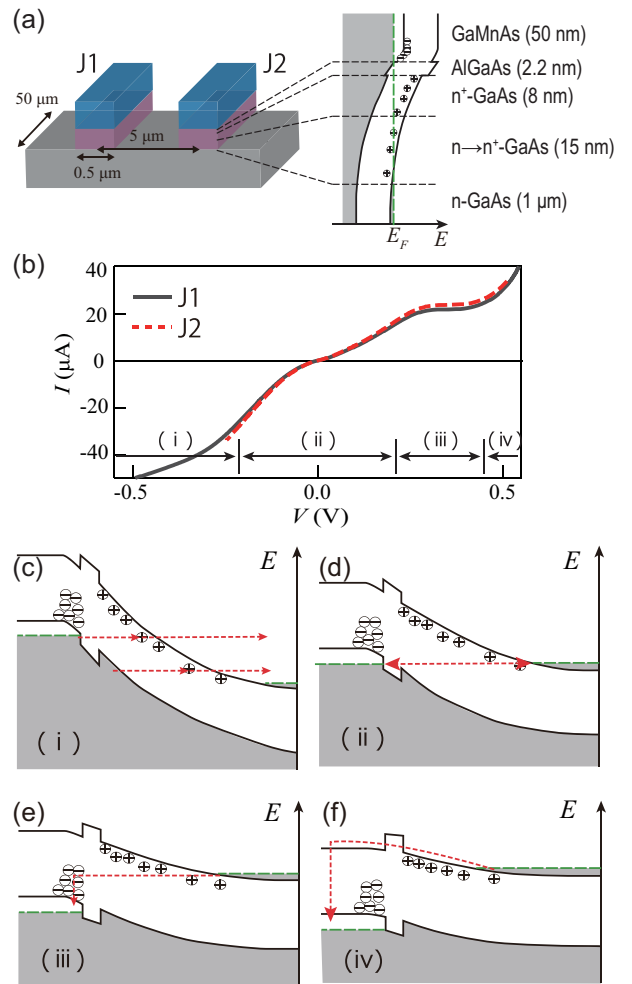

FIG. 1. (a) Schematic illustration of our lateral spin valve devices with two spin Esaki junctions (J1 and J2). Right panel shows the band diagram of the (Ga,Mn)As/GaAs epitaxial multilayer stacks and energy of electrons. In the electron band diagram, the vertical dashed green line represents the Fermi energy. (b) Current-voltage (*I-V*) characteristics of each spin Esaki diode junctions. (c)–(f) Energy diagrams for several bias voltage conditions; the red dashed arrows sketch typical transport mechanisms, where (c), (d), (e), and (f) correspond to the bias regimes (i), (ii), (iii), and (iv) in (b), respectively.

chemical etching. Then the ferromagnetic (Ga,Mn)As electrodes with a width of 0.5 μm were formed by electron beam lithography and reactive ion etching, where the etching process was stopped above the *n*-GaAs channel layer. In this study, we used two junctions located in the center of the mesa, namely Junction 1 ("J1") and Junction 2 ("J2"), with a size of 0.5 μm×50 μm and a center-to-center distance of 5 μm, as shown in the left panel of Fig. 1(a). Additionally, we used two large Esaki diode junctions of a size 150 μm×150 μm placed at the edges of the mesa, as reference contacts for electrical measurements [see Fig. 2]. Note that the top (Ga,Mn)As is a heavily doped *p*-type conductor, the interface between the Au/Ti electrode and (Ga,Mn)As forms an ohmic junction.

All the measurements were performed at a low temperature (1.6 K) to reduce thermal noise, using a variable temperature
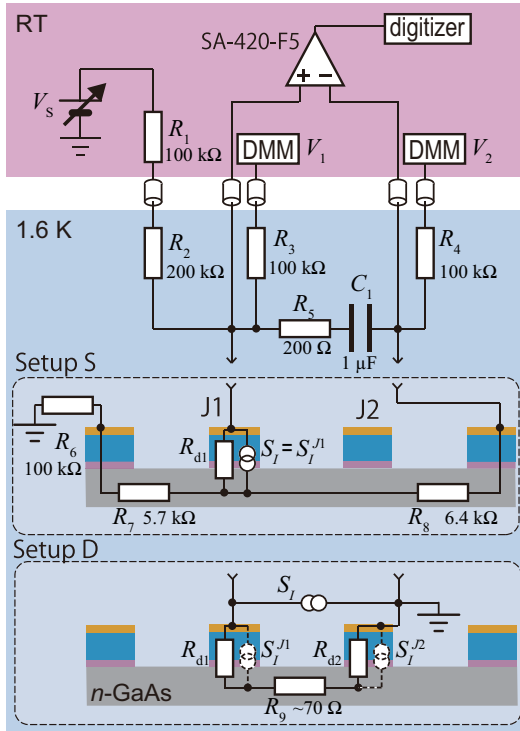
FIG. 2. Schematics of the noise measurement setups including the equivalent circuit of the sample (see text for detail). By using a homemade sample holder, the low-temperature resistors and a capacitor are placed very close to the sample.

insert (Oxford Instrument plc.) equipped with a superconducting magnet. Although an external magnetic field was applied parallel to the long axis of the ferromagnetic electrodes to saturate their magnetization along this direction, it was set to zero before the actual measurement was performed. Figure 1(b) shows the I-V characteristics of the J1 and J2 measured at 1.6 K using three-terminal configuration as explained in Sec. II B. These two curves are almost identical. The nonlinear behavior, typical to the Esaki diode, is clearly pronounced. It consists of the following four regions (i, ii, iii, and iv) as shown in Figs. 1(c), 1(d), 1(e), and 1(f), respectively. At the large negative bias region (i), nonlinearity appears due to the expansion of the depletion layer [Fig. 1(c)]. In region (ii) the direct tunneling between the valence band of (Ga,Mn)As and the conduction band of n-GaAs [Fig. 1(d)] dominates. The region (iii) is a so-called negative differential resistance region where the direct tunneling is forbidden [Fig. 1(e)]. However, a clear dip, constituting a truly "negative" resistance, expected for an ideal Esaki diode, is not seen in the present spin Esaki diode. This is due to the excess current through LSs as discussed below. Finally, (iv) is a region where the thermal excitation current across the built-in potential, as in conventional p-n junctions becomes dominant, resulting in a rapid increase of the current [Fig. 1(f)].

B. Noise measurement

The equivalent circuit of our noise measurement system is shown in Fig. 2. In this study, electrical measurements were performed in two different experimental setups: single

junction (Setup S) and two junctions connected in series (Setup D) as shown in the bottom panel of Fig. 2. The "sample" indicates J1 (R_{d1}) alone in Setup S, and the series circuit of J1 and J2 ($R_{d1} + R_9 + R_{d2}$) in Setup D, where R_{d1} and R_{d2} are the differential resistance of the J1 and J2, respectively. Here we first describe the common parts. A dc bias current (I) is fed to the sample by using a programmable dc voltage source with the output voltage V_S and two resistors ($R_1 = 100$ kΩ at RT and $R_2 = 200$ kΩ at 1.6 K). The voltages (V_1 and V_2) across the sample were monitored by two digital multimeters, respectively. Here, I is deduced by $I = (V_S - V_1)/(R_1 + R_2)$ and the bias voltage (V) across the sample is given by $V = V_1 - V_2$. Note that the reference voltages (V_2) are measured at the right edge of the channel in Setup S and the contact on J2 in Setup D, respectively. We also measured the differential resistance at a given bias by modulating I and measuring V in response.

The time domain voltage fluctuation signal was measured by a digitizer (National Instruments PCI-5922) after amplification with a low-noise amplifier (NF Corporation SA-420F5). Then, the voltage spectral density S_V was obtained by fast Fourier transformation (FFT). The resistances and the capacitance of the coaxial cables ($\sim$300 pF in total) work as a low-pass filter. To increase the cutoff frequency, we use $R_5 = 200$ Ω and $C_1 = 1$ μF at 1.6 K in parallel with the sample. Moreover, R_2, $R_3 = 100$ kΩ and $R_4 = 100$ kΩ are placed just near the sample to cut the capacitance of the coaxial cables that are connected to the RT measurement system. Here, since R_5 is small compared to other resistances, it dominates the conversion from the current spectral density of the sample S_I to S_V. Thus, $S_V \approx G^2 R_5{}^2 S_I$ where G is the gain of the amplifier. The frequency independent component of S_V was estimated by fitting the spectrum taking the low-pass cutoff into account in the frequency range between 1.4 and 5 MHz.

In Setup S, S_I is equal to the current noise generated by J1 ($S_I = S_I^{J1}$). However, S_V contains not only S_I but also the thermal noise from the constant resistors ($S_I^{R_5} = 4k_B T/R_5$ and $S_I^{R_8} = 4k_B T/R_8$), and other external current noise and voltage noise contributions (S_I^{offset} and S_V^{offset}) mainly due to the amplifier. The relation between S_V and S_I is given by

$$S_V = G^2 \Bigg[\left(\frac{R_{d1} R_5}{R_{d1} + R_5 + R_8} \right)^2 S_I + \left(\frac{(R_{d1} + R_8) R_5}{R_{d1} + R_5 + R_8} \right)^2$$

$$\times \left(S_I^{R_5} + S_I^{\text{offset}} \right) + \left(\frac{R_5 R_8}{R_{d1} + R_5 + R_8} \right)^2 S_I^{R_8} + S_V^{\text{offset}} \Bigg].$$
$$(1)$$

Since R_{d1} varies depending on the bias voltage, two unknown variables (S_I^{offset} and S_V^{offset}) are carefully calibrated. R_7 and R_8 are the sums of the junction resistance of the reference contact at the left and the right edge of the mesa and the longitudinal resistance of the $\sim$300-μm-long channel between the corresponding reference contact and J1, respectively. The large size of the reference contact, however, makes its resistance negligible compared to the channel resistance. Note that, without $R_6 = 100$ kΩ, the noise signal S_I leaks to the ground side, resulting in a slight deviation from Eq. (1).
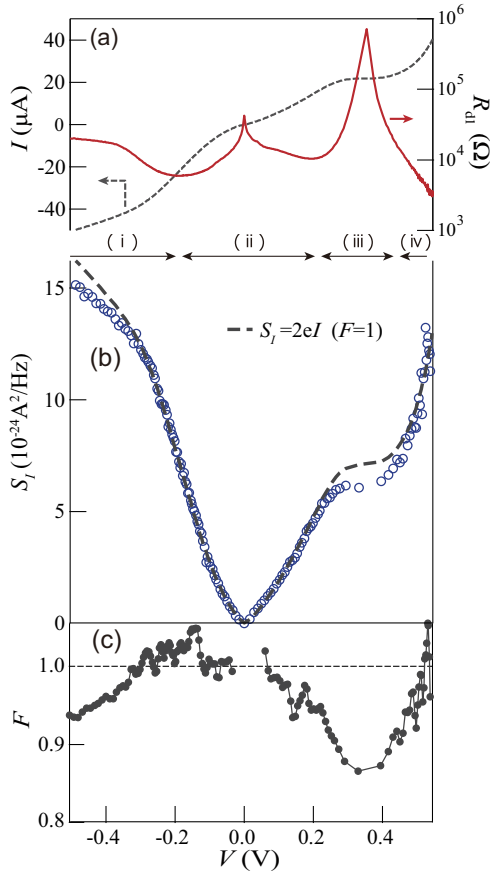
FIG. 3. (a) I and R_{d1} of junction J1 as a function of bias voltage. (b) Measured S_I in Setup S and calculated full-shot noise ($2eI$). (c) Estimated $F(\equiv S_I/2eI)$ by using the data in (b).

In the case of Setup D, S_I is generated by the series circuit of J1, J2, and n-GaAs channel ($R_{d1} + R_{d2} + R_9 \equiv R_d$). The relation between S_V and S_I of the series circuit is then expressed as

$$S_V = G^2 \left[\left(\frac{R_d R_5}{R_d + R_5} \right)^2 \left(S_I + S_I^{R_5} + S_I^{\text{offset}} \right) + S_V^{\text{offset}} \right]. \quad (2)$$

In the absence of spin accumulation in the n-GaAs channel, one can express S_I of the series circuit based on the shot noise generated by each single junction. By using $R_{d1} + R_{d2} \gg R_9$ and defining the current noise generated by J2 as S_I^{J2}, S_I is expressed as

$$S_I = \frac{R_{d1}{}^2 S_I^{J1} + R_{d2}{}^2 S_I^{J2}}{(R_{d1} + R_{d2})^2}. \quad (3)$$

III. RESULTS AND DISCUSSION

A. Single junction (Setup S)

Figure 3(a) shows the bias voltage ($V = V_1 - V_2$) dependence of I and R_{d1} [the dotted curve is the same as shown in Fig. 2(b)]. Applying a positive bias voltage, R_{d1} gradually decreases, except for a peak in region (iii). This peak reflects the negative differential resistance and reaches its maximum around $V \sim 0.35V$. For a negative bias, R_{d1} first similarly decreases, and then increases in regions (i). As mentioned

above, full-shot noise ($F = 1$) is expected for the Poissonian process in a conventional tunnel barrier. To see the difference from this value, the obtained S_I through Eq. (1) and calculated $S_I = 2eI$ under the assumption that $F = 1$ are plotted in Fig. 3(b). In regions (ii) and (iv), the measured shot noise is in good agreement with the calculated curve, while reductions in S_I are observed in regions (i) and (iii). To see these reductions more clearly, the bias voltage dependence of the estimated $F(\equiv S_I/2eI)$ is shown in Fig. 3(c). In the region (ii), F is very close to unity, although the data points are scattered. On the other hand, in the region (iii), F has a broad dip structure with a local minimum $F = 0.87$ at $V \sim 0.35V$, which is in accord with the peak in R_{d1}.

Let us focus on the transport properties in the region (ii). Since the direct tunnel process [see Fig. 1(d)] is supposed to be dominant in this region, our result ($F \sim 1$) is not surprising. The experiments on germanium Esaki diodes [48,49] reported full-shot noise in this region. However, it is important to confirm the full-shot noise in the spin Esaki diode junction to evaluate the device quality. In fact, many types of deviation mechanisms from the full-shot noise limit have been studied both theoretically [1,9,10,16,22,24,43] and experimentally [7,11–14,17–19,23,25–27,50,51]. Our result of $F \sim 1$ indicates that the junction conductance in this bias region is purely governed by direct tunneling without leaking process such as sequential tunneling via defects.

In the previous paper [40], instead of $F = 1.0$, we reported $F = 0.78 \pm 0.04$ in the region (ii) using the same device. This difference in Fano factor is due to the measurement circuit, namely, the leakage of the noise signal through the ground loop was not well treated in the previous work [40]. This effect results in a systematic deviation in the noise signal, leading to the reported Fano factor less than 1. The important aspect here is the relative relationship between the resistance of the undesired parallel path via ground and the resistance of the signal line. In the present work, to prevent the leakage effect, we have inserted a large resistance R_6 and choose a smaller resistance for R_5, as shown in Fig. 2. R_6 increases the resistance of the parallel path, while the smaller R_5 decreases the resistance of the signal line. The proper combination of the used resistances has perfectly eliminated the artifact, enabling us to observe $F \sim 1.0$ as expected. Note that the difference in the absolute value of the Fano factor does not change at all the validity of the discussion in Ref. [40].

Next, we discuss the region (iv) where R_{d1} rapidly decreases in increasing of V due to the influence of a thermal excitation current [see Fig. 1(f)]. Although the noise signals are scattered, the average value of the Fano factor approaches $F \sim 1$. This full-shot noise behavior has a different origin from that observed in region (ii). The thermal excitation current consists of the following processes. An electron is excited to the conduction band of (Ga,Mn)As by thermal agitation, followed by a radiative recombination after diffusion, as shown in Fig. 1(f). This process is the same as in a usual p-n junction under forward bias. In this situation, full-shot noise is theoretically expected, as the thermal excitation and radiative recombination generate two-thirds and one-third of the full-shot noise, respectively. Thus full-shot noise is realized in total [52].

Now we discuss the mechanism of the reduced Fano factor in the region (iii). As direct tunneling is energetically prohibited here, electrons in the n-GaAs have to pass through LSs within the (Ga,Mn)As [30], as shown in Fig. 1(e). In a germanium Esaki diode exhibiting a clear negative differential resistance, full-shot noise is reported in this region [48]. The present reduced Fano factor obtained in region (iii) is most likely due to LSs. The obtained Fano factor >0.87 is always larger than expected for a random distribution ($F = 3/4 = 0.75$) [9], indicating that LSs are nonuniformly distributed. This is consistent with the concentration of dopants being much larger on the (Ga,Mn)As side than on the n-GaAs side, as shown in Fig. 1(e). The importance of the LSs for tunneling in (Ga,Mn)As spin Esaki diodes has been demonstrated also in other studies. Tunneling anisotropic magnetoresistance measurements on similar devices have shown the change of the transport mechanism between regions (ii) and (iii) [34]. Further, the I-V characteristic of the present junction is well explained by theoretical work taking the impurity band in (Ga,Mn)As into account [41].

Finally, in the region (i), the reduction of the Fano factor can be explained as follows. The negative bias voltage widens the depletion layer [53], resulting in an increase of the contribution of sequential tunneling events, as shown in Fig. 1(c). In this region, only the LSs on the n-GaAs side can contribute to the sequential process. Consequently, the reduction of the Fano factor is likely due to the sequential tunneling through the LSs in the depletion layer.

B. Double junction (Setup D)

In the Setup D, one has to distinguish between parallel (P) and antiparallel (AP) configurations of the relative magnetization directions of the two ferromagnetic (Ga,Mn)As electrodes. In the AP configuration, the spin accumulation in the GaAs channel underneath and between ferromagnetic electrodes is typically much larger than in case of the P configuration [37]. Figure 4(a) shows the I-V characteristics for P and AP configurations (the left axis) and the differential resistance of each junction for P configuration (the right axis). Although V shows a clear spin valve signal [33] in the magnetic field sweep, it is just 0.2% of the offset signal due to the large junction resistance. Hence, it is hard to see a difference in I-V characteristics between the P and AP configurations. In this study, the current polarity is defined as the forward direction for J1, which is the opposite direction for J2. Thus, the sign of the bias is opposite for the two junctions, and therefore the negative differential resistance region (iii) is achieved at around $V = +0.5V$ and -0.5 V for J1 and J2, respectively. Note that when one junction is in the region (iii), the other is in the direct tunnel region (ii), as clearly seen in the right axis in Fig. 4(a).

Figure 4(b) shows the bias dependence of the obtained S_I extracted from Eq. (2). S_I is clearly the same for AP and P configurations, which indicates the negligibly small influence of the spin accumulation. Assuming the latter, we can now discuss the relation between S_I in Setup D and Setup S. Equation (3) indicates that S_I depends on the quantitative balance between R_{d1} and R_{d2}. Based on the result in Setup S, we first consider the situation that shot noise of each junction
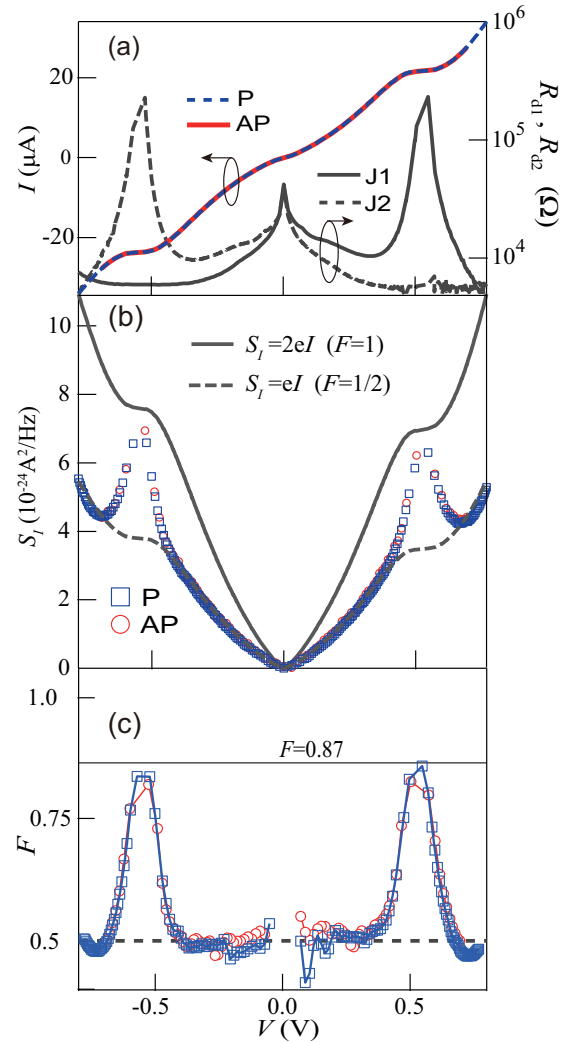

FIG. 4. (a) I-V characteristics of the junctions in series as a function of a bias voltage for parallel (P) and antiparallel (AP) configurations. The right axis shows R_{d1} and R_{d2} of each junction for P configuration. (b) Measured S_I in Setup D for P and AP. The solid and dashed lines show two shot noise limits. (c) Estimated $F (\equiv S_I/2eI)$ by using the data in (b).

exhibits the full-shot noise ($S_I^{J1} = S_I^{J2} = 2eI$). As a result, S_I in the series junction is expected to be eI for $R_{d1} \sim R_{d2}$ and $2eI$ for $R_{d1} \ll R_{d2}$ or $R_{d1} \ll R_{d2}$. In Fig. 4(b), the measured S_I is compared with these two limits, namely, a solid line for $S_I = 2eI$ and a broken line for $S_I = eI$. Except for the strong asymmetric case due to the negative differential resistance regions around $V = \pm 0.5$ V, S_I matches the broken line. This result indicates full-shot noise in region (ii), which is consistent with the result for Setup S.

In order to see it more clearly, the bias voltage dependence of the estimated $F (\equiv S_I/2eI)$ is plotted in Fig. 4(c). Here, the two limits yield $F = 1/2$ for $R_{d1} \sim R_{d2}$ [horizontal dotted line in Fig. 4(c)] and $F = 1$ for $R_{d1} \gg R_{d2}$ or $R_{d1} \ll R_{d2}$. It is clear that the curves are in good agreement with the $F = 1/2$ line except around $V = \pm 0.5$ V. For these voltages the maximum values of F are clearly smaller than unity. Now, defining the Fano factor of J1 and J2 junctions as F_1 and F_2, respectively,

we obtain the relations: $F = F_1$ for $R_{d1} \gg R_{d2}$ and $F = F_2$ for $R_{d1} \ll R_{d2}$. Indeed, the maximum values of the F peaks agree with value of $F_1(=0.87)$ obtained in region (iii) of Setup S, as shown in Fig. 4(c) as a horizontal solid line. These results indicate that Setup S and Setup D show consistent results.

The present series circuit consists of a nonmagnetic channel sandwiched by two ferromagnetic materials through a tunnel barrier. The shot noise in such a system has been studied theoretically [54,55], indicating that the Fano factor depends on the magnetic configuration. In fact, experimental studies on layered double-barrier magnetic tunnel junctions report magnetic configuration dependent shot noise and discuss spin relaxation in the middle layer [56,57]. However, no significant difference of the Fano factor between P and AP configurations was detected in the present study. In our lateral device, the spin accumulation in the n-GaAs channel is energetically small compared to the voltage drop across J1 and J2, thus too small to affect the tunneling current across the junctions.

IV. CONCLUSION

We measured shot noise properties of (Ga,Mn)As/GaAs-based spin Esaki diode junctions over a wide bias voltage range. We have clarified that transport through the Esaki junction changes dramatically depending on an applied bias. In the low bias voltage regime, full-shot noise ($F = 1$) associated with direct tunneling was observed. This was also observed in the large positive bias region, resulting from recombination of the thermal diffusion current. On the other hand, we observed the reduced Fano factor in the negative differential resistance region and in the large negative bias region. These reductions can be explained by taking the excess current via LSs into consideration. In addition, we also measured shot noise of a series circuit of two spin Esaki diode junctions in a lateral geometry and obtained consistent results for the single junction and double junction cases. Our findings of bias dependence of the Fano factor in the Esaki diode junction provide an important information for in-depth understanding of the transport mechanism in the presence of the LSs.

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