Realizing spin qubits in ^{28}Si/SiGe: heterostructure gating, qubit decoherence and asymmetric charge sensing

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Contents

1. Introduction

Since the advent of computing, this technology has brought substantial economic growth and scientific discoveries. This success is based on the ability for computers to solve some kinds of problems faster than humans. However, there is still a class of intractable problems that is hard to solve for classical computers, meaning that the computing time and memory scale exponentially with the problem size [1]. A new kind of computer, harnessing the quantum superposition and entanglement for computation, should be able to solve some of these problems in polynomial time [1, 2]. Such a universal quantum computer is proven to solve problems such as prime factorization, finding discrete logarithms, solving linear systems of equations and searching unsorted data faster than its classical counterpart for large problem sizes [3–6]. Apart from these applications, a quantum computer is predicted to be highly efficient in simulating physical systems governed by quantum mechanics, offering insights which would be hard to obtain in the real system [7–10]. For example, the development of drugs could be sped up by quantum simulation [11].

The fundamental building block of a quantum computer is the qubit: a two-level quantum system allowing the superposition of the levels as well as the entanglement between multiple qubits. Qubits can be realized in a multitude of physical systems including photons, trapped ions and superconducting circuits [12–15].

The field of quantum computing is currently in a stage of noisy intermediate-scale quantum technology, where around 50 noisy qubits have been demonstrated in a single device [16, 17]. Although quantum supremacy, the point where it takes longer to calculate a specific algorithm in a classical supercomputer than on a quantum computer, is claimed to be surpassed [17], there is still a long way to go for the realization of a fault tolerant universal quantum computer [18, 19]. Especially the large number of physical qubits expected to be required for the implementation of one logical, meaning error-corrected, qubit imply that scalable qubit implementations have to be developed for progress in fault-tolerant quantum computing.

A particularly promising approach is the implementation of spin qubits in gate-defined semiconductor nanostructures due to the existing highly scalable manufac-

turing techniques and the good tunability of the confinement potential [20]. Most of the preliminary work in this branch of quantum computing research was done in GaAs, building on advancements in quantum-transport-, Coulomb-blockade- and spin-blockade-physics [21]. Yet, the strong fluctuating Overhauser field of the host nuclei and the strong spin-orbit coupling strength were limiting the qubit coherence with dephasing times in the order of 10 ns [22–24].

By moving to silicon as the basis for gate-defined quantum dots, with only 4.685 % of the nuclear spin carrying isotope ^{29}Si in the natural Si composition and a weak spin-orbit interaction, the interaction of the spin with its environment is reduced [25–32]. The isotopical purification of ^{28}Si allows to engineer a virtually nuclear-spin-free host material [33–35]. These improvements yielded remarkable dephasing times in the order of 120 µs in metal oxide semiconductor (MOS) structures [31] and 20 µs for electron spin qubits in ^{28}Si/SiGe heterostructures [36, 37] with control-fidelities surpassing 99.9 % [36].

In our group, we have developed a qubit platform based on gate-defined quantum dots (QDs) in ^{28}Si/SiGe heterostructures in previous work [38–40]. The heterostructures intended for qubit experiments feature a quantum well (QW) which is grown by means of molecular beam epitaxy (MBE) using an isotopically purified ^{28}Si source crystal with only 60 ppm of remaining ^{29}Si. Combining this MBE-grown heterostructure with a magnet placed in the plane of the QD-defining gate layer, we have a unique framework for qubit realization in a collaborative effort with the group of Lars Schreiber at the RWTH Aachen. Previous work demonstrated single electron operation in our qubit platform.

In this thesis we set out to deepen our understanding of the heterostructure properties to reach high-yield single electron tuning, since for example charge reconfigurations in defect trap states impede the device tuning. In parallel, a demonstration of qubit operation and with this a measurement of qubit characteristics such as relaxation and dephasing times remained as the aim of this thesis.

The current research in quantum computing is moving towards qubit operation at temperatures around 1 K where more cooling power is available in the refrigerators, in an effort towards the integration of control electronics in vicinity of the qubits [41]. Signal-to-noise ratio (SNR) and bandwidth plays an important role for a robust and fast measurement of the spin, especially at elevated temperatures [42]. A new kind of charge sensor, presented in the last part of this thesis, is a promising candidate to deliver these features.

This thesis is organized as follows:

- In chapter 2 we will discuss the fundamental theoretical concepts required for a basic understanding of the experimental studies presented in this thesis.
- In chapter 3 we will present a characterization of the gated undoped Si/SiGe heterostructures building the basis for our nanostructure devices.
- In chapter 4 we will show the initial tuning of a single quantum dot with an adjacent charge sensor in ^{28}Si/SiGe.
- In chapter 5 we will demonstrate the spin-to-charge conversion and study the spin relaxation in order to extract the valley splitting in our qubit device.
- In chapter 6 we will introduce the spin manipulation via electric dipole spin resonance (EDSR) and access the dephasing and decoherence times in our qubit.
- In chapter 7 we will study a concept for a new kind of charge sensor aiming towards a large SNR and high bandwidth spin readout.

2. Fundamental concepts

In this chapter, we will discuss the underlying concepts required for an understanding of the experiments studied in this thesis.

2.1. Silicon and germanium material system

The devices studied in this thesis are based on Si/SiGe QW-heterostructures. Therefore, we first turn towards the properties of this material system. Fig. 2.1 shows the simulated band structure of silicon (a) and germanium (b). Both materials are indirect semiconductors, which manifests in a conduction band minimum that is not at the Γ-point of the Brillouin . The band gaps of Si and Ge have been determined to 1.12 eV and 0.661 eV, respectively [43, 44]. Both elements crystallize in a diamond lattice with lattice constants of $a_{\mathrm{Si}} = 543.1\,\mathrm{pm}$ for silicon and $a_{\mathrm{Ge}} = 565.8\,\mathrm{pm}$ for germanium [43, 44]. The two elements are miscible into the alloy $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ with any desired Ge content x. The resulting lattice constant $a_0(x)$ of the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ is described by Vegard's law [45]

$$a_0(x) = a_{\mathrm{Si}}(1-x) + a_{\mathrm{Ge}}x. \tag{2.1}$$

Fig. 2.2 a shows the band gap for relaxed $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ bulk material with a monotonous decrease in band gap for increasing Ge content x. Despite of the larger band gap of pure Si compared to any $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ alloy, it is possible to engineer a Si-QW heterostructure.

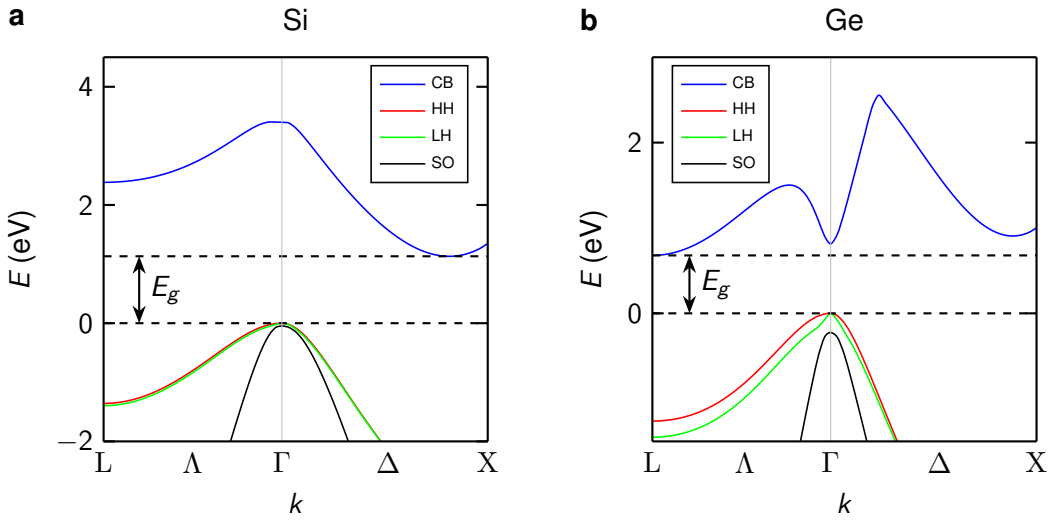

Figure 2.1. – **a** The band structure of silicon with the conduction (blue), heavy-hole (red), light-hole (green) and split-off (black) bands. The indirect band gap of Si with $E_g = 1.12\,\text{eV}$. **b** The band structure of germanium with an indirect band gap of $E_g = 0.661\,\text{eV}$. Simulated with [46]. Adapted from [47].

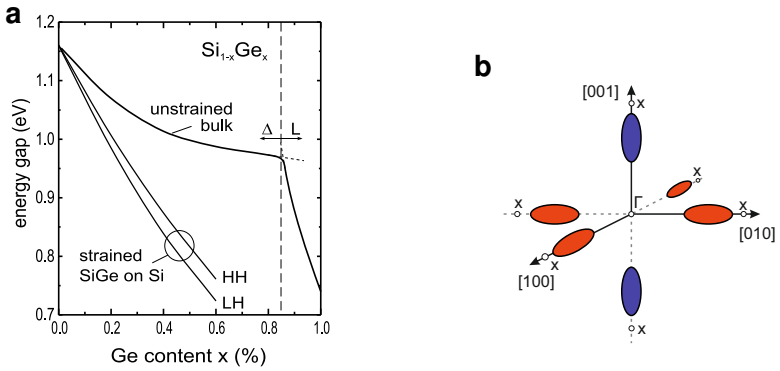

Figure 2.2. – **a** The band gap of unstrained $Si_{1-x}Ge_x$ as a function of the Ge content x is shown in the upper line. The nature of the band gap is Si-like with the conduction band minimum lying in the Δ-direction for $x < 0.85$ and Ge-like with the conduction band minimum located at the L point of the Brillouin zone for $x > 0.85$. The lower lines cover strained $Si_{1-x}Ge_x$ which is not covered in this thesis. Republished with permission of IOP Publishing, Ltd and AIP Publishing, from [48, 49]; permission conveyed through Copyright Clearance Center, Inc. **b** The surfaces of constant energy close to the conduction band minima in the Si Brillouin zone forming ellipsoids. In the case of biaxial tensile strain applied to bulk Si in the [100] and [010] directions, the ellipsoids in the [001] direction (shown in blue) are shifted lower in energy, while the ellipsoids in the [100] and [010] directions are shifted up in energy.

2.2. Si/SiGe heterostructures

When Si is grown onto a relaxed $Si_{1-x}Ge_x$ substrate, the Si lattice adapts to the larger SiGe lattice constant, introducing strain in the Si layer. This strain lifts the sixfold valley degeneracy present in bulk Si, as depicted in Fig. 2.2 b. The twofold degenerate Δ_2 valleys are shifted down in energy and the fourfold degenerate Δ_4 valleys are shifted up in energy in the strained Si. Furthermore, the twofold ground state degeneracy is lifted by the QW confinement potential leading to the valley splitting E_{VS} [50]. The band gap of the strained Si gets reduced, which leads to a type-II band alignment in a $Si/Si_{1-x}Ge_x$ QW heterostructure [39].

Fig. 2.3 a shows the simulated conduction band edge energy as a function of the coordinate in growth direction z in an undoped Si/SiGe QW heterostructure. Due to the absence of doping, the band edge energy is flat with steps due to differences in the material composition. The Si QW as well as the Si cap represent a minima of the conduction band edge energy. In this flat-band condition the first subband in the QW is above the Fermi energy indicated by the dashed line and no electrons are allowed to enter the QW, indicated by the zero electron density in Fig. 2.3 a. Therefore, it is mandatory to add a gate oxide and a metal layer further referred to as accumulation gate, located at $z < 0\,\text{nm}$, in order to manipulate the band edge energy. A positive voltage applied to the TiAu accumulation gate lowers the band edge energy, as shown in Fig. 2.3 b, eventually leading to the first subband energy in the QW shifting below the Fermi energy. This allows electrons to enter the QW, indicated by the non-zero electron density in the QW region. When only the first subband is occupied, the electrons form a two dimensional electron gas (2DEG). Note that no electron density is predicted to accumulate in the 1 nm Si cap, as the larger confinement energy contribution keeps the first subband energy above the Fermi energy. The 2DEG can be characterized by magnetotransport studies, which will be covered in the following section.

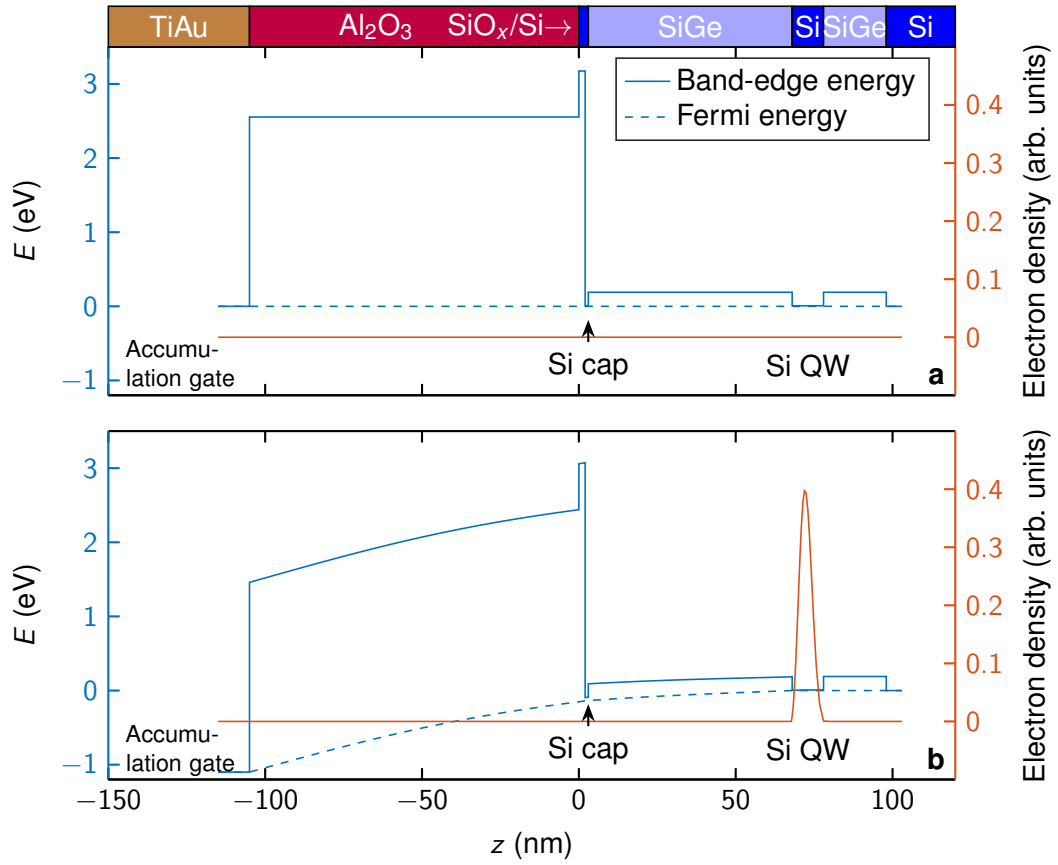

Figure 2.3. – The simulated conduction band edge energy of a Si/SiGe heterostructure with an Al_2O_3 gate oxide and a metal accumulation gate as a function of the coordinate z oriented along the growth direction (blue). The simulated electron density as a function of z is plotted in orange. **a** The flat band structure in the case of 0 V applied to the accumulation gate with respect to the grounded QW. As the first subband in the QW is above the Fermi energy, no charge carriers are allowed in the QW resulting in zero electron density. **b** Here, 1.1 V is applied to the accumulation gate, resulting in a band bending which induces a non-zero charge carrier density in the QW as the first subband moves below the Fermi energy. Adapted from [47].

2.3. Magnetotransport properties of two dimensional electron gases

A 2DEG patterned in a Hall bar geometry is schematically depicted in Fig. 2.4, with the ohmic contacts indicated by the dark gray regions. A typical magnetotransport measurement accesses the longitudinal and transversal resistivities ρ_{xx} and ρ_{xy} in a four-point measurement of the longitudinal and transversal resistance $V_{\parallel}/I$ and $V_{\perp}/I$, respectively and the consideration of the Hall bar width and length dimensions:

$$\rho_{xx} = \frac{V_{\parallel}}{I}\frac{W}{L} \tag{2.2}$$

$$\rho_{xy} = \frac{V_{\perp}}{I}. \tag{2.3}$$

The out-of-plane magnetic field B_{ext} is varied and due to the Lorentz-force acting upon the moving charge carriers, a non-zero Hall resistance is detected. In the regime described by the classical Hall effect [51], $V_{\perp}$ rises linearly with the magnetic field while $V_{\parallel}$ stays constant. The resulting longitudinal and transversal resistivities are described by

$$\rho_{xx} = \frac{m^*}{ne^2\tau} = \frac{1}{ne\mu} \quad \text{and} \tag{2.4}$$

$$\rho_{xy} = \frac{B_{ext}}{en}, \tag{2.5}$$

where m^* is the effective mass of the charge carriers, e is the elementary charge, n is the charge carrier density, τ is the mean scattering time and $\mu = \frac{e\tau}{m^*}$ is the charge carrier mobility [52].

The Fermi wave vector is then described by

$$k_F = \sqrt{\frac{4\pi n}{g_s g_v}}, \tag{2.6}$$

with g_s and g_v being the spin and valley degeneracies, respectively. The Fermi velocity v_F and the mean free path l are obtained as

$$v_F = \frac{\hbar k_F}{m^*} \quad \text{and} \tag{2.7}$$

$$l = v_F\tau = \frac{\hbar}{e}\mu\sqrt{\pi n}. \tag{2.8}$$

The mean free path l is a measure for the average length the charge carriers travel between two scattering events.

By confining the 2DEG in the two in-plane dimensions, it is possible to create QDs in the Si host material. We will discuss the characteristic properties of these systems in the following section.

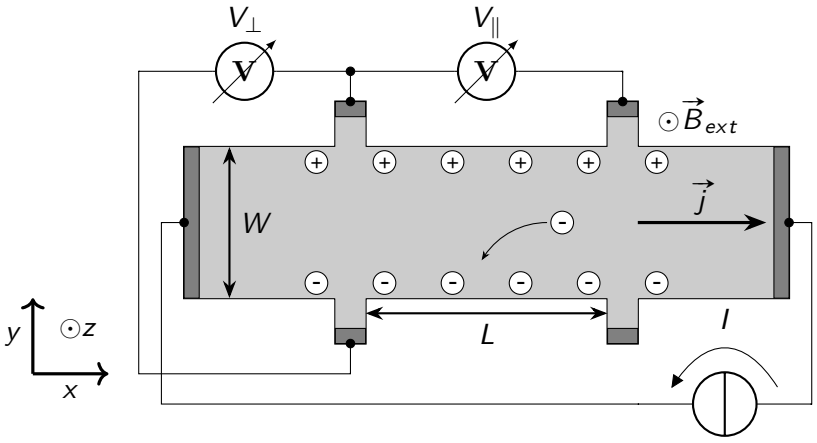

Figure 2.4. – A schematic illustration of a Hall bar sample with width W and segment length L. A current density $\vec{j}$ is injected in the x direction. The external magnetic field $\vec{B}_{ext}$ is oriented along the z direction, leading to a deflection of the electrons due to the Lorentz force. Charges accumulate on the edges of the sample, inducing a non-zero transversal voltage $V_\perp$.

2.4. Quantum dots in Si/SiGe

An island formed in the 2DEG due to lateral confinement, commonly referred to as single quantum dot (SQD), coupled to the source and drain reservoirs via tunnel contacts is illustrated in Fig. 2.5. A plunger gate is capacitively coupled to the SQD. This structure is commonly approximated by a circular disc in the 2DEG with a radius r and an electron charge of $-eN$ for N electrons occupying the SQD. The self-capacitance of this disc is described by

$$C = 8\epsilon\epsilon_0 r, \tag{2.9}$$

with ϵ being the dielectric constant of the surrounding material, which is assumed to be homogeneous in this approximation, and the vacuum permittivity ϵ_0 [52]. The

electrostatic energy of the island is then given by

$$E_{\mathrm{elstat}}(N) = \frac{e^2N^2}{2C} = \frac{e^2N^2}{16\epsilon\epsilon_0 r}. \tag{2.10}$$

The energy required to add the $(N+1)$-th onto a SQD occupied with N electrons is the difference between the electrostatic energies

$$E_c(N+1) = E_{\mathrm{elstat}}(N+1) - E_{\mathrm{elstat}}(N) = \frac{e^2}{C}\left(N+\frac{1}{2}\right) \overset{N\gg 1}{\approx} \frac{e^2}{C}N = \frac{e^2}{8\epsilon\epsilon_0 r}N. \tag{2.11}$$

However, the term charging energy is commonly used for

$$\Delta E_c = E_c(N+1) - E_c(N) = \frac{e^2}{C} = \frac{e^2}{8\epsilon\epsilon_0 r}. \tag{2.12}$$

For a SQD with a radius of 50 nm and $\epsilon = 11.7$ of Si this characteristic energy scale is $\Delta E_c \approx 3.9\,\mathrm{meV}$, which corresponds to a temperature of 45 K.

The single-particle level spacing can be approximated using the model of a quantum mechanical harmonic oscillator [52]

$$\Delta = \hbar\omega_0 = \frac{\hbar^2}{4m^*r^2}. \tag{2.13}$$

For a SQD in Si with $m^* = 0.19\,m_e$ and a radius of 50 nm, this energy scale computes to 40 µeV or a temperature of 0.5 K. This is two orders of magnitude smaller than ΔE_c indicating that the total energy of the SQD is governed by the Coulomb interaction energy for the laterally defined SQDs studied in this thesis.

Considering the capacitively coupled plunger gate shown in Fig. 2.5, the ground state energy for a SQD occupied with N electrons depends on the plunger gate voltage V_{pg}

$$E_N(V_{pg}) = E_N(V_{pg}^0) - eN\alpha_{pg}(V_{pg} - V_{pg}^0), \tag{2.14}$$

for small ranges around a fixed V_{pg}^0 with $\alpha_{pg} = \frac{C_{pg}}{C}$ being the lever arm describing the ratio of the capacitive coupling C_{pg} of the plunger gate to the SQD to the self-capacitance C [52]. For a SQD with initially $N-1$ electrons we define the electrochemical potential for increasing the electron occupation to N as

$$\mu_N(V_{pg}) = E_N(V_{pg}) - E_{N-1}(V_{pg}). \tag{2.15}$$

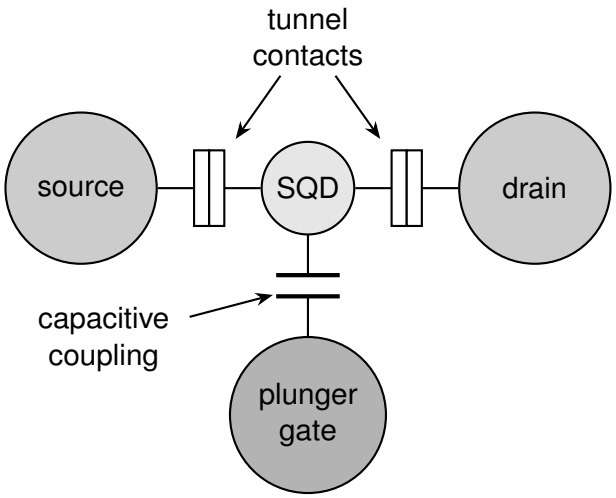

Figure 2.5. – A schematic depiction of a SQD with tunnel contacts to source and drain reservoirs. The plunger gate couples capacitively onto the SQD.

2.4.1. Coulomb blockade

Fig. 2.6 shows a schematic representation of the energetic situation for a SQD in between source and drain reservoirs. The electronic levels in the source and drain reservoirs are filled up to the electrochemical potentials μ_S and μ_D, respectively, in the case of low temperatures. We first consider the situation where only a small bias voltage is applied between the reservoirs. In Fig. 2.6 a the SQD is occupied with N electrons, as $\mu_N < \mu_D < \mu_S$. However, the energy required to add the $(N+1)$-th electron onto the SQD is not available, as $\mu_{N+1} > \mu_S > \mu_D$. This leads to a constant occupation of the SQD with the same N electrons, which effectively blocks the current flowing between the source and drain reservoirs. This situation is commonly termed Coulomb blockade since the Coulomb interaction prevents a $(N+1)$-th electron to enter the SQD. Using the plunger gate voltage, combining Eqs. 2.14 and 2.15 the electrostatic potential can be tuned with

$$\mu_N(V_{pg}) = \mu_N(V_{pg}^0) - e\alpha_{pg}(V_{pg} - V_{pg}^0). \tag{2.16}$$

Fig. 2.6 b shows the situation where Coulomb blockade is lifted, by tuning μ_{N+1} to a value in between μ_S and μ_D by a change of V_{pg}. In this situation either $N+1$ or N electrons can occupy the SQD, allowing for sequential transport of electrons through the SQD, indicated by the arrows in Fig. 2.6 b.

2.4.2. Coulomb diamonds

Considering the current through the SQD as a function of the bias voltage V_{SD} and V_{pg}, we expect the regions of suppressed current to form diamond shaped regions, as depicted in Fig. 2.7 a. The grey regions mark a transport current through the SQD. The borders of the blockade regions, commonly referred to as Coulomb diamonds, mark the configurations of V_{SD} and V_{pg} where either of the reservoir chemical potentials is aligned with a SQD chemical potential, as schematically depicted in Fig. 2.6 c for $\mu_S = \mu_{N+1}$ and Fig. 2.6 d for $\mu_D = \mu_{N+1}$. We mark the configurations in Fig. 2.7 a with the labels corresponding to the subfigures in Fig. 2.6.

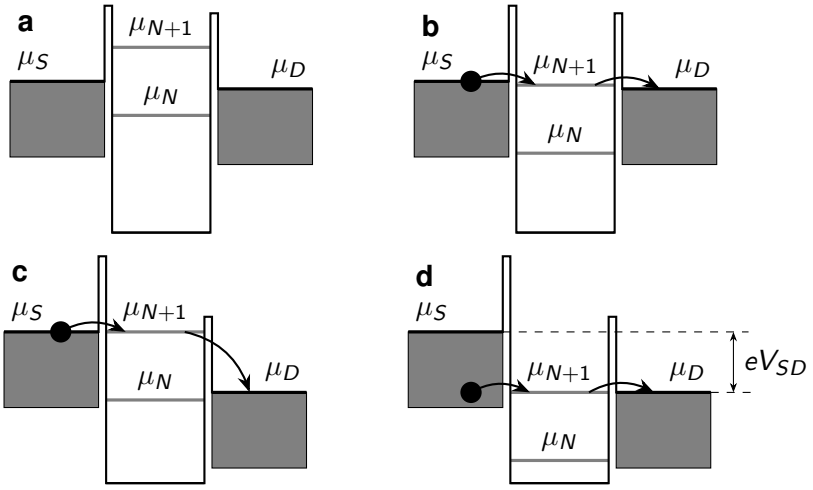

Figure 2.6. – A schematic illustration of the electrochemical potentials in a SQD occupied with N electrons with small (a, b) and large (c, d) source-drain bias voltages. **a** There are no energy levels in the QD lying in between the electrochemical potentials of source and drain μ_S and μ_D. The system is considered to be in Coulomb blockade as no electron transport is allowed. **b** The level μ_{N+1} lies in the source-drain bias window and sequential tunneling of electrons is allowed. **c** μ_{N+1} is aligned with μ_S and transport is allowed. **d** μ_{N+1} is equal to μ_D and current is allowed to flow. The difference in the source and drain electrochemical potentials eV_{SD} is indicated on the right hand side.

In the following, we consider the case where the drain reservoir is grounded while the bias voltage is applied to the source reservoir. So far we only took the capacitive coupling of the plunger gate into account, but also the reservoirs are coupled capacitively to the SQD. The negatively sloped diamond borders, labeled

m_- in Fig. 2.7 a, satisfy

$$\Delta\mu_N = \mu_D = 0, \tag{2.17}$$

meaning that the capacitive coupling of the source reservoir and the plunger gate keeps the SQD electrostatic potential aligned with the potential of the grounded drain reservoir. The shift in μ_N in response to changes of ΔV_{SD} and ΔV_{pg} can be described by

$$\Delta\mu_N = -e\Delta V_{SD}\frac{C_S}{C} \text{ and} \tag{2.18}$$

$$\Delta\mu_N = +e\Delta V_{pg}\frac{C_{pg}}{C}. \tag{2.19}$$

Here, C_S describes the capacitive coupling of the source reservoir onto the SQD. Dividing Eq. 2.18 by Eq. 2.19, we get an equation for the negative slope m_- of the diamond borders described by Eq. 2.17

$$m_- = \frac{\Delta V_{SD}}{\Delta V_{pg}} = -\frac{C_{pg}}{C_S} = -\frac{\alpha_{pg}}{\alpha_S} \tag{2.20}$$

with the source lever arm

$$\alpha_S = \frac{C_S}{C}. \tag{2.21}$$

In a similar fashion we can derive the slope of the positively sloped diamond borders

$$m_+ = \frac{C_{pg}}{C - C_S}. \tag{2.22}$$

Inserting Eqs. 2.20 and 2.22 in Eq. 2.21, we can express the source lever arm as a function of the negative (m_-) and positive (m_+) diamond border slopes

$$\alpha_S = \frac{m_+}{m_+ - m_-} \overset{m_+>0;\ m_-<0}{=} \frac{|m_+|}{|m_+| + |m_-|}. \tag{2.23}$$

Fig. 2.7 b shows the current I through the SQD as a function of V_{pg} for a small fixed V_{SD} indicated by the dotted line in Fig. 2.7 a. Peaks in I are expected when the Coulomb blockade is lifted. On each side of the peaks, $\mathrm{d}I/\mathrm{d}V_{pg}$ is large, yielding a large change in I for a small change in V_{pg}. In the same way the current signal is sensitive to changes in V_{pg}, it is also sensitive to any other changes to the electrostatic potential. An electron entering or leaving a nearby QD may induce such a change in

the electrostatic potential, which can be detected in the change of the current flowing through the SQD. Thus we can employ a SQD as a charge sensor for nearby QDs. This is especially useful in configurations where the tunnel barriers are too opaque for the tunnel current to be detected. The sensor has to be in the regime with large $\mathrm{d}I/\mathrm{d}V_{pg}$ in order to have a large sensitivity, indicated by the working point marked in Fig. 2.7 b.

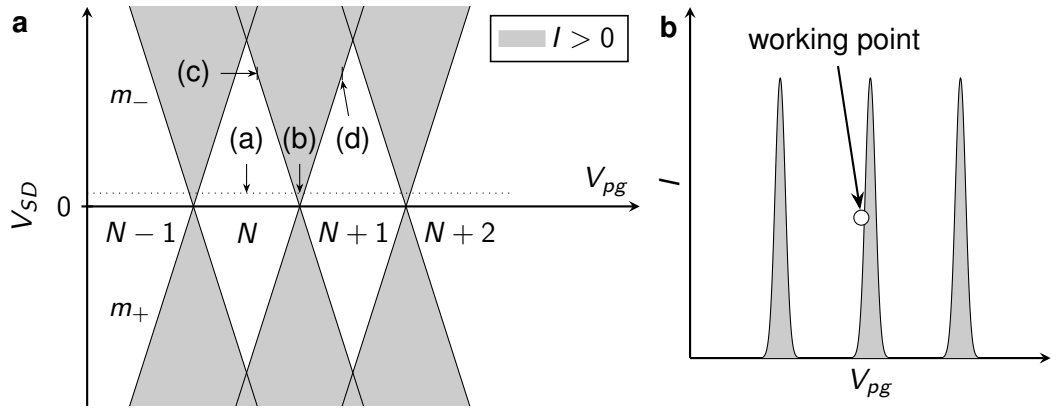

Figure 2.7. – **a** A schematic illustration of the current through a SQD as a function of the source-drain voltage V_{SD} and the plunger gate voltage V_{pg}. The regions with significant current flow are indicated in grey, while the white regions mark the Coulomb diamonds, where current flow is suppressed due to Coulomb interaction. The points marked with the labels (a) to (d) correspond to the configurations depicted in Fig. 2.6. The electron occupation of the SQD, indicated by the labels from (N-1) to (N+2), stays constant inside each Coulomb diamond. **b** The schematic current I through a SQD as a function of V_{pg} at the bias voltage indicated by the dotted line in **a**. Sharp Coulomb peaks emerge where the Coulomb blockade is lifted. Choosing a working point on the side of a peak, as indicated by the circle, the SQD can be used as a charge sensor with a large change in I for a small change in the electrostatic potential.

2.5. Double quantum dots

For some experiments, such as the demonstration of two-qubit logic or the implementation of singlet-triplet qubits a more complex structure than a SQD is required. Fig 2.8 shows the schematic for a structure with two serial QDs placed in between the reservoirs, with two corresponding plunger gates. In these gate-defined double quantum dots (DQDs), the inter-dot tunnel barrier between the QDs is tunable by

gate voltages, giving the freedom to transition the system from a large SQD to two separated QDs.

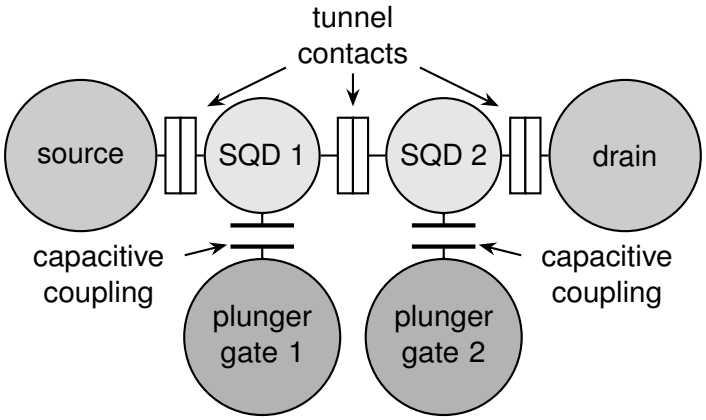

Figure 2.8. – A schematic illustration of two SQDs connected in series via tunnel contacts forming a DQD. The two separate plunger gates ideally act only capacitively on the corresponding QD.

Fig. 2.9 shows the transport current through a serial DQD as a function of the plunger gates of the two QDs for a variation of the inter-dot tunnel coupling. In Fig. 2.9 f the coupling is very large, with the conductance resonances showing one set of parallel lines characteristic for a SQD. Two sets of parallel lines emerge for decreasing tunnel couplings of Fig. 2.9 c-d, indicating the formation of a DQD system, with each set of lines representing the conductance resonances of the individual QDs. For even smaller tunnel coupling, shown in Fig. 2.9 a and b, transport is allowed only at the configurations, where both chemical potentials of the two QDs are aligned with each other and the reservoirs chemical potentials. The points where current can flow in this regime are commonly referred to as triple points, as the charge state of the system sequentially switches between three configurations.

A similar pattern is expected when a charge sensor is employed for the detection of the electron occupation, with two sets of parallel lines emerging in the derivative of the sensor current corresponding to a DQD system.

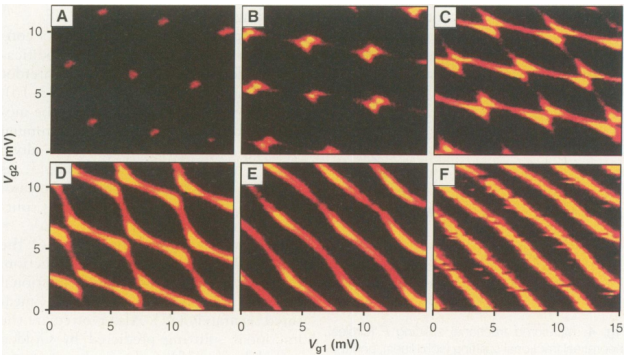

Figure 2.9. – The current through a DQD as shown in Fig. 2.8 as a function of the plunger gate voltages, here denoted as V_{g1} and V_{g2}. The bright values represent a significant current flow, while the dark values indicate a suppressed current flow. The coupling strength increases from A to F. The single set of parallel lines observed in F indicate a SQD. This SQD is split into two separate SQDs forming a DQD when the inter-dot tunnel coupling is decreased by the tuning of a gate voltage, with two sets of parallel lines emerging for a strongly coupled DQD in C-E and triple points being observed for weak inter-dot coupling in A and B. From [53]. Reprinted with permission from AAAS.

2.6. Single electron in magnetic field

We now consider a SQD in Si host material which is occupied by a single electron. For zero magnetic field, the single particle ground state is two-fold spin-degenerate. In a non-zero static magnetic field B, the spin-up and -down states $|\uparrow\rangle$ and $|\downarrow\rangle$ split by the Zeeman energy splitting

$$E_Z = g_s \hbar \gamma B = g_s \mu_B B \tag{2.24}$$

$$\text{with } \mu_B = \hbar\gamma = \frac{e\hbar}{2m_e}, \tag{2.25}$$

being the Bohr magneton, the gyromagnetic ratio γ and the electron g-factor g_s. These states build the basis for the electron spin qubits which will be discussed in the course of this thesis.

2.7. Electric dipole spin resonance using a magnetic field gradient

In the following, we will discuss how a magnetic field gradient can be utilized to manipulate single e^- spins in semiconductor heterostructures. One key requirement for this concept of manipulation is the presence of a small magnet, typically referred to as micro- or nanomagnet, that provides a local magnetic field gradient across the region where the electron is confined.

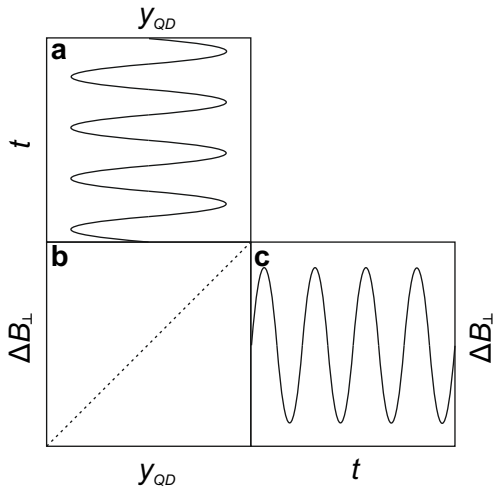

Figure 2.10. – Illustration of artificial spin-orbit coupling: **a** The QD position y_{QD} as a function of time t. In our device the change in position is induced by a microwave (MW)-pulse applied to a gate near the SQD confining the electron. **b** The field component $\Delta B_\perp$ perpendicular to B_{ext} as a function of y_{QD}. **c** The oscillating ac magnetic field perpendicular to B_{ext} in the electron's rest frame.

For EDSR the magnetic field component $B_\perp$ perpendicular (transversal) to $\vec{B}_{ext}$ is relevant. Fig. 2.10 a shows as schematic representation of the position of the electron wavefunction center y_{QD} as a function of time t. This oscillating displacement, in our case, is induced by applying an ac electric field to a gate in proximity of the SQD confining the electron. As illustrated in Fig. 2.10 b the transversal magnetic field gradient $\Delta B_\perp$ converts this oscillation in space into an ac magnetic field perpendicular to $\vec{B}_{ext}$ in the electrons rest frame, with the resulting oscillation shown in Fig. 2.10 c. This conversion of the electron motion into an ac magnetic field via the artificial spin-orbit coupling introduced by the local magnetic field gradient is the key component for all-electrical spin-manipulation in our ^{28}Si/SiGe spin-qubit device.

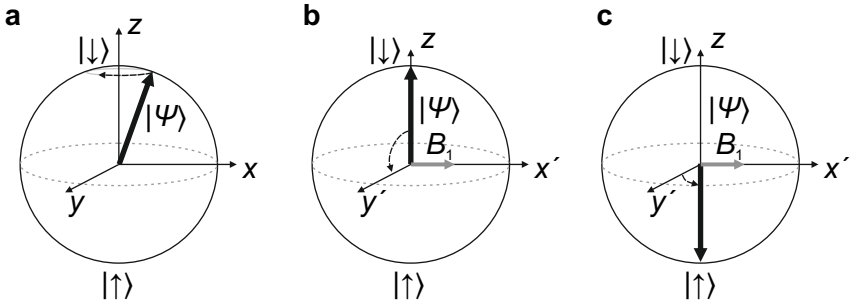

Figure 2.11. – Illustration of EDSR on the Bloch sphere with $|\downarrow\rangle$ $|\uparrow\rangle$ as the basis states for $|\Psi\rangle = a\,|\downarrow\rangle + b\,|\uparrow\rangle\,; a, b \in \mathbb{C}$: **a** The laboratory frame of reference, where $|\Psi\rangle$ precesses around the z-axis with ω_L. **b** The rotating frame of reference with x', y' rotating at ω_L around the z-axis. The ac magnetic field, shown in Fig. 2.10 c, converts into a stationary field B_1 along the x-axis. **c** The spin precesses around the B_1 axis, leading to Rabi oscillations.

Yet, for a controlled spin-manipulation it is required to couple resonantly to the electron spin. The spin precesses around $\vec{B}_{ext}$ with the Larmor frequency

$$f_L = \frac{\omega_L}{2\pi} = \frac{g\mu_B B}{h}, \tag{2.26}$$

where g is the electron g-factor, μ_B is the Bohr magneton, B is the total magnetic field along the nanomagnet axis and h is the Planck constant.

Fig. 2.11 a shows a representation of the electron wavefunction $|\Psi\rangle = a\,|\downarrow\rangle + b\,|\uparrow\rangle\,; a, b \in \mathbb{C}$ on the Bloch sphere with the qubit basis states $|\downarrow\rangle$ and $|\uparrow\rangle$ located on the poles of the sphere. In this representation the external magnetic field B_{ext} is oriented along the z-axis. For any $|\Psi\rangle$ not oriented parallel or anti-parallel to the z-axis, $|\Psi\rangle$ undergoes a precession around the z-axis at a frequency of $\omega_L = \frac{g\mu_B B}{\hbar}$. Fig. 2.11 b shows the reference frame rotating at ω_L indicated by the rotating basis vectors x' and y'. The electron is in the ground state $|\Psi\rangle = |\downarrow\rangle$ represented by the black arrow. The gray arrow represents the effective magnetic field B_1 created by the resonant driving in the nanomagnet gradient, which is stationary in this rotating frame of reference. This stationary field pointing along the x'-axis in turn leads to a precession of $|\Psi\rangle$ around the x'-axis at a Rabi frequency of $\omega_{Rabi} = \frac{g\mu_B B_1}{\hbar}$. The magnitude of B_1 depends on the microwave amplitude, the capacitive coupling of the driving gate onto the QD as well as the strength of the magnetic field gradient. Fig. 2.11 c shows the case where $|\Psi\rangle$ was rotated by 180° using a microwave pulse of the length $t_{MW} = \frac{\pi}{\omega_{Rabi}}$ resulting in $|\Psi\rangle = |\uparrow\rangle$.

3. Gating of undoped Si/SiGe 2DEG

In this chapter, we will discuss the solid-source MBE of the undoped Si/SiGe heterostructures used as the basis for all devices studied in the rest of the thesis. The charge carrier accumulation in these undoped structures will be demonstrated, followed by a characterization in the form of a magnetotransport study. We will focus on the behavior of Hall bar samples when a bias voltage is applied to the accumulation gate during the cool-down and how the sample characteristics change under illumination at cryogenic temperatures. In particular, we will discuss a previously proposed model [40, 54] based on interface trap states to explain the observed illumination behavior.

3.1. Growth and semiconductor layer structure

3.1.1. Molecular beam epitaxy

The Si/SiGe heterostructures used for the studies in this thesis were grown by means of solid source MBE based on recipes described in [38–40]. In Fig. 3.1 a the epitaxy chamber is schematically depicted. There are electron beam evaporator sources equipped with single-crystalline natural silicon and germanium, labeled Si and Ge, respectively. A smaller electron beam single-crystalline source equipped with single-crystalline isotopically purified ^{28}Si is located at the side of the chamber. The source crystal for ^{28}Si, provided by the Leibniz-Institut für Kristallzüchtung (IKZ) in Berlin, is purified to a residual concentration below 60 ppm ^{29}Si [34, 35]. The wafer, onto which the heterostructure is grown, is attached to the temperature-controlled manipulator shown at the top. The chamber is pumped to an ultra high vacuum (UHV) base pressure below 5×10^{-11} mbar.

In order to reach relaxed SiGe as a basis for a strained Si QW, a graded buffer is grown onto the initial (001) Si wafer. As shown in Fig. 3.1 b, within the graded buffer, the Ge content x is linearly increased over a thickness of several µm to the desired composition of $Si_{1-x}Ge_x$. This gradual increase in Ge content leads to a formation of threading dislocations which tend to stay in regions of constant Ge

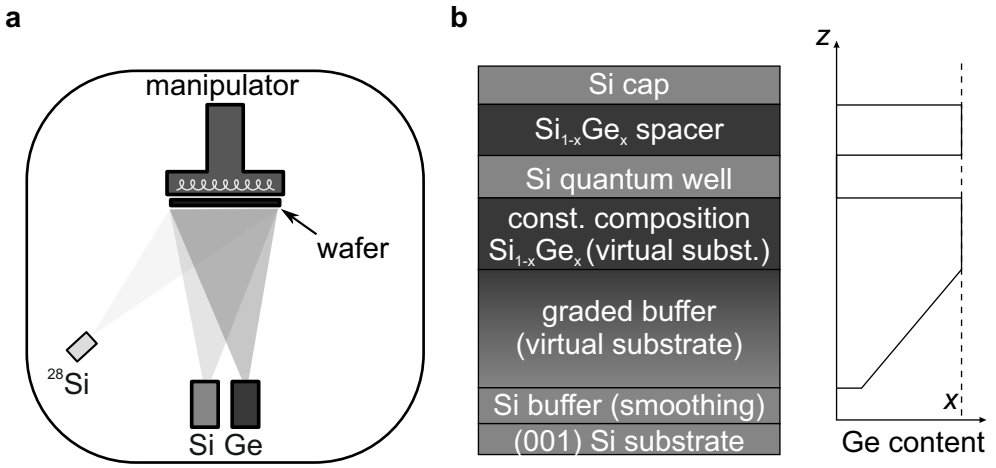

Figure 3.1. – **a** Schematic representation of the MBE ultra high vacuum chamber, including the source cells for Si, Ge and ^{28}Si. The wafer, colored black, is attached to the temperature controlled manipulator. **b** Illustration of a typical undoped Si/SiGe layer structure. The Ge content through the layer structure is indicated by the graph on the right and additionally by the tone of the background, with a light gray corresponding to a low Ge content while a dark gray represents a higher Ge content. The Ge content is linearly increased in the graded buffer layer.

content. Therefore, while the relaxation of the lattice is promoted, the dislocation density at the top of the graded buffer is reduced compared to other buffer concepts such as low temperature Si [38]. This graded buffer is followed by a layer of relaxed constant composition SiGe, completing the part of the heterostructure denoted as virtual substrate (VS) in Fig. 3.1 b. A strained Si QW is grown onto the VS. Either natural Si or ^{28}Si were employed as a QW material in this thesis. A SiGe spacer is grown to keep the QW away from the heterostructure surface, in order to reduce the scattering potential of defects for a 2DEG in the QW. Finally, a Si cap is employed to create a more stable natural oxide, compared to oxidized SiGe. A chemically stable surface protects the 2DEG properties from deterioration over time.

Fig. 3.2 gives a schematic representation of the two layer structures used for all Hall bar samples and QD devices studied in this thesis. Here, Fig. 3.2 a shows a natural Si QW structure with a 35 nm $Si_{0.7}Ge_{0.3}$ spacer and a 1 nm Si cap and Fig. 3.2 b shows an isotopically purified ^{28}Si QW structure with a 45 nm $Si_{0.7}Ge_{0.3}$ spacer and a 1.5 nm Si cap.

3.1.2. Post-growth processing

In further ex-situ processing, outside of the ultra high vacuum of the MBE, the ohmic contact to the QW is created by implantation of high energy ions and a rapid thermal activation anneal at a temperature of 700 °C for 30 s, both performed in the group of Kentarou Sawano (Advanced Research Laboratories, Tokyo City University, Tokyo, Japan). An Al_2O_3 gate oxide is applied by atomic layer deposition (ALD) at 300 °C. We employ a post-ALD anneal at 350 °C for 15 min in a forming gas environment (10% H_2 90% N_2). The bond pads for the ohmic contacts and the metallic gates are patterned by lithography and metallization in a standard evaporation chamber.

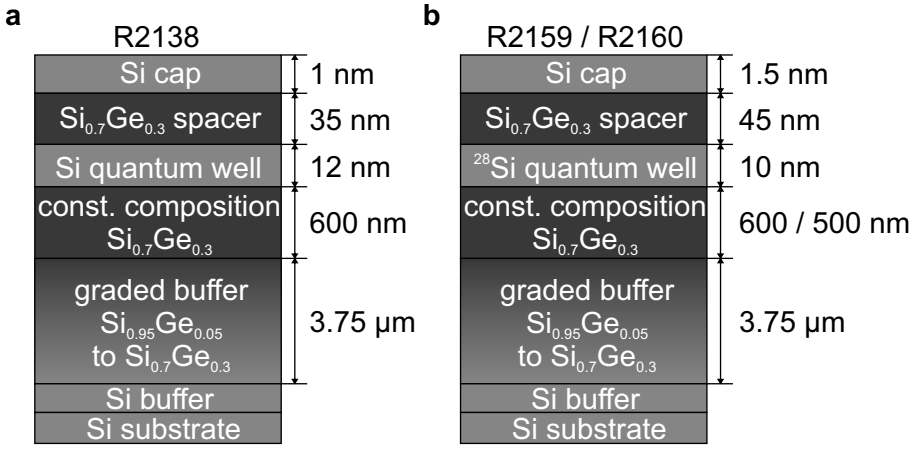

Figure 3.2. – Layer structures with the layer thicknesses noted on the right: **a** A natural Si QW with 35 nm $Si_{0.7}Ge_{0.3}$ spacer and 1 nm Si cap (R2138). **b** A ^{28}Si QW with 45 nm $Si_{0.7}Ge_{0.3}$ spacer and 1.5 nm Si cap (R2159 and R2160).

3.2. Hall measurement

In this section, we present the methods for the characterization of the Si/SiGe heterostructures studied in this thesis. We start with an overview of the Hall bar sample layout employed to access important heterostructure properties. We will proceed with a short description of the electrical magnetotransport measurement used for the determination of the charge carrier density and mobility throughout this chapter.

3.2.1. Hall bar sample layout

As shown in Fig. 3.3 a, we fabricate gate-induced Hall bars with the accumulation gate depicted in light gray. This gate is employed to induce charge carriers forming a 2DEG in the QW via the field effect. The Hall bar borders are given by the regions where the field induced by the gate is too weak to induce charge carriers in the QW. The individual Hall bar segments have a width-to-length ratio of $\frac{W}{L} = \frac{1}{15}$ with $W = 20\,\mu m$ and $L = 300\,\mu m$. The QW is contacted by ion-implanted regions, shown in dark gray in Fig. 3.3 a. An etched bar, indicated by the arrow in Fig. 3.3 a, prevents a leakage current from the accumulation gate bond pad (labeled 2) into the active Hall bar region which has occasionally been observed experimentally.

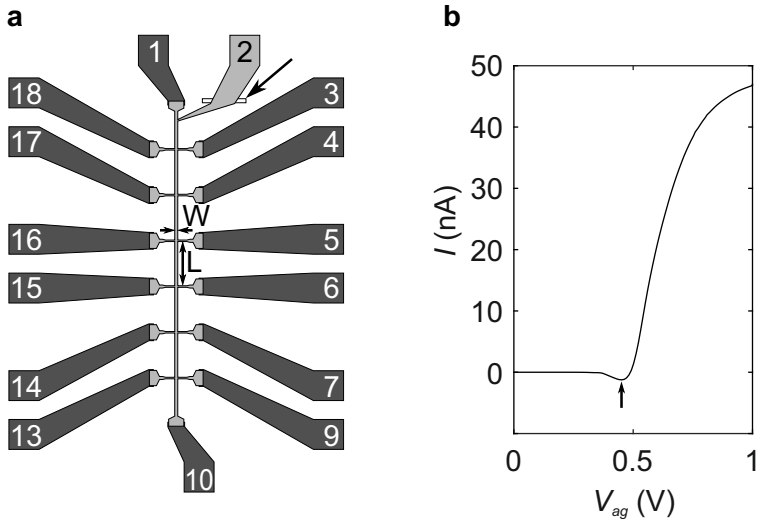

Figure 3.3. – **a** Hall bar sample layout, with implanted regions in dark gray, accumulation gate in light gray and an etched leakage current block marked by the arrow. The contact numbers which we will refer to in this chapter are indicated in white. **b** Current through a Hall bar sample as a function of the accumulation gate voltage V_{ag}. A significant current flows when a threshold voltage V_{thr} is reached. The maximum current through the sample is limited to 50 nA by a 100 MΩ resistor. The arrow marks the negative current feature, attributed to a non-linear I-V curve.

3.2.2. Accumulation of charge carriers in undoped Si/SiGe

Using a standard low-frequency lock-in technique, we measure the current through the sample as well as the longitudinal and Hall voltages in a four-point geometry for one or more segments of the gate-induced Hall bar. For details on the measurement setup, see A.2.1. This allows us to calculate ρ_{xx} and ρ_{xy}, the longitudinal and transversal resistivities, using the width-to-length ratio of the Hall bar following the Eqs. 2.2 and 2.3 in Sec. 2.3.

Fig. 3.3 b shows the current flowing through a typical Hall bar sample while increasing the accumulation gate voltage V_{ag} from 0 V to 1 V. We limit the maximum current flowing through the sample to 50 nA by a 100 MΩ series resistor to prevent damaging of the sample by resistive heating. In the regime of $0\,\mathrm{V} \leq V_{ag} \leq 0.5\,\mathrm{V}$ there is no significant current flow through the sample, which we attribute to the energy of the first 2D subband ($E_{1st\ sb}$) in the QW still lying above the Fermi energy (E_F). At about $V_{ag} = 0.5\,\mathrm{V}$, marked by the arrow in Fig. 3.3 b, we observe a negative current which is a measurement artifact, explained by a non-linear I-V curve exhibited for low densities of charge carriers in the QW causing a rectification of AC noise signals [55]. With increasing V_{ag} $E_{1st\ sb}$ in the QW gets shifted below E_F. The current through the sample approaches 50 nA, as the 2D charge carrier density in the QW (n_{QW}) increases, as a result of the capacitive coupling of the accumulation gate to the QW. V_{ag} thus is a tuning knob for the charge carrier density, which will be used to conduct the studies presented in the following sections.

3.2.3. Magnetotransport characterization

An exemplary magnetotransport measurement on the sample R2160A8 for a constant $V_{ag} = 1.1\,\mathrm{V}$ is shown in Fig. 3.4, where we plot ρ_{xx} and ρ_{xy} as a function of the external magnetic field B pointing in out-of-plane direction. For low magnetic fields, ρ_{xy} shows a linear behavior. The slope of ρ_{xy} allows the determination of the type and density of charge carriers via the theory of the classical Hall effect. As intended, we find the charge carriers to be electrons, with a density of $n = 5.8 \times 10^{11}\,\mathrm{cm}^{-2}$ according to Eq. 2.5. Additionally, using the ρ_{xx} value for $B = 0\,\mathrm{T}$ and Eq. 2.4, the mobility of the charge carriers may be extracted to a value of $\mu = 1.1 \times 10^5\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$. The mobility is a measure for the scattering of electrons during their transport through the segment under test. Apart from the classical Hall effect, we observe plateaus in ρ_{xy} at even filling factors indicated by the dotted lines in Fig. 3.4 and Shubnikov-de Haas (SdH) oscillations in ρ_{xx} for $B > 1\,\mathrm{T}$. These are features of a 2DEG which is

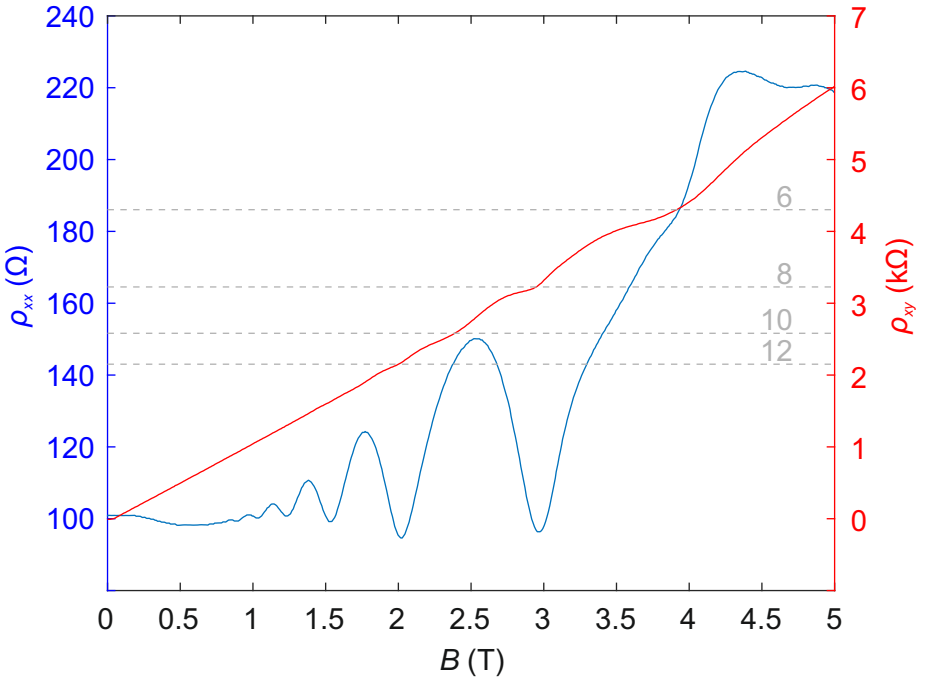

Figure 3.4. – Exemplary magnetotransport measurement on a sample with ^{28}Si QW and 20 nm of Al_2O_x (R2160A8). The longitudinal resistivity ρ_{xx}, plotted in blue as a function of the magnetic field B, shows Shubnikov-de Haas oscillations indicating a well defined 2DEG. The transverse resistivity ρ_{xy}, plotted in red as a function of B, shows a linear behaviour for low magnetic field strengths. Quantum Hall plateaus are observed for even filling factors indicating a twofold degeneracy in this measurement.

well described by the theory of the integer quantum Hall effect. The SdH oscillations allow for a separate determination of the charge carrier density, only taking into account charge carriers in the 2DEG. Due to the comparatively larger effective e^- mass, in contrast to for example the extensively studied GaAs material system, only a few SdH oscillations are observed in our samples in the accessible magnetic field range of $B < 5\,\mathrm{T}$. These few oscillations render the determination of the charge carrier density error prone. Therefore, the charge carrier densities presented in this thesis are solely extracted from the classical Hall effect.

3.3. Introduction to the gating regimes of undoped Si/SiGe

In Fig. 3.5 a the electron density n is plotted as a function of V_{ag} for a Hall bar sample produced from a piece of the wafer R2159 (^{28}Si QW, see Fig. 3.2 b). Note that three different sample positions are plotted. The legend indicates the contact numbers used for the measurements as introduced in Fig. 3.3 a. The charge carrier density rises linearly with increasing V_{ag} in the regime labeled II in Fig. 3.5 a, until the saturation regime, labeled III, is reached for $V_{ag} > 1.1\,\mathrm{V}$. The linear increase in charge carrier density in regime II is in perfect agreement with a simple plate capacitor model, with the plates being represented by the accumulation gate and the 2DEG [40, 54, 56]. Based on a previously introduced phenomenological model [40], we attribute the saturation to a charge transfer process from the QW to trap states at the semiconductor-insulator interface. As the densities for all contact pairs coincide, we conclude that the density is constant across the $4 \times 5\,\mathrm{mm}^2$ sample for a given V_{ag}. This behavior is representative for all Hall bar samples ($\sim$10) studied in the course of this thesis.

In Fig. 3.6 a-c we give a schematic representation of the conduction band structure for the three regimes proposed in the model, labeled I to III. Fig. 3.6 d shows a sketch of the charge carrier density as a function of V_{ag} with the regimes separated by the dashed lines. Fig. 3.6 a represents the starting condition for a sample cooled to 1.5 K with a cool-down voltage $V_{cd} = 0\,\mathrm{V}$ applied to the accumulation gate during cool-down. We sketch the conduction band edge as a function of the z-coordinate (growth direction of the heterostructure). The strained Si-material of the QW and the Si cap form the minima of the conduction band in the heterostructure. Since the heterostructure is undoped, there is no inherent band bending and the ground state energy for electrons in the conduction band $E_{1st\ sb}$, indicated by the dotted line in

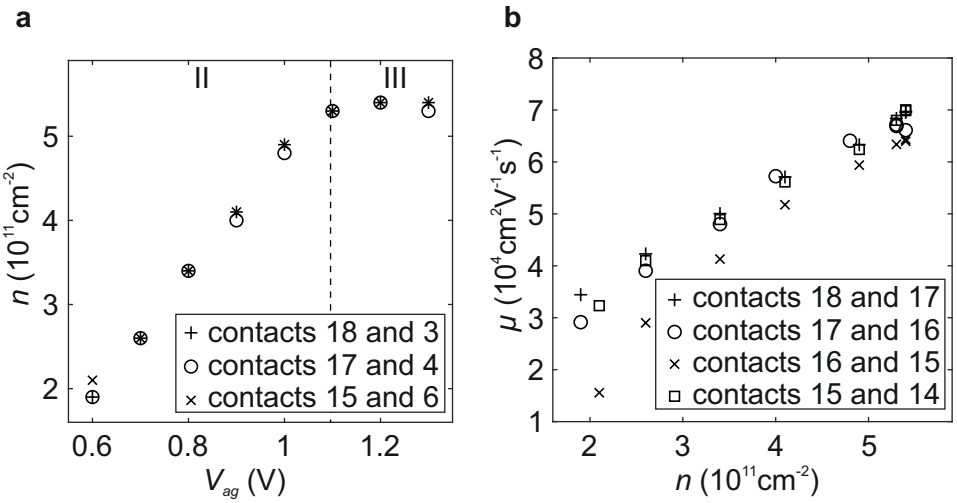

Figure 3.5. – **a** Charge carrier densities n extracted at three contact pairs via the classical Hall effect theory as a function of the accumulation gate voltage V_{ag}. A sample with ^{28}Si QW and 20 nm of Al_2O_x (R2159A4) was used for this measurement. A linear regime is observed for $V_{ag} \leq 1.1$ V where the charge carrier density in the QW may be described by a classical capacitance model (labeled II). For $V_{ag} > 1.1$ V we observe a saturation attributed to a charge reconfiguration into the semiconductor-insulator interface (labeled III). **b** Mobilities μ as a function of n calculated for four segments along the sample. The mobility rises with increasing n due to self-screening. The segment with contacts 16 and 15 shows a lower mobility compared to the other segments, which is found to be caused by an imperfection in the sample fabrication present in multiple samples.

Fig. 3.6 a, in the QW is above E_F, indicated by the dashed line. $E_{1st\ sb}$ in the thin Si cap (1-1.5 nm) lies higher than in the QW (10 nm). Considering the phenomenological model previously developed in our group [40, 54], we assume trap states to be present in the vicinity of the semiconductor-insulator interface. In our model, these states are initially filled up to E_F when cooled-down from room temperature. Raising the accumulation voltage V_{ag} decreases the potential of the accumulation gate in this picture, leading to a band bending analogous to the operation principle of a field effect transistor and lowering $E_{1st\ sb}$ in the QW with respect to E_F. We define regime I for all V_{ag} for which in the QW $E_{1st\ sb}>E_F$ and therefore with no charge carrier density accumulated in the QW. With a more positive V_{ag}, it is possible to bend the band structure in a way that $E_{1st\ sb}\leq E_F$ as sketched in Fig. 3.6 b. A non-zero charge carrier density is accumulated, with the density depending on V_{ag} as well as on the thickness and dielectric constants of the material between the QW and the accumulation gate, according to a simple parallel plate capacitor model. We define regime II for all V_{ag} where the n_{QW} shows a linear dependence on V_{ag}. In this regime, V_{ag} serves as a tuning knob for the charge carrier density in the undoped Si/SiGe heterostructures studied in this thesis.

As indicated by the arrow in Fig. 3.6 d, the metal-insulator transition (MIT) is crossed in regime II for $E_{1st\ sb}\approx E_F$. The values for the charge carrier density at the MIT observed for samples studied in this thesis in the order of $2 \times 10^{-11}\,\mathrm{cm}^{-2}$ (compare Fig. 3.5) do match quite well with the theoretical predictions of $1.6 \times 10^{-11}\,\mathrm{cm}^{-2}$ for similar undoped Si/SiGe heterostructures [57].

We observe a distinct transition from the linear regime II to a saturation of n_{QW} above a certain $V_{ag} = V_{sat}$, defined as regime III. The constant density for $V_{ag} \geq V_{sat}$ is further referred to as saturation density (n_{sat}). Based on the phenomenological model [40, 54], we attribute this saturation to a charge transfer from the QW to the interface trap states which are energetically available, as sketched in Fig. 3.6 c. The charge transfer has been found to be independent of the SiGe spacer thickness in previous results from our group where n_{sat} did not change significantly for a variation in the spacer thickness [40]. Therefore, we suspect this charge transfer process to involve Fowler-Nordheim tunneling which is dependent on the strength of the electric field present between the QW and the accumulation gate but independent on the thickness of the tunnel barrier [58–60]. One important aspect differs in our model compared to other models discussed in the literature [59, 60]: our model considers trap states, while other models incorporate a secondary conduction channel located at the semiconductor-insulator interface. The absence of a secondary conduction channel

in our structures, is motivated by findings derived from biased-cooling experiments which will be further discussed in 3.4.

In order to investigate the homogeneity of the sample, we turn towards Fig. 3.5 b which shows the mobility calculated for four different segments as a function of the charge carrier density. As expected, the mobility rises for increasing charge carrier densities due to the effect of self-screening [60–62]. One may note, that all but one segment show an identical increase. The lower mobility for the segment between the contacts 16 and 15 was traced back to an imperfection of the lithography mask, as the mobility of this segment was consistently reduced for multiple samples fabricated in the same batch [63]. We conclude that we observe an excellent homogeneity across a single Hall bar sample covering 1.5 mm of active Hall bar region.

Fig. 3.7 shows a log-log plot of the μ vs. n data of contacts 18 and 17 identical to the data shown in Fig. 3.5 b. Assuming a relation of $\mu \sim n^{\alpha}$ [62], we perform a linear regression to the experimental data and find $\alpha = 0.79 \pm 0.06$ for the whole data set with $1.9 \times 10^{11}\,\mathrm{cm}^{-2} \leq n \leq 5.4 \times 10^{11}\,\mathrm{cm}^{-2}$ with the fit plotted in blue and $\alpha = 0.89 \pm 0.09$ for the low densities: $n \leq 4 \times 10^{11}\,\mathrm{cm}^{-2}$ shown in red. Comparing these exponents with the literature [60–62], we exclude interface-roughness scattering to be the dominant scattering mechanism, as it is predicted that the mobility falls with rising charge carrier density in this case [64], which is not the trend that we observe in our samples. Since the exponents for purely background (scattering centers incorporated due to the finite background pressure during growth) and remote impurity scattering (i.e. impurities at the semiconductor oxide interface further discussed in section 3.4.2) in the strong screening regime are predicted to be $\frac{1}{2}$ and $\frac{3}{2}$ [62], respectively, it is likely that both of these mechanisms contribute to the scattering in the studied sample. As this analysis features only one data set, it would be worthwhile to extend this study to achieve better statistics.

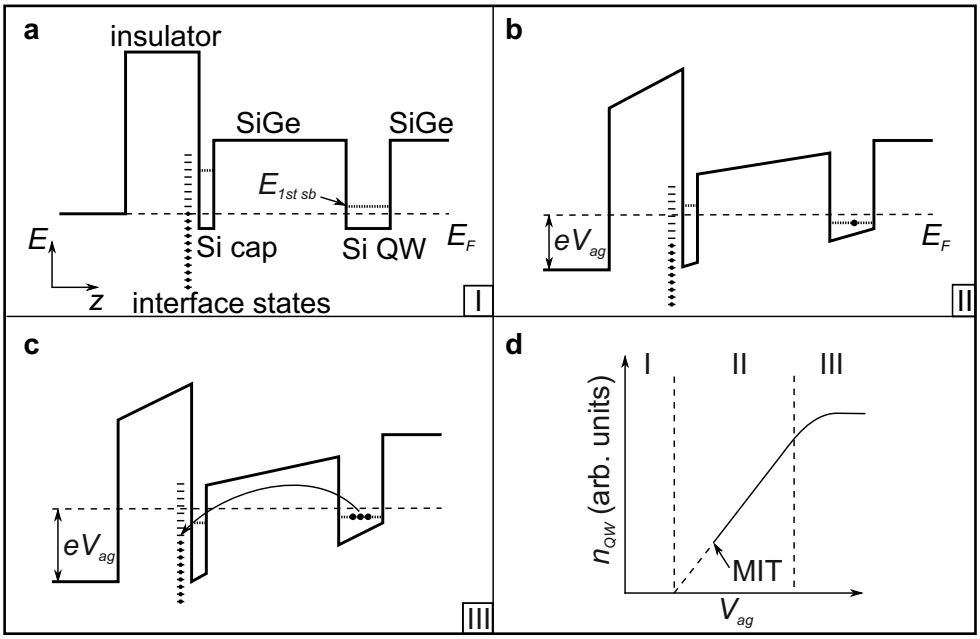

Figure 3.6. – Schematic representation of the conduction band edge energy as a function of the coordinate in growth direction z draw as a solid line. The ground state energies of electrons in the Si cap and the Si QW are indicated by the dotted lines. **a** Regime I with $E_{1st\ sb} > E_F$. **b** Regime II with $E_{1st\ sb} \leq E_F$. **c** Regime III with $E_{1st\ sb} \leq E_F$ and $V_{ag} \geq V_{sat}$. The charge transfer from the QW to the interface trap states is indicated by the arrow. **d** Sketch of n_{QW} as a function of V_{ag} with the regimes I to III separated by the dashed lines.

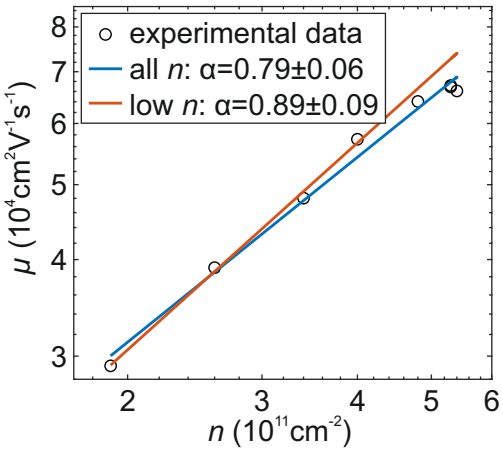

Figure 3.7. – Log-log plot of mobility μ as a function of the charge carrier density n. The data points are identical to the segment with contacts 18 and 17 in Fig. 3.5 b. A linear regression to the experimental data yields $\alpha = 0.79 \pm 0.06$ for the whole data set with $1.9 \times 10^{11}\,\mathrm{cm}^{-2} \leq n \leq 5.4 \times 10^{11}\,\mathrm{cm}^{-2}$ (blue line) and $\alpha = 0.89 \pm 0.09$ for $n \leq 4 \times 10^{11}\,\mathrm{cm}^{-2}$ (red line).

3.4. Biased cool-down

In contrast to a standard cool-down of the sample to a temperature of 1.5 K using a voltage $V_{cd} = 0\,\mathrm{V}$ applied to the accumulation gate, we may get more insight into the characteristics of the trap states suspected to be present at the semiconductor-insulator interface by examining non-zero cool-down voltages V_{cd}. Applying non-zero V_{ag} at room temperature induces internal electric fields in the structure which should influence the population of possible charge traps before cool-down.

3.4.1. Shift of the threshold voltage and density

In Fig. 3.8 a, we plot the increasing current through the sample as a function of V_{ag} applied at 1.5 K after cool-downs with a variety of cool-down voltages V_{cd} indicated in the legend. V_{thr} is defined as the voltage where $I(V_{ag}) = 1\,\mathrm{nA}$. We observe a shift in the threshold voltage V_{thr} as a function of V_{cd} in the form of a significant x-axis offset of the measured curves. Apart from the shift in V_{thr}, we observe a typical accumulation curve, as the one previously discussed in Fig. 3.3 b, for most of the tested V_{cd}. Only towards the two largest V_{cd}, we see a deviation from the typical behavior: for $V_{cd} = 0.4\,\mathrm{V}$ the undershoot feature is not present, while for $V_{cd} = 0.6\,\mathrm{V}$ we detect a significant current flowing through the sample even without increasing V_{ag} for $V_{ag} = V_{cd}$.

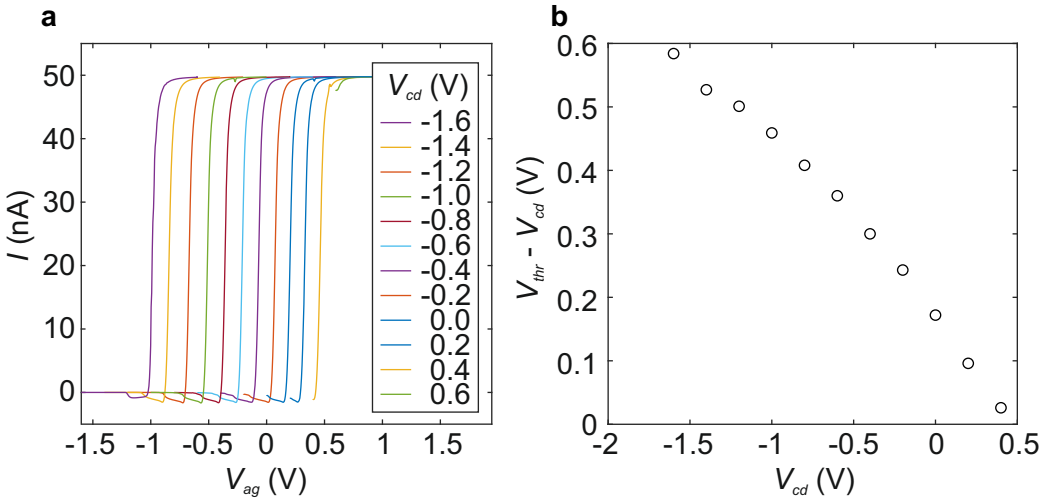

Figure 3.8. – **a** Current I through the Hall bar sample (R2138B3) as a function of the accumulation gate voltage V_{ag} for cool-down voltages $-1.6\,\mathrm{V} \leq V_{cd} \leq 0.6\,\mathrm{V}$ indicated in the legend. **b** Difference of threshold voltage and cool-down voltage $V_{thr} - V_{cd}$ as a function of V_{cd} for the data shown in **a**. V_{thr} is the voltage where the current through the sample $I = 1\,\mathrm{nA}$.

This shift of V_{thr} is consistent with the hypothesis of V_{cd}-dependent change in the charge configuration of trap states at the semiconductor-oxide interface [40, 56]. The V_{cd} applied to the accumulation gate while the device is cooled to a temperature of 1.5 K sets the interface state occupation for the cool-down, with more negative (positive) V_{cd} leading to a decrease (increase) in the negative charge at the interface. The interface charge configuration stays constant for V_{ag} variations at 1.5 K, unless the saturation regime III, introduced in section 3.3, is reached. This leads us to the conclusion, that indeed trap states are involved in the mechanism shifting V_{thr}, since the trap states are expected to stay at a constant charge configuration for moderate V_{ag} keeping the system in regimes I and II. In contrast, a secondary conduction channel could be loaded with charge in a similar way for positive V_{cd}, but we would not expect that the charge in a secondary conduction channel would stay constant, as we observed in the biased cool-down experiments. Additionally, it is hard to imagine why a negative V_{cd} should induce a V_{thr} shift involving a secondary conduction channel as the negative voltage should deplete the channel in this case.

Fig. 3.9 shows a schematic representation of the conduction band edge energy with respect to the growth direction for three regimes of V_{cd}, reflecting our current understanding of the biased cool-down behaviour. The standard cool-down with $V_{cd} = 0\,\mathrm{V}$

is depicted in Fig. 3.9 a, while Fig. 3.9 b (c) shows the positively (negatively) biased cool-down cases where the interface trap state occupation is increased (decreased) in comparison to Fig. 3.9 a.

Fig. 3.8 b shows the difference between V_{cd} and V_{thr} as a function of V_{cd} evaluated for the measurements shown in Fig. 3.8 a. Note that we have excluded the data point for $V_{cd} = 0.6\,\mathrm{V}$ as the threshold current of 1 nA has already been surpassed at $V_{ag} = V_{cd}$ for this cool-down voltage. There is a linear regime at $V_{cd} \approx 0\,\mathrm{V}$ while $V_{thr} - V_{cd}$ starts to saturate towards more negative V_{cd}. The shift of V_{thr} with varying V_{cd} is attributed to the compensation of the electric field induced by the accumulation gate through an increased (decreased) density of negative charges at the interface for positive (negative) V_{cd} [40].

Therefore, we may use $V_{thr} - V_{cd}$ as a measure for the amount of band bending that is required to induce charge carriers in the QW by increasing V_{ag}. We expect this measure to depend on the amount of negative charge trapped at the semiconductor-insulator interface, with a larger (smaller) $V_{thr} - V_{cd}$ corresponding to more (less) negative charges in the interface trap states. The mostly linear dependence of $V_{thr} - V_{cd}$ on V_{cd} with a larger $V_{thr} - V_{cd}$ for more negative V_{cd} may be explained by an increase in the density of interface trap states loaded at negative V_{cd} compared to the density at more positive V_{cd}. More data for an even broader range of V_{cd} would be beneficial in order to gain insight about the density of the trap states in a larger range of accessible energies. The observed shift in V_{thr} for all tested V_{cd} leads us to the conclusion that trap states are present over the entire probed energy range. If the density of trap states would be zero for an energy range accessible by tilting the band structure at room temperature, we would expect to see a saturation in V_{thr} with respect to V_{cd}.

Fig. 3.10 a shows the charge carrier density for several V_{cd} as a function of V_{ag}. As expected, for each of the curves, the density first increases linearly with increasing V_{ag} as described by a simple plate capacitor model. For several V_{cd}, we observe a saturation of the density, denoted regime III in section 3.3. One may note that the charge carrier density obtained at a specific V_{ag} depends strongly on the chosen cool-down voltage. This effect is explained by a different interface charge occupation for every distinct V_{cd} leading to a constant electric field influencing the number of charge carriers induced in the QW. One may use this behaviour to engineer a desired charge carrier density at a specified V_{ag} by varying V_{cd} accordingly.

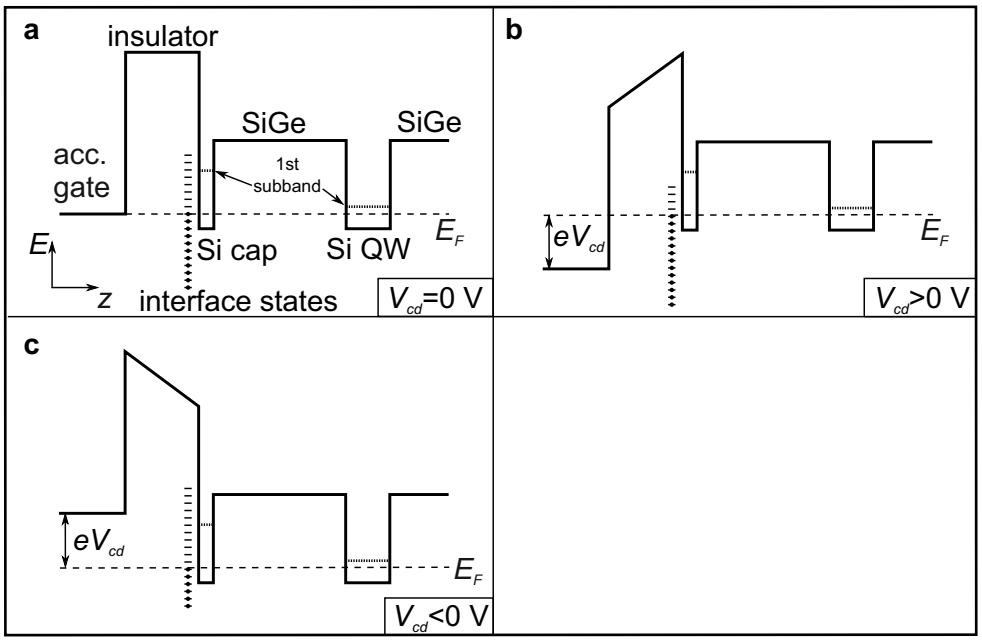

Figure 3.9. – Schematic illustration of the conduction band edge energy as a function of the coordinate in growth direction z for a variation in V_{cd}. **a** $V_{cd} = 0\,\mathrm{V}$ with a flat conduction band edge **b** $V_{cd} > 0\,\mathrm{V}$ with an increase in interface state occupation compensating for the positive V_{cd}. **c** $V_{cd} < 0\,\mathrm{V}$ with a decrease in interface state occupation compensating for the negative V_{cd}.

3.4.2. Effect of biased cool-down on the mobility

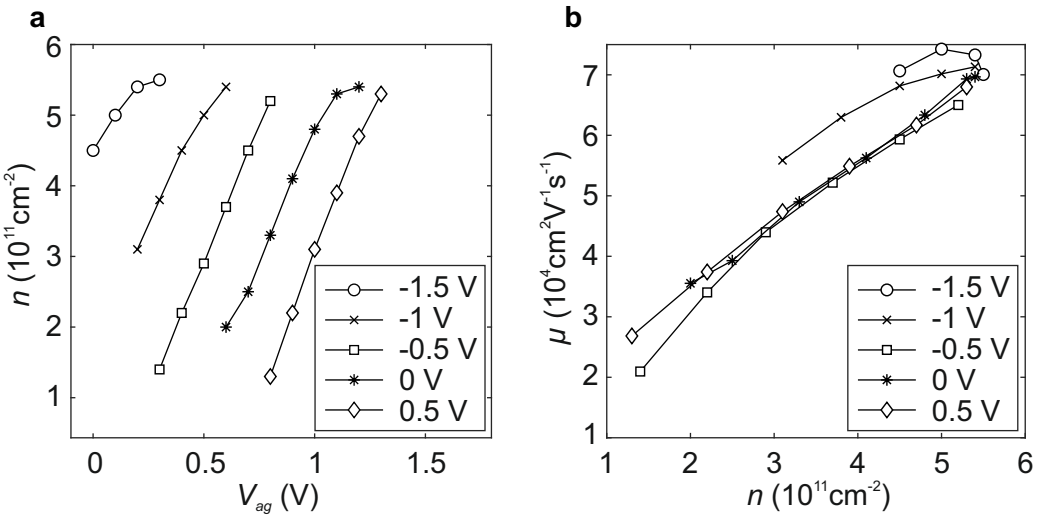

Figure 3.10. – **a** Charge carrier density n as a function of the accumulation gate voltage V_{ag} for $-1.5\,\mathrm{V} \leq V_{cd} \leq 0.5\,\mathrm{V}$ measured at the contacts 17 and 4 (R2159A4). **b** Mobility μ as a function of n for $-1.5\,\mathrm{V} \leq V_{cd} \leq 0.5\,\mathrm{V}$ measured at the contacts 17 and 16 in the same measurement run as shown in **a**. The lines in between the data points are provided as guides to the eye.

As we attribute the shift in the threshold voltage and the charge carrier densities to a change in the interface state occupation, one might think that the choice of V_{cd} could have an influence on the mobility of charge carriers as the scattering centers could be either reduced or enhanced by a change in the occupation of interface states. Fig. 3.10 b shows the mobility μ as a function of the charge carrier density n for V_{cd} in the range of $-1.5\,\mathrm{V} \leq V_{cd} \leq 0.5\,\mathrm{V}$. For all V_{cd} the general trend matches the typical behaviour with an increasing mobility for an increasing charge carrier density due to the self-screening of the charge carriers. We observe similar curves for $-0.5\,\mathrm{V} \leq V_{cd} \leq 0.5\,\mathrm{V}$ with a maximum mobility $\mu \sim 6.5 \times 10^4\,\mathrm{cm^2 V^{-1} s^{-1}}$ at a density of $n > 5 \times 10^{11}\,\mathrm{cm^{-2}}$. In contrast, the curves with $V_{cd} = -1.5\,\mathrm{V}$ and $V_{cd} = -1\,\mathrm{V}$ do show a slightly enhanced mobility at comparable densities. A lower cool-down voltage is associated with a decrease in the number of electrons in the interface trap states after cool-down. This leads us to the conclusion that a decrease in the trap state occupation induced by negative V_{cd} increases the electron mobility, likely caused by the reduced number of remote impurity scattering centers in the form of charged interface trap states. Note that in the measurement runs with

$V_{cd} = -1.5\,\mathrm{V}$ and $V_{cd} = -1\,\mathrm{V}$ showing the highest mobility, the metal-insulator transition occurs at larger charge carrier densities than the rest of the tested V_{cd}.

3.5. Illumination

The illumination of Si/SiGe samples at low temperatures was previously reported for doped systems with Pd-Schottky gates which were insulating prior to the illumination [65]. It was suspected, that the illumination alters the saturation of Si dangling bonds and the E_F pinning at the Pd-Si interface. Recently, undoped Si/SiGe heterostructures have been reported to require illumination at cryogenic temperatures in order to measure a significant current through a Coulomb-blockade device [66]. It is still unclear why this illumination does help in making the samples conductive and therefore worth to be investigated in the following section. Furthermore, the influence of this illumination on other sample characteristics such as the mobility is not well understood at the time of the writing of this thesis. In particular, we will show that illumination may be a tool to reset the electrostatic configuration of a sample without requiring the usual thermal cycle.

The cool-down voltage was kept at 0 V for all measurements discussed in this section. The illumination was performed in the cooled-down state at $T \approx 1.5\,\mathrm{K}$, by driving a constant current I_{LED} for a defined amount of time through a red light-emitting diode (LED) mounted beside the sample. After the illumination, we performed an evaluation of the sample characteristics.

3.5.1. Resetting the charge configuration

In Fig. 3.11 the current through a Hall bar sample (R2159A4) is plotted as a function of V_{ag} for the dark sample as well as after illumination with a LED for 5 s with a current of 5 mA at $V_{illum} = V_{ag} = 0\,\mathrm{V}$ and consecutively $V_{illum} = V_{ag} = -1\,\mathrm{V}$. Colored in red, the sample shows a region with no significant current flow when V_{ag} is varied, that is no visible accumulation, for the dark measurement, up to 0.3 V. In contrast, for the measurement taken after illumination at $V_{illum} = V_{ag} = 0\,\mathrm{V}$, colored in blue, a significant current flow is now detected immediately after V_{ag} is only slightly increased from 0 V. Apart from the shifted V_{thr}, the accumulation curve is similar to a typical dark accumulation measurement (compare Fig. 3.3 b). After the up-sweep of V_{ag}, we plot the depletion curve for the sweep to $-1\,\mathrm{V}$ with the current vanishing at $V_{ag} \approx -0.4\,\mathrm{V}$. At $V_{ag} = -1\,\mathrm{V}$, in depletion, we performed another illumination with the same parameters as above. Again, as shown by the orange

curve, the current set in right after V_{ag} was increased from $V_{illum} = V_{ag} = -1\,\mathrm{V}$. Without illumination, no current was detectable up to beyond $V_{ag} = -0.4\,\mathrm{V}$ which is the threshold observed in the down-sweep of the blue curve. This experimental behavior indicates that the illumination process alters the electrostatic configuration in the sample in such a way that current is then measured for any small increase in V_{ag}, independently of the value V_{illum} at which the illumination is carried out. This leads us to the assumption, that under these conditions, $E_{1st\ sb}$ of the QW matches E_F, so that a small increase in the band bending via the field effect induced by the accumulation gate always allows a significant current flow, with a charge carrier density above the MIT. The behavior discussed above was observed in a subset of the samples characterized after illumination. Table 3.1 shows the accumulation behavior for the samples tested in the course of this thesis. Two of the four tested samples show the behavior described above while one sample did not show any sign of a shifted V_{thr} after illumination and one did show a shift to larger V_{thr}. We will further discuss our understanding of the mechanism underlying the illumination of Si/SiGe samples in the following section.

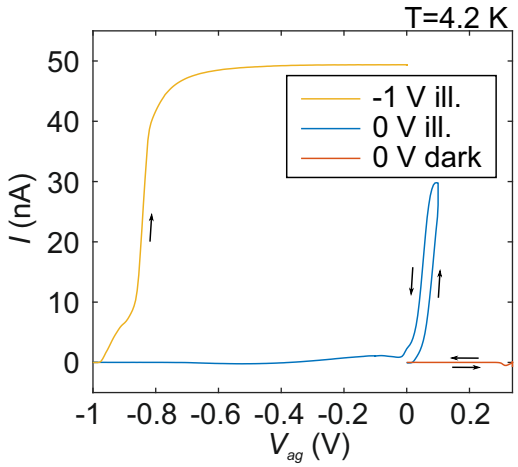

Figure 3.11. – Current I through the Hall bar sample (R2159A4) as a function of the accumulation gate voltage V_{ag} after a cool-down at $V_{cd} = 0\,\mathrm{V}$ for the following sequence: (Red) Sweep V_{ag} to 0.3 V, sweep V_{ag} back to 0 V. (Blue) Illuminate with red LED at $I_{LED} = 5\,\mathrm{mA}$ for 5 s, sweep V_{ag} to 0.1 V, sweep V_{ag} down to $-1\,\mathrm{V}$. (Orange) Illuminate with red LED at $I_{LED} = 5\,\mathrm{mA}$ for 5 s, sweep V_{ag} to 0 V.

Sample	d_{QW}	d_{spacer}	$d_{Al_2O_3}$	V_{thr} shift
R2159A4	12 nm ^{28}Si	45 nm	20 nm	$V_{thr} \approx V_{illum}$
R2160A5MIV	12 nm ^{28}Si	45 nm	100 nm	$V_{thr} \approx V_{illum}$
R2159A6	12 nm ^{28}Si	45 nm	100 nm	$V_{thr} > V_{illum}$
R2138B3	12 nm Si	35 nm	20 nm	V_{thr} const.

Table 3.1. – V_{thr} shift behaviour after illumination at $V_{illum} = V_{ag}$. d_{QW}, d_{spacer} and $d_{Al_2O_3}$ are the thicknesses of the QW, the SiGe spacer layer and the Al_2O_3 gate dielectric, respectively. The sample R2160A5MIV is a QD device presented in chapter 7.

3.5.2. Illumination model of undoped Si/SiGe

We propose a model for the illumination process in the following. We start from a flat band structure after a cool-down of the sample with $V_{cd} = 0\,\mathrm{V}$ as illustrated in Fig. 3.12 a. As in section 3.4, we assume charge trap states to be present at the interface of the semiconductor (Si cap) to the insulator (SiO_x/Al_2O_3) across the whole band gap. In this model the accumulation gate represents a comparatively large e^- reservoir.

When the LED is turned on, photons with an energy sufficient to excite electrons from the charge traps are emitted towards the sample, as depicted in Fig. 3.12 b. In our model, the electrons excited by the incoming photons are able to tunnel into the reservoir provided by the accumulation gate. As a consequence, a more positive charge is created at the semiconductor-insulator interface compared to before illumination due to the decrease in electrons occupying the charge traps.

This more positive charge translates into bending the band structure in such a way, that $E_{1st\ sb}$ of the QW crosses E_F, as shown in Fig. 3.12 b. Consequently, electrons are accumulated into the QW during the illumination. In Fig. 3.12 b, we indicate photon excitation (dotted arrows), tunnel paths (solid arrows) and relaxation of electrons (dashed arrows). We expect three tunnel processes to govern the equilibrium state and n_{QW} during the illumination process: First, the tunneling of electrons from the interface charge traps into the accumulation gate reservoir (labeled I in Fig. 3.12 b) and second, the tunneling of electrons from the interface trap states into the QW (labeled II in Fig. 3.12 b), both increasing the band bending in real space. And third, as a counterpart, the tunneling of electrons from the QW back into the trap states at the interface (labeled III in Fig. 3.12 b), which decreases the band bending.

Based on these assumptions we expect an equilibrium when the rates of the first two processes get equivalent to the rate of the third process, leading to an equilibrated interface charge and therefore a constant band bending. This band bending is found to be persistent after the LED is turned off. This observation is expected, since the charges bound in the trap states were found to be localized for low temperatures in previous work in our group [40, 54, 56], leading to a constant charge in the trap states unless the sample is either illuminated or warmed-up significantly. As described in section 3.3, in our current understanding, the trap states occupation may also be increased by a more positive V_{ag} driving the system into the saturation regime.

Fig. 3.12 c illustrates a situation where the band bending induced by the depletion of interface trap states is large enough for the Si cap electron ground state energy to be below E_F allowing the occupation of electrons in the Si cap during and after the illumination process. We will elaborate on this regime in the following section.

In some of the tested samples we observe a characteristic behavior, with immediate current flow when increasing V_{ag} after the illumination (see Tab. 3.1). We propose that the rate of tunneling from the QW to the interface trap states (process III in Fig. 3.12 b) rapidly increases as soon as $E_{1st\ sb}$ in the QW moves below the E_F. This can lead to an equilibrium state during the illumination where n_{QW} is kept below the MIT. The state of equilibrium is motivated as follows: For less electrons in the interface traps, a larger band bending is expected. This leads to an increased n_{QW}, which in turn increases the rate of the charge transfer process III in Fig. 3.12 b. This increases the number of electrons in the interface trap states reducing the band bending. When the LED is turned off and V_{ag} is raised slightly, the MIT is crossed and we measure a significant current flowing through the sample.

In the framework of the model proposed above, the voltage applied to the accumulation gate is compensated during the illumination process in the form of a change in the interface trap occupation. For example, after a cool-down with $V_{cd} = 0\,\mathrm{V}$, applying a negative $V_{ag} < 0\,\mathrm{V}$, prior to illumination, moves some of the occupied interface trap states above E_F due to band bending. When the illumination is turned on, these occupied states would get depopulated by process I in Fig. 3.12 b. This leads to the same equilibrium state as for $V_{ag} = 0\,\mathrm{V}$, after illumination. Setting V_{ag} slightly more positive induces a significant current regardless of the voltage applied to the gate during illumination as shown in Fig. 3.11.

As the tunneling processes described above depend on heterostructure characteristics such as the magnitude of the barrier potential as well as the thickness of the SiGe spacer layer, we expect to observe different equilibrium conditions for

heterostructures with a different $Si_{1-x}Ge_x$ composition (which influences the magnitude of the barrier potential) and a different SiGe spacer thickness. Furthermore, altering the illumination intensity may have an influence on the equilibrium condition, as we expect the tunnel rates to depend on the rate of incoming photons at the semiconductor-insulator interface and the QW. Indeed, we have tested samples which did not exhibit a V_{thr} shift induced by illumination (see Tab. 3.1). One tested sample, with a 100 nm Al_2O_3 gate dielectric, showed a shift to more positive V_{thr} compared to the shift to more negative V_{thr} shown in Fig. 3.11 [63]. As we have only performed a few measurements here, a more systematic study testing the characteristics of a wider variety of Si/SiGe heterostructures after illumination could help to confirm the proposed model and build a more statistically significant evidence. We suggest to systematically vary the SiGe alloy composition, the SiGe spacer thickness, the intensity of illumination controlled by I_{LED} and the illumination time in order to further solidify our understanding of the illumination mechanism. In the following section we investigate the impact of the illumination process on the charge carrier mobility in order to perform a first test of the illumination model.

3.5.3. Effect of illumination on mobility

We turn towards the effect of illumination on the mobility of a Hall bar sample, with the intention to examine scattering in a Si/SiGe sample after the illumination process and test the model proposed in the previous section. Fig. 3.13 a shows the mobility μ of the Hall bar sample (R2159A6) as a function of the charge carrier density n for several illumination intensities given by the current through the LED I_{LED} indicated in the figure legend. The sample is illuminated at $V_{illum} = 0\,\mathrm{V}$. A large I_{LED} is expected to yield a large illumination intensity. As for all μ vs. n graphs shown in this chapter, the general trend of an increasing μ for increasing n is also reflected in these measurements. Comparing the measurements taken after illumination to the dark measurement, there is a significant reduction in mobility for all tested illumination intensities over the whole accessible range of charge carrier densities n. Furthermore, the measurement taken with the lowest $I_{LED} = 500\,\mathrm{nA}$ yields a higher mobility than the larger $I_{LED} \geq 5\,\mu\mathrm{A}$ across the range of accessible charge carrier densities. Comparing the measurement after illumination with $I_{LED} = 2\,\mathrm{mA}$ to the dark measurement at $n \approx 2.5 \times 10^4\,\mathrm{cm}^{-2}$ yields a reduction of the mobility by 48 %. For $I_{LED} \geq 5\,\mu\mathrm{A}$ we do not see any significant difference between the three tested current values. This may either be due to a saturation in the LED intensity for $I_{LED} \geq 5\,\mu\mathrm{A}$ operated at 1.5 K (outside of its specification) or to a mobility

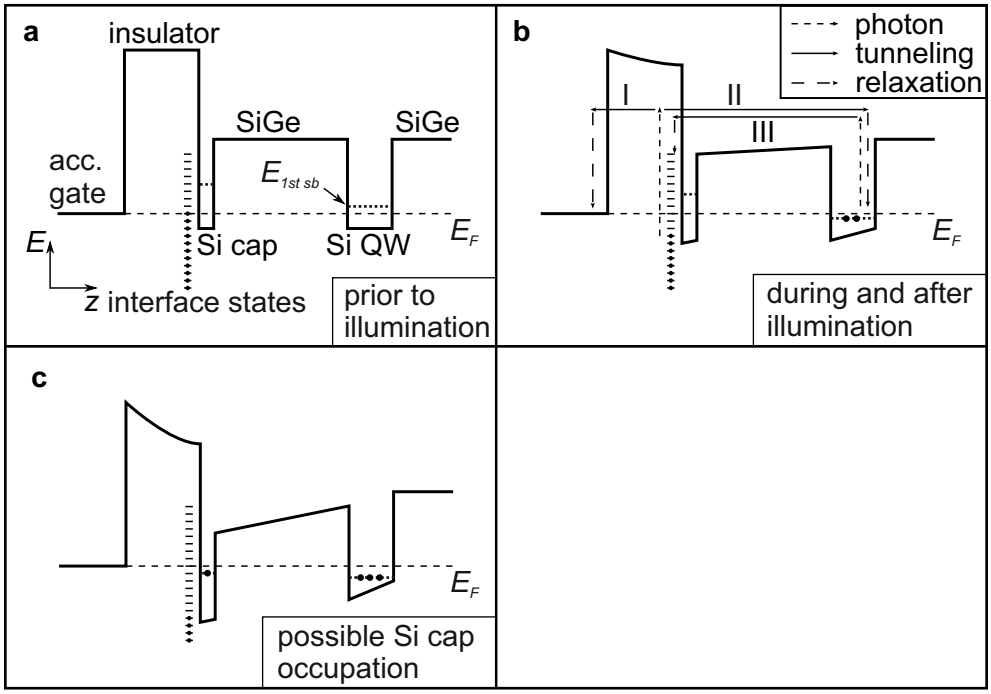

Figure 3.12. – Schematic illustration of the conduction band energy as a function of z, the growth direction of the Si/SiGe heterostructure. **a** Initial flat conduction band after cool-down with $V_{cd} = 0\,\mathrm{V}$ prior to illumination. The interface states are filled up to E_F. **b** Curved conduction band during and after illumination with LED. The transfer processes are illustrated via arrows representing photon excitation (dotted arrows), tunnel processes (solid arrows) and relaxation processes (dashed arrows). Three transfer paths are labeled with roman numerals: interface to accumulation gate (I), interface to QW (II) and QW to interface (III). **c** Illustration of the possible occupation of the Si cap ground state for a large decrease in negative charge during illumination inducing a strong band bending.

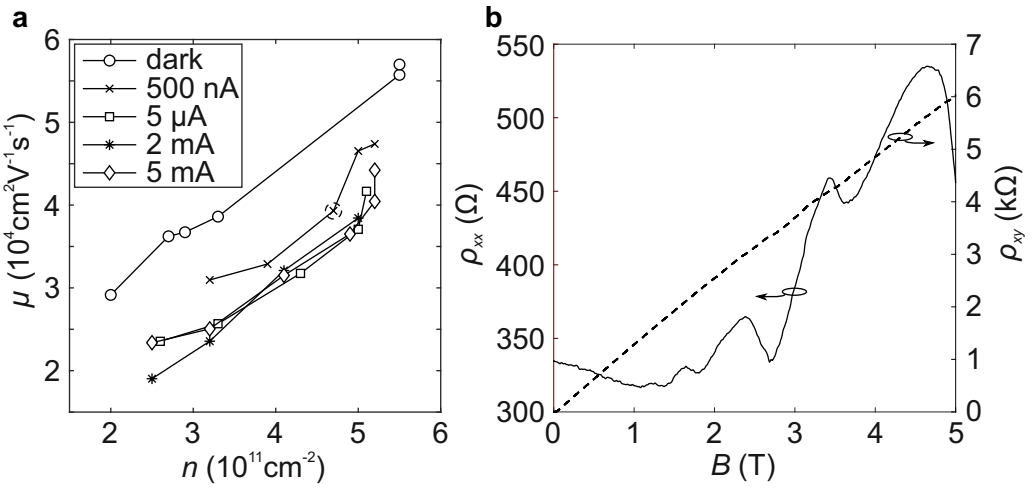

Figure 3.13. – **a** Mobility μ as a function of the charge carrier density n for the dark sample (R2159A6) and for measurements taken after an illumination with $500\,\text{nA} \leq I_{LED} \leq 5\,\text{mA}$ for 30 s. The mobility is found to be significantly reduced for the measurements after illumination. The lines in between the data points are provided as guides to the eye. **b** Hall measurement after illumination with $I_{LED} = 500\,\text{nA}$ for the circled data point in **a**. ρ_{xx} and ρ_{xy} as a function of magnetic field B and plotted with solid and dashed lines, respectively.

reducing process for larger LED intensities. This reduction in the mobility has been shown for another Hall bar sample fabricated from a different heterostructure (R2138B3) as well [63]. We find this behavior to be caused by either an introduction of additional scattering centers presumably by populating traps via the illumination in the semiconductor-insulator interface or by the formation of a second conduction channel near the Si cap of the heterostructure. As discussed in section 3.4, we attribute an increase in mobility to a decrease in the negatively charged interface trap occupation. In contrast, a decrease in mobility would be explained by an increase in the interface trap occupation, which is in conflict with the picture of the model proposed in the previous section where the trap state occupation is decreased under illumination. At the same time, Fig. 3.13 b shows the longitudinal (ρ_{xx} solid line) and Hall (ρ_{xy} dashed line) resistivity as a function of the magnetic field for the circled data point in Fig. 3.13 a with $I_{LED} = 500\,\text{nA}$. Although there are SdH oscillations visible, a strong parabolic background is present in ρ_{xx}. This combined with the slight S-shape visible in ρ_{xy}, is an indication of a secondary conduction channel. This can be explained in the framework of the model described in the previous section: a strong decrease in electron occupation would lead to a large band bending with not

only the Si QW but also the Si cap ground state energy being smaller than E_F, as illustrated in Fig. 3.12 c, leading to an electron occupation in the Si cap. We thus conclude that the observed mobility decrease is due to occupation of the Si cap.

As a secondary conduction channel does impede later qubit operation by reducing the capacitive coupling of the metal gates to a QD formed in the QW layer illumination should be used with care in Si/SiGe qubit devices.

3.6. Conclusion

In this chapter, we have shown that parameters such as the charge carrier density and the mobility are homogeneous on the scale of a few mm for our MBE-grown heterostructures. Furthermore, we have found elements which confirm a previously developed interface trap state model and underline its important role in the gate operation of undoped QWs. By performing a detailed biased cool-down study, we give further insight on the density of interface trap states: We did not observe any sign of a saturation in the threshold voltage shift, which lets us conclude that interface trap states are energetically available over the entire probed cool-down voltage V_{cd} parameter space. For a deeper understanding of the interface trap density of states, we suggest extending the V_{cd} range even further in future experiments. We also evaluated the influence of a biased cool-down on the electron mobility. While the mobility stayed constant for most of the tested V_{cd}, for large negative V_{cd}, we observed a slight enhancement of the mobility, hinting towards a reduction of scattering centers due to a lower interface trap state occupation.

In the context of the illumination of Si/SiGe heterostructures, we expanded the interface trap model by the introduction of photon-assisted tunneling processes in order to account for the experimentally observed behaviour of an immediate electron accumulation after illumination, independently of the accumulation gate voltage during the illumination. For a better understanding of the illumination process we would suggest to examine the dependence of the illumination effect on the parameters controlling the proposed tunneling processes: either the SiGe spacer thickness and alloy composition (influencing the magnitude and width of the tunnel barrier) or the illumination intensity and time (changing the rate and total amount of incoming photons). In a study of the mobility dependence under illumination, we found evidence for a secondary conduction channel created after the illumination, potentially hampering the qubit control in illuminated Si/SiGe qubit devices.

4. Tuning of a single quantum dot to the last electron regime

In this chapter, we will present measurements on a DQD device, based on the MBE-grown ^{28}Si QW heterostructure R2159 shown in Fig. 3.2 b. First, the gate layout, including the optimization of the fabrication recipe, is discussed. Second, we will show the tuning and characterization of the single electron transistor (SET) used for sensing the electron occupation in the qubit region of the device. Then, we will employ the charge sensing (CS) technique in order to tune the qubit region to a single-electron SQD configuration with a tunable tunnel barrier, which is a prerequisite for the qubit measurements discussed in the following chapters.

4.1. Device layout and fabrication

4.1.1. Improvements to the gate design

Fig. 4.1 a shows the layer structure of the DQD device studied in this thesis. The 2DEG is hosted in the ^{28}Si-QW of the R2159 heterostructure already discussed in Fig. 3.2 b of chapter 3. A SEM image of the accumulation gate layer is shown in Fig. 4.1 b which is separated from the semiconductor by 100 nm of Al_2O_3 dielectric. The accumulation gate is fabricated by means of electron beam lithography (EBL). In the same way as already described in section 3.3 the accumulation gate is used to induce charge carriers in the QW. The depletion gate layer, a SEM image is shown in Fig. 4.1 c, is patterned with EBL in between the semiconductor and the accumulation gate, with 20 nm and 80 nm of Al_2O_3 dielectric insulation to the semiconductor and the accumulation gate, respectively. These gates locally deplete the underlying 2DEG as the electric field induced by the accumulation gate is screened. This local depletion creates the potential landscape required for the QDs to form in the desired locations. Additionally, the depletion gates are used to apply voltage pulses and microwave excitation during the qubit operation. The Co nanomagnet provides a magnetic field gradient required for all-electrical qubit control via EDSR.

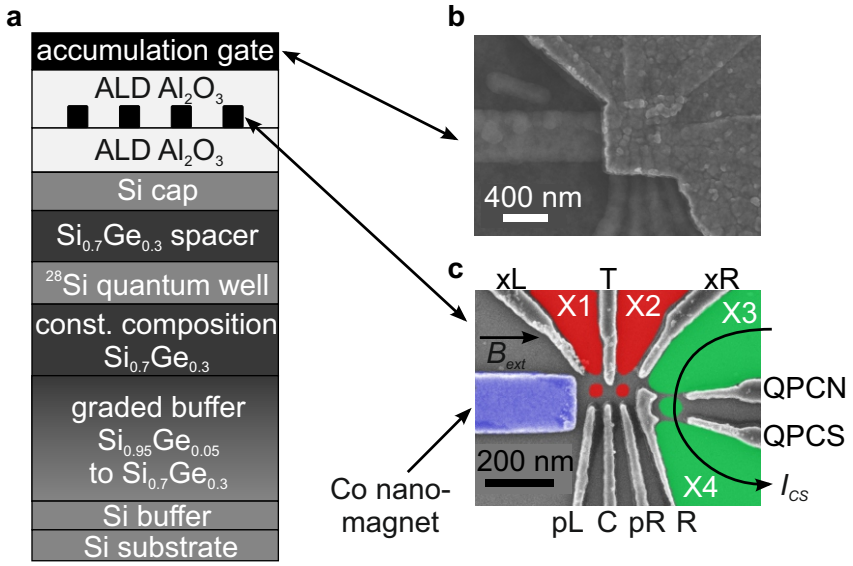

Figure 4.1. – **a** A schematic illustration of the full DQD device layer structure. Above the semiconductor heterostructure, 20 nm of Al_2O_3 gate dielectric is grown by means of ALD below the depletion gate layer, indicated by the black squares. Another 80 nm of the same dielectric insulates the depletion gate layer from the accumulation gate. **b** A scanning electron microscopy (SEM) image of the accumulation gate in a device similar to the one discussed in this chapter. **c** A false colored SEM image of the depletion gate layer in a device similar to the one discussed in this chapter. The nanomagnet is colored blue, while the electron reservoirs for the DQD and CS parts of the device are colored red and green, respectively. The current flowing through the charge sensor I_{CS} is indicated by the arrow.

Fig. 4.2 shows a SEM image of a DQD depletion gate layer with the gate layout studied in previous work in our group [47]. As in the current design the cobalt nanomagnet, colored in blue in Fig. 4.2, was added to the Ti/Au depletion gates, colored in green, which were fabricated in a separate EBL and metallization step. A weak coupling of the gates L, pL and pR in this layout has been observed and it was hard to form a well-defined QD in the charge sensing region of the device between the gates R, QPCN and QPCS [47]. This motivated the changed positions of the pL and pR gates, closer to the DQD, and the elimination of the L gate, which was not feasible to accommodate in the more closely spaced layout depicted in Fig. 4.1 c.

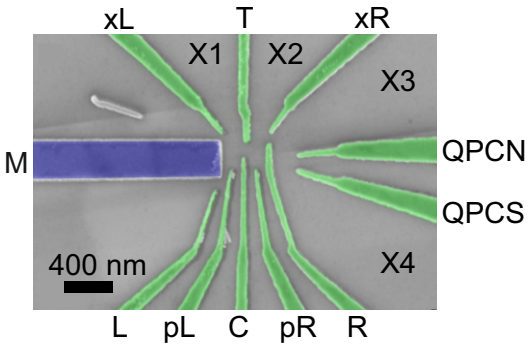

Figure 4.2. – A false colored SEM image of a depletion gate layer used in work previous to this thesis. The nanomagnet, colored blue, is placed in the same layer as all other depletion gates, colored green. The electron reservoirs are formed in the regions labeled X1 to X4. Adapted from [40].

4.1.2. Robust fabrication of the depletion gate layer

The new design of the depletion gate layer as depicted in Fig. 4.1 c is realized by means of EBL, subsequent metallization and lift-off. The electron dose chosen for the exposure of the poly(methyl methacrylate) (PMMA) does substantially affect the quality of the fabricated metal gates. Therefore, we perform a dose series in order to find the optimal dose for the new gate layout. The base dose for the optimization process is 1550 pC/cm for line elements and 800 µC/cm^2 for area elements. Fig. 4.3 shows SEM images for three different electron exposure doses, with a low (0.8 × base dose), high (1.2 × base dose) and optimal (1 × base dose) dose shown in subfigures a,b and c, respectively. Note that the nanomagnet is missing in these structures as it is added to the same layer, but in a different EBL step due to the Co material [40]. All three exposure doses produce a potentially functional

depletion gate layer which indicates a robust lithography recipe. The individual gates get thicker with increasing dose as expected. For the device studied in this and the following chapters, we chose the dose shown in Fig. 4.3 c.

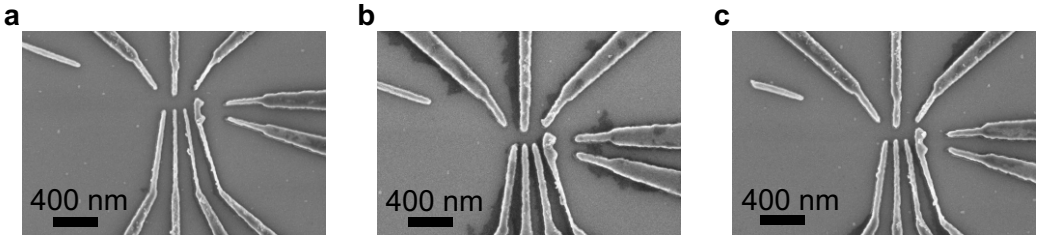

Figure 4.3. – A set of SEM images taken during the fabrication optimization process with **a** showing a low electron exposure dose, **b** showing a high dose and **c** showing the optimized dose used for the processing of the device discussed in this chapter.

4.2. Charge sensor optimization

4.2.1. Initial sensor characterization

All the electrical measurements discussed in this chapter were performed in a dilution refrigerator with a base temperature of 40 mK at RWTH Aachen. For futher details on the setup, see A.2.2. In Fig. 4.4 a we plot the current I_{CS} through the CS part of the device (colored green in Fig. 4.1 c) as a function of the voltages applied to the two gates tuning the SET tunnel barriers, V_{QPCN} and V_{QPCS}. This measurement was taken right after the accumulation of electrons into the 2DEG by increasing V_{ag} after the cool-down to 40 mK. In general both gates show a significant influence on I_{CS}, allowing the complete pinch-off of the CS part of the device, visible in the negligible current flow for the most negative V_{QPCN} and V_{QPCS} shown in Fig. 4.4 a. Additionally, we observe resonances, manifested in diagonal lines in Fig. 4.4 a, which are indications for a Coulomb blockade structure forming in the charge sensing part of our DQD device. The slope of the resonances implies a slightly stronger coupling of the QD to the gate QPCN. We observe a few oscillations with one of them being well defined. This indicates that the tunnel barriers, in this measurement controlled by QPCN and QPCS, get too opaque at about the same setting of gate voltages where a SQD starts to form. This may impact the usability of this charge sensor, as the regime with suitable working points delivering a large change in I_{CS} for a small

change in the electrostatic potential is smaller than for a well defined SQD showing many resonances. For the early stage charge sensing measurements, that will be discussed later in this chapter, no dynamical tracking of the charge sensor working point via a compensation of e.g. V_{QPCS} has been employed. During scans of the qubit dot gate parameter space, it is beneficial to have multiple Coulomb blockade peaks in order to have a multitude of sensitive charge sensor regions at hand in order to maximise the visibility of charge transitions in the qubit dot region of the device. Furthermore, in this early stage of the experiment, after the cool-down of the device, we experienced sudden jumps in the current flowing through the sensor, most likely caused by charge reconfigurations in the device. As the measurement shown in Fig. 4.4 a was taken with the most negative V_{QPCN} first, the charge reconfiguration reduced I_{CS} in this case. These charge reconfigurations have previously been observed in other accumulation mode Si/SiGe devices (see Ref. [47] and Fig. A.1) and we attribute them to initial reordering or filling of trap states mostly present up to a few days after an increase in V_{ag} was performed. This phenomenon was observed after the initial electron accumulation by raising V_{ag} from 0 V after the cool-down, as well as for changes of V_{ag} in later tuning procedures. Additionally, preceding this measurement, the voltage applied to the charge sensor gate R was adjusted as part of the tuning process from $V_R = -0.75$ V to a more positive $V_R = -0.2$ V which may also have induced the charge reconfiguration observed in Fig. 4.4 a.

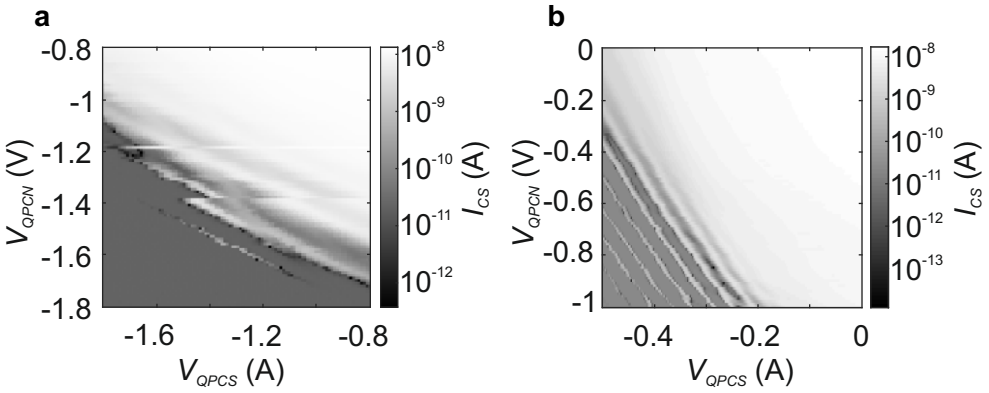

Figure 4.4. – The current through the CS part of the DQD device I_{CS} as a function of the voltages applied to the SET tunnel barrier gates QPCN and QPCS with **a** showing a configuration just after device tune-up and **b** showing a configuration after charge reconfigurations possibly induced by the tuning of gate voltages.

4.2.2. A different charge sensor configuration

Fig. 4.4 b shows the same type of measurement as plotted in Fig. 4.4 a but taken after a charge reconfiguration possibly induced by the more positive $V_R = -0.2\,\mathrm{V}$, leading to well-defined Coulomb blockade features. The occurrence of one single slope in the Coulomb peaks is attributed to the formation of a SQD with well defined tunnel barriers in the CS region of the device. As we observe a multitude of Coulomb peaks in this configuration, the SQD can be used as a charge sensor for the qubit region of the device even without a dynamical working point tracking system in place. This allows us to detect changes in the charge occupation in the qubit region down to one single electron when the sensor is in a configuration were I_{CS} is highly dependent on the electrostatic potential (see Fig. 2.7 b in Sec. 2.4.2).

As opposed to the measurement shown in Fig. 4.4 a, from the slope we see that the gate QPCS couples approximately two times stronger onto the electrochemical potential of the QD as the gate QPCN. This is an anomaly, as the two gates were intended to capacitively couple roughly in the same way onto the SET. Potentially, the retuning of V_R initiated a repositioning of the QD from lying closer to the gate QPCN, as observed in Fig. 4.4 a, to a location lying closer to the gate QPCS. In contrast, previous work in our group [40] did show an almost equal coupling of the gates QPCN and QPCS onto the SET.

4.3. Depletion to the last electron

4.3.1. Initial qubit dot region characterization

Fig. 4.5 a shows the derivative of the current through the SET as a function of the gate voltages V_{xR} and V_T. Charging lines emerge in this diagram whenever electrons are allowed to enter or leave a QD which corresponds to a change in the electrostatic potential altering the current flow through the SET. For $V_T > 0.17\,\mathrm{V}$ we observe a variety of different charging lines, indicating a complicated multi dot system in this regime. In contrast, for $V_T < 0.17\,\mathrm{V}$ we observe only two sets of parallel charging lines indicating a well-defined DQD system with the characteristic avoided crossings near the triple points (see Fig. 2.9 in Sec. 2.5). This behavior may be due to the suppression of QDs forming below the gate T, which separates the DQD region reservoirs X1 and X2 as shown in Fig. 4.1 c, as for more negative V_T the QW is expected to be locally depleted underneath the T gate. With the voltages V_{xR} and V_T more negative, in the lower left corner of Fig. 4.5 a, we do not observe any further

charging lines. This can be explained by one of the following arguments: either there are no more electrons in the system and therefore no more changes in the charge occupation are detected or the tunnel barriers get too opaque, resulting in very slow tunnel rates compared to the measurement time and therefore a reduced visibility of the charging lines or the charge sensor sensitivity is not sufficient to resolve charging lines for more negative gate voltages. In the following section we will show our way towards a configuration with only one QD in the qubit region.

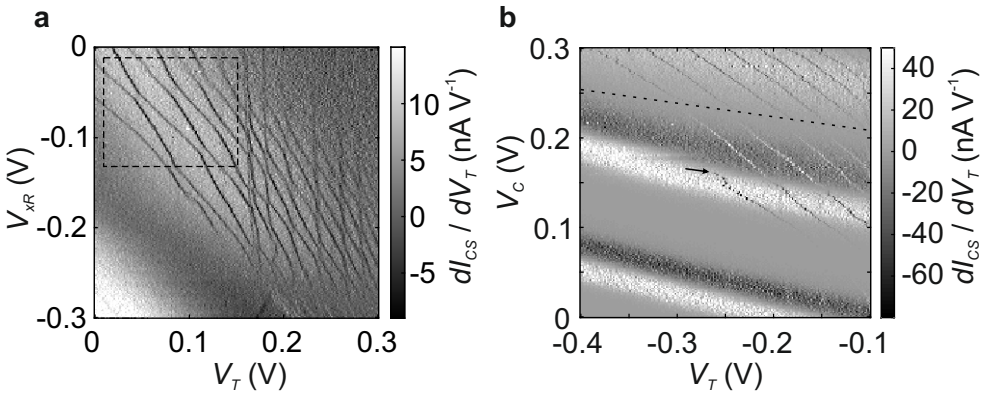

Figure 4.5. – The derivative of the current flowing through the CS part of the DQD device as a function of two gate voltages. The derivative increases the visibility of changes in I_{CS} primarily caused by a change in the electron occupation of the DQD region. **a** A broad scan of the voltages applied to the gates xR and T, revealing multiple sets of parallel charging lines. In the regime indicated by the dashed rectangle, we observe a clean coupled DQD honeycomb pattern. **b** shows a scan of the voltages applied to the gate C and T, after closing the tunnel barrier to the reservoir X2. One set of parallel lines dominates this measurement indicating the formation of a SQD. The last transition we are able to observe, marked by the arrow, shows a tunable tunnel rate to the reservoir X1 as the transition line gets blurred towards more negative V_T. There is one transition with a different slope, indicated by the dotted line, with no more transitions of the same slope detected for $V_C < 0.2\,\mathrm{V}$.

4.3.2. Suppressing unintentional quantum dots and the last electron

As already discussed in the previous section, we are able to reduce the number of observable QDs to two by setting $V_T < 0.17\,\mathrm{V}$. With the aim of a single electron occupation in a well defined SQD coupled to a single reservoir in the qubit region, we close the tunnel barrier to the reservoir X2 by driving V_{xR} to more negative values.

This measure is taken on the one hand to only have one reservoir coupled to the QDs in the qubit region and on the other hand to deplete QDs on the right side of the qubit region near the reservoir X2. The result is shown in Fig. 4.5 b where we plot the derivative of I_{CS} as a function of V_T and V_C.

Apart from one transition, indicated by the dashed line, which is primarily coupling to gate C, we observe only one set of parallel lines, indicating the formation of a SQD. For the voltage regime below the dashed line, $V_C < 0.2\,\mathrm{V}$, we do not observe any additional charge transitions parallel to the dashed line. The slope of the SQD transition lines indicates an equal coupling to the gates C and T, which hints at a SQD position with an equal distance to these gates.

We do not observe any transitions at more negative gate voltages than the last one visible in Fig. 4.5 b. The decreased tunnel coupling does not impede the visibility for additional lines and other sensor dot configurations with better visibility in the relevant regime did not show any further transition lines either. This lets us conclude that the charging line, marked by the arrow in Fig. 4.5 b, does mark the transition from zero to single electron occupation of a SQD.

The last visible charge transition, indicated by the arrow, fades out towards more negative V_T. This is expected as V_T affects the tunnel rate to the X1 reservoir. By lowering V_T we decrease the tunnel rate and the charging line gets blurred as the tunnel rate approaches the measurement timescale. This effect is used to tune the tunnel rate to the reservoir in combination with a quantification of the tunnel rate which will be discussed in the following chapter.

4.4. Conclusion

In this chapter we have introduced the depletion gate layout used for the DQD device studied in this and the following chapters. We have shown the robustness of the fabrication process for the depletion gates. We proceeded with a tuning and a characterization of the SQD charge sensor, which has proven to be essential for measurements in the low electron regime, where no transport experiment is possible in the qubit region due to opaque tunnel barriers. With the charge sensing technique in place, we have shown the tuning of the qubit dot region of the device from multiple QDs to a well-controlled mainly SQD configuration with a single electron occupation. We additionally have discussed the tunability of the tunnel barrier of the SQD to the reservoir, which is essential for performing spin-resolved pulsed gate measurements

providing access to the single spin relaxation and dephasing times which will be subject to the subsequent chapters.

5. Relaxation study on single electron spins

In this chapter, we will discuss how the spin-sensitive readout is performed in our qubit device. We will further quantify the tunneling rate from the reservoir onto the SQD and vice-versa. In order to examine the spin-relaxation in our device we will turn towards T_1 measurements over a broad range of external magnetic fields, yielding long T_1 times and an exceptionally large and robust valley splitting. All measurements discussed in this chapter have been obtained in cooperation with Arne Hollmann and Tom Struck at the RWTH Aachen with more details published in Ref. [67].

5.1. Energy selective spin readout

5.1.1. Spin-to-charge conversion

In order to distinguish the spin of the single electron occupying the QD we employ a method pioneered in GaAs QD structures which is commonly referred to as spin-to-charge conversion [68]. This method leverages the energy difference in the $|\uparrow\rangle$ and $|\downarrow\rangle$ states of an electron in an external magnetic induced by the Zeeman splitting $E_Z = g\mu_B B$ (see Sec. 2.6). This energy difference may be used to convert a spin-state into a charge state, which can be read out by charge sensing. The method is illustrated schematically in Fig. 5.1 with three distinct phases "unload", "load" and "read" separated by the dotted lines. We assume that we have formed a single e^- SQD with a tunnel coupling to one reservoir. The external magnetic field induces an energy splitting with $|\uparrow\rangle$ state lying higher in energy than $|\downarrow\rangle$ due to the positive g-factor of electrons in Si, as shown in the energy diagrams in the top row of Fig. 5.1. The voltage applied to the plunger gate capacitively coupled to the SQD, V_{pg}, as a function of time is shown on the middle row of Fig. 5.1 while the corresponding current through the charge sensor I_{CS} is depicted in the bottom row.

First, the SQD is emptied in the "unload" phase by lowering V_{pg} to a point of zero electron occupancy, where both spin-levels are above the Fermi energy of the reservoir. Any electron residing on the SQD will tunnel to the reservoir in this step, which ensures that we do not have any residual electrons on the SQD while proceeding with the protocol. In the case of an electron leaving the SQD, we expect a change in I_{CS} while no change is detected if the SQD started empty. Secondly, in the "load" phase, V_{pg} is set more positive, in order to shift both spin-levels down in energy, below the Fermi energy of the reservoir, allowing for a spin-up or spin-down electron to tunnel from the reservoir onto the SQD. In both cases a change in I_{CS} is expected when the electron enters the SQD regardless of its spin orientation. Third, in the "read" phase, we set V_{pg} to an intermediate level in order to reach a configuration where the chemical potential of the $|\uparrow\rangle$ state is above, while the potential of the $|\downarrow\rangle$ state is below the Fermi energy of the reservoir. This leads to a spin-dependent tunneling process, where only a spin-up electron can leave the SQD into the reservoir while an electron occupying the $|\downarrow\rangle$ state does not have free states in the reservoir for a successful tunneling process. This leads to a change in I_{CS} for a spin-up electron indicated by the solid line in the bottom row of Fig. 5.1. Note that the increase in I_{CS} is followed by a decrease to the previous current level induced by the filling of the SQD by a spin-down electron. This gives rise to the characteristic signal manifested in a short bump in I_{CS}. If a spin-down electron occupied the SQD at the transition of the "load" to the "read" phase, we expect no change in I_{CS} as tunneling to the reservoir is suppressed. In the following, we will discuss the current signal that is experimentally obtained in the "read" section.

5.1.2. Spin-up and -down signal

Fig. 5.2 a shows the current through the charge sensor I_{CS} of the device, colored green in Fig. 4.1 c, during the "read" phase. The device is operated at the last transition shown in Fig. 4.5 b. No bump in the current is detected, which we interpret as a spin-down event, meaning that a spin-down electron was loaded on the SQD in the beginning of the "read" phase. In contrast, Fig. 5.2 b shows the same "read" phase current window as Fig. 5.2 a, but this time with a bump in the current. We attribute this bump to a spin-up electron, which was loaded at the beginning of the "read" phase, tunneling out of the SQD into the reservoir, leading to an increase in the current. In the same manner, we attribute the decrease in current to a spin-down electron entering the SQD from the reservoir. This bump in the current is the signal which we interpret as a spin-up event, with a spin-up electron loaded on the SQD

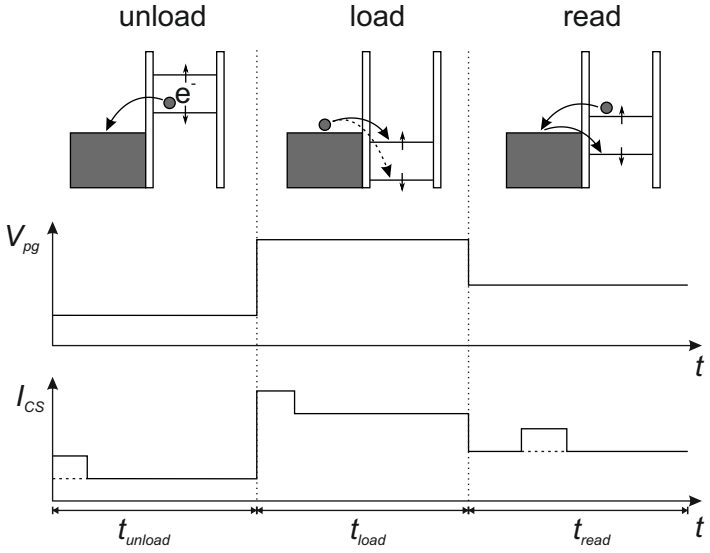

Figure 5.1. – Schematic representation of the energy diagram (top row), the plunger gate voltage $V_{pg}(t)$ (middle row) and the charge sensor current $I_{CS}(t)$ (bottom row) of a spin-to-charge conversion pulse scheme. The pulse scheme contains three phases: "unload": remove any electron residing on the QD by raising both spin levels above E_F of the reservoir (dotted I_{CS} trace: no electron on QD, solid I_{CS} trace: electron on QD), "load": lower both spin levels below E_F to load either a spin-down or a spin-up electron, "read": set $E_\uparrow > E_F > E_\downarrow$ leading to spin-dependent tunneling (dotted I_{CS} trace: spin-down electron was loaded, solid I_{CS} trace: spin-up electron was loaded, leaves the QD and is replaced by a spin-down electron)

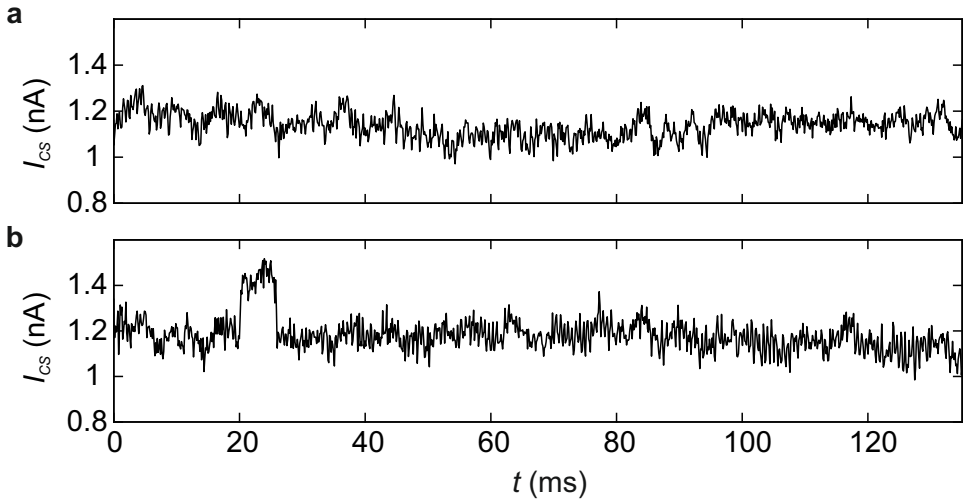

Figure 5.2. – The current through the charge sensor I_{CS} in the "read" phase of the pulse scheme presented in Fig. 5.1 as a function of the time t. **a** No bump in the current is detected. **b** A bump in the current, beginning at $t = 20\,\text{ms}$, indicates a spin-up event.

at the beginning of the "read" phase. By choosing a threshold current in the "read" phase, it is feasible to determine that a spin-up electron was loaded at the beginning of the "read" phase, when the threshold current is crossed. In practice, we preprocess the data by subtracting the mean of all the current values in the "read" phase to account for slow variations in the sensor current and applying a median filter to suppress fast current noise. After the preprocessing, a Schmitt-trigger is employed in order to digitize the data. By repetition of the pulse scheme discussed in the previous section, we are able to extract the fraction of spin-up events with respect to the total number of repetitions, which will be referred to as $P_\uparrow$ in the course of this thesis. Further details on the evaluation procedure along with a discussion of the readout errors can be found in Ref. [69]. In order to resolve a current signal as shown in Fig. 5.2 b within the measurement bandwidth, the tunneling rates between the SQD and the reservoir need to be controlled, which we will discuss in the following section.

5.1.3. Measurement of the tunnel barriers

Working at the last transition observed in Fig. 4.5 b, we turn towards a quantification of the tunneling rates to the reservoir. For the sequence presented in the previous

section, Fig. 5.3 shows the normalized I_{CS} as a function of time t averaged for multiple traces featuring a spin-up signal, as presented in Fig. 5.2 b. The beginning of the "read" phase is placed at $t = 0\,\mathrm{ms}$. As discussed in the previous section the spin-up signal consists of an increase in the current and a decrease back down to the initial I_{CS}. We observe a fast increase of I_{CS} in the first few milliseconds followed by a slow exponential decay. As the signal is composed of two tunnel processes it is well described by a double exponential

$$I_{CS}(t) = a\left(1 - \exp\left(-\frac{t}{\tau_\uparrow}\right)\right)\exp\left(-\frac{t}{\tau_\downarrow}\right) + b, \tag{5.1}$$

with $\tau_\uparrow$ being the tunneling time constant for a spin-up electron tunneling from the SQD to the reservoir and $\tau_\downarrow$ the tunneling time constant for a spin-down electron tunneling onto the SQD. Here, the factor $\left(1 - \exp\left(-\frac{t}{\tau_\uparrow}\right)\right)$ is taking into account the increase of I_{CS} due to spin-up electrons leaving the SQD, while the factor $\exp\left(-\frac{t}{\tau_\downarrow}\right)$ describes the decrease in I_{CS} as spin-down electrons enter the SQD from the reservoir. We fit Eq. 5.1 to the current signal and obtain a fit indicated by the dotted line in Fig. 5.3. From the fit we extract the tunneling times $\tau_\uparrow = (0.7 \pm 0.1)\,\mathrm{ms}$ and $\tau_\downarrow = (16 \pm 1)\,\mathrm{ms}$.

The time it takes for a spin-up electron to leave the SQD to the reservoir should be significantly lower than the readout time t_{read}, which is confirmed in this measurement. Additionally, the time for a spin-down electron to fill the empty SQD from the reservoir should not be too short as the bandwidth of the readout amplification circuit (10 kHz RC-filtered) and a post-processing filter applied in the readout evaluation process suppress short spikes in I_{CS}. The tunneling times presented in Fig. 5.3 are a result of an adjustment of the tunnel barrier by tuning the gate voltages along the last transition shown in Fig. 4.5 b with details described in Ref. [69]. In Fig. 5.3, the time $\tau_\downarrow$ is sufficiently long for the signal to be detected by the readout evaluation.

With the readout of the spin-states in place, we are able to monitor the spin-up fraction $P_\uparrow$ at the beginning of the "read" phase. This is realized by repeating pulse sequences while varying the time spent in the "load" phase in order to access the spin-relaxation time T_1 in our single e^- device. We will present the extraction of this characteristic timescale in the following section.

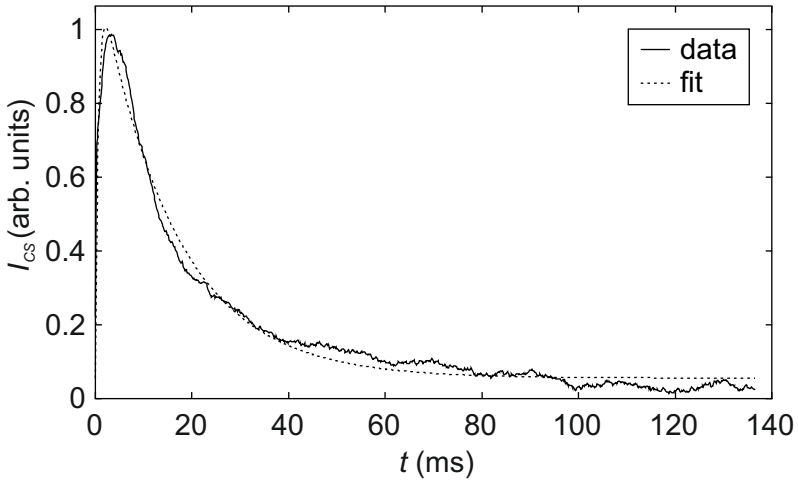

Figure 5.3. – Normalized I_{CS} averaged over multiple "read" phases where a spin-up event was detected. A fit with Eq. 5.1 yields the tunneling rates of a spin-up electron leaving the QD $\tau_\uparrow = (0.7 \pm 0.1)\,\mathrm{ms}$ and a spin-down electron entering the QD $\tau_\downarrow = (16 \pm 1)\,\mathrm{ms}$.

5.2. T_1 relaxation study

5.2.1. Load time variation yields T_1 time

In order to access the T_1 relaxation time in our spin qubit system, we vary the length of the "load" phase t_{load}. The fraction of spin-up electrons at the beginning of the "read" phase is influenced by the time we wait in the "load" phase. This is explained by the spin-up electron experiencing spin-relaxation to the energetically lower lying spin-down state during the "load" phase. Fig. 5.4 shows the measured spin-up fraction $P_\uparrow$ as a function of t_{load} for three external magnetic field values. This fraction was determined by counting the single-shot spin-up events of 3000 pulse sequences resembling the one illustrated in Fig. 5.1 for each tested t_{load} and dividing by the total number of pulse sequences. For each of the three data sets, we observe an exponential decay with a decreasing spin-up fraction $P_\uparrow$ for an increasing waiting time t_{load}. We fit the experimental data using a single exponential decay

$$P_\uparrow = a \exp\left(-\frac{t_{load}}{T_1}\right) + b. \tag{5.2}$$

The lines in Fig. 5.4 fit the experimental data very well, yielding a value for T_1 for each B_{ext}. One may note, that the value for T_1 decreases significantly from $(450 \pm 40)\,\mathrm{ms}$

to (39 ± 3) ms with increasing magnetic field from 1.6 T to 3.25 T. This shows that T_1 is highly dependent on the external magnetic field. In the following section we will explore the spin-relaxation in a broad range of B_{ext} and discuss the mechanisms influencing T_1 in our Si/SiGe QDs.

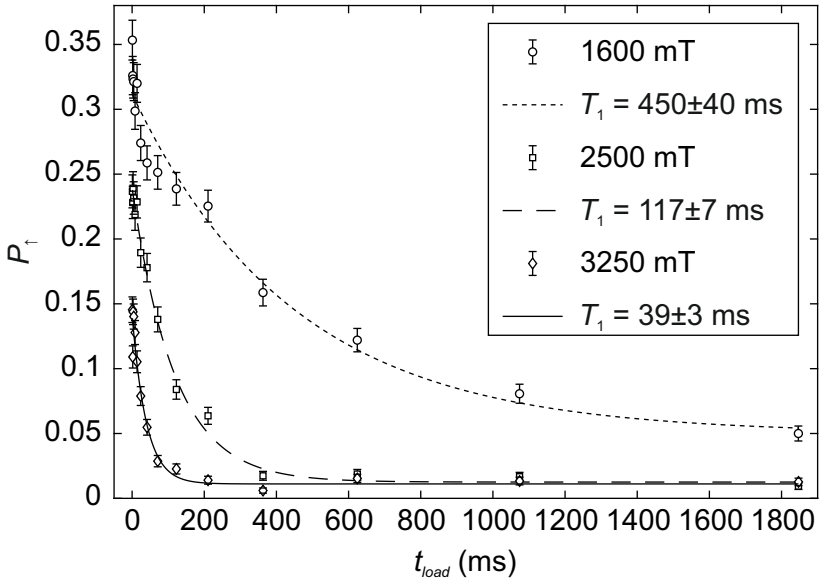

Figure 5.4. – Fraction of detected spin-up events $P_\uparrow$ as a function of the time of the "load" pulse t_{load} for three external magnetic field values indicated in the legend. Each data-point is created by evaluating 3000 single-shot measurements. The fits with Eq. 5.2, represented by the lines, match the data-points well and yield the relaxation time T_1 indicated in the legend.

5.2.2. $T_1(B)$ spectroscopy and valley hotspot

In order to gain a more detailed insight into the spin-relaxation in our device, we extend the measurements discussed in the previous section to B_{ext} between 0.3 T and 4.25 T. Fig. 5.5 shows the relaxation rate $1/T_1$ with respect to B_{ext}. We observe a low and constant relaxation rate for $B_{ext} < 1.6$ T (regime I in Fig. 5.5) with an average of (1.8 ± 0.2) Hz corresponding to an average relaxation time of (570 ± 80) ms. For $1.6\,\mathrm{T} < B_{ext} < 2\,\mathrm{T}$ (regime II in Fig. 5.5) a peak (hotspot) is detected with relaxation rates almost two orders of magnitude larger than for the low B_{ext} data. For larger $B_{ext} > 2$ T (regime III in Fig. 5.5) the data shows a monotonous increase in $1/T_1$.

The low-field regime I with the long and constant T_1 times in the order of 0.5 s offers a good working point for the qubit manipulation presented in chapter 6 as

the field range up to 1.6 T is more than sufficient for resonant driving of the qubit, which is performed at an external magnetic field of 668 mT in our qubit manipulation experiments. The long T_1 times in regime I compared to the low-field T_1 times of 160 ms in a similar single e^- device in Si/SiGe [70] can potentially be explained by the different design of our nanomagnet providing less artificial spin-orbit coupling. However, this reduced coupling can in turn reduce the driving frequency when moving to spin manipulation.

In the high-field regime III, by fitting the magnetic field dependence of possible relaxation mechanisms, we find the spin relaxation to be most likely dominated by phonon noise coupling to the spin via a mixture of artificial and intrinsic spin-orbit interaction with more details given in Ref. [67]. As mentioned before, the artificial spin-orbit interaction is a direct consequence of the magnetic field gradient induced by the nanomagnet [70].

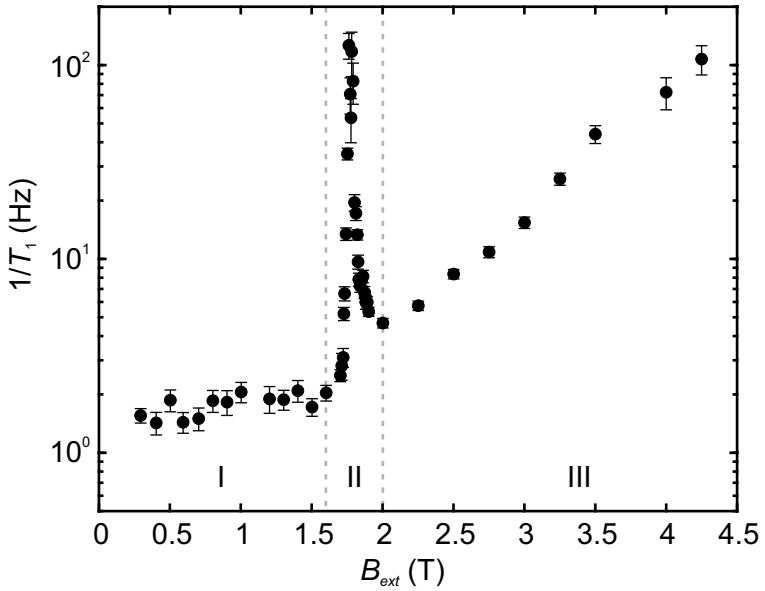

Figure 5.5. – spin-relaxation rate $1/T_1$ with respect to the external magnetic field B_{ext}. A strong increase in the relaxation rate is detected for $1.6\,\mathrm{T} < B_{ext} < 2\,\mathrm{T}$ (regime II). For $B_{ext} < 1.6\,\mathrm{T}$ the relaxation rate stays approximately constant (regime I), while for $B_{ext} > 2\,\mathrm{T}$ $1/T_1$ increases with increasing B_{ext} (regime III).

We now turn towards the regime II featuring the sharp peak in the spin-relaxation rate. As discussed in Sec. 2.2, in Si/SiGe QW structures the sixfold valley degeneracy of bulk Si is lifted by the strain of the QW resulting in a twofold ground state degeneracy. This twofold is lifted due to the out-of-plane electric field E_z and the

sharpness of the QW [50, 71–73]. This valley splitting E_{VS} is indicated in the energy diagram depicted in Fig. 5.6 as a separation of the lower and upper valley states v_- and v_+. A non-zero total magnetic field strength B introduces a Zeeman splitting $E_Z = g\mu_B B$, with the electron g-factor g and the Bohr magneton μ_B, between the spin-up and spin-down states which are degenerate for $B = 0\,\mathrm{T}$. As indicated by the dashed line in Fig. 5.6, the $|-,\uparrow\rangle$ state energetically matches with the $|+,\downarrow\rangle$ state when the condition $E_Z = E_{VS}$ is fulfilled. These two states mix, resulting in the anticrossing shown in Fig. 5.6. This spin-valley mixing leads to an enhanced spin-relaxation for B_{ext} satisfying

$$g\mu_B B \approx E_{VS} \tag{5.3}$$

$$B = B_{ext} + B_{nm}, \tag{5.4}$$

with the external magnetic field B_{ext} and the magnetic field induced by the nanomagnet B_{nm}. This explains the spin-relaxation peak we observe for $1.6\,\mathrm{T} < B_{ext} < 2\,\mathrm{T}$ in Fig. 5.5 where we assume Eq. 5.3 to be fulfilled.

Using a peak fit to the relaxation hotspot and taking into account the magnetic field of $(40.7 \pm 0.1)\,\mathrm{mT}$ introduced by the nanomagnet, we extract a valley splitting of $E_{VS} = (213.1 \pm 0.3)\,\mu\mathrm{eV}$. This method is a very precise determination of E_{VS} compared to methods such as pulsed gate spectroscopy. Relative to the valley splittings reported for Si/SiGe devices mostly below $70\,\mu\mathrm{eV}$ [28, 30, 70, 74–80] the extracted valley splitting in our device is 2 to 3 times larger. To test the robustness of the valley splitting in our device, we vary the gate voltage configuration in the following section.

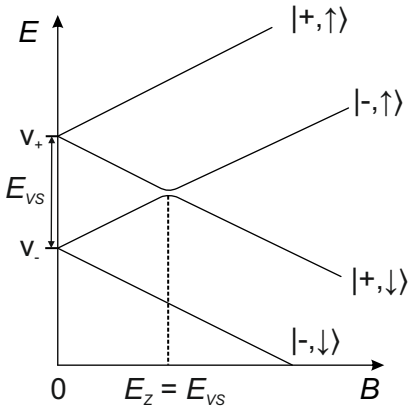

Figure 5.6. – Schematic energy level diagram of the valley- and spin-split states $|+,\uparrow\rangle, |-,\uparrow\rangle, |+,\downarrow\rangle$ and $|-,\downarrow\rangle$ as a function of the total magnetic field $B = B_{ext} + B_{nm}$. B_{nm} is the magnetic field of the nanomagnet. The states $|-,\uparrow\rangle$ and $|+,\downarrow\rangle$ show an anticrossing at $E_Z = E_{VS}$ leading to enhanced spin-relaxation due to spin-valley mixing.

5.3. Valley splitting across multiple gate voltage configurations

We set out to measure E_{VS} while the gate voltage configuration is varied in order to gain insight into the robustness of E_{VS} in our device. We adjust V_{pL} while keeping the tunnel coupling to the reservoir constant by compensating with V_T.

Fig. 5.7 shows the extracted E_{VS} for five pL and T voltage configurations. The data point for the configuration of Fig. 5.5 is marked with the arrow. We observe a monotonous shift in E_{VS} which is approximately linear in V_{pL} and V_T. The lowest E_{VS} we observe in our measurement series is $(185 \pm 4)\,\mu\text{eV}$ which is a shift of $(28 \pm 4)\,\mu\text{eV}$ or $(15 \pm 2)\,\%$ compared to the largest E_{VS}. We find the values of E_{VS} to be robust and reproducible with respect to fast changes between the voltage configurations. This large and robust E_{VS} enables a broad range of B_{ext} for spin manipulation via EDSR without a fast spin-relaxation which can be limiting qubit coherence, Pauli-spin blockade and operation at higher temperatures in Si/SiGe devices with lower E_{VS} [41]. Since our device is based on a MBE-grown ^{28}Si/SiGe heterostructure, it is possible that the solid source purity combined with the low substrate temperature of 350 °C during the QW-growth are beneficial for a sharp QW interface. This hypothesis is currently investigated by means of atom probe tomography and high resolution transmission electron microscopy (TEM).

In the following section, we will discuss self-consistent Schrödinger-Poisson simulations giving insight into another possible origin of the E_{VS} shift.

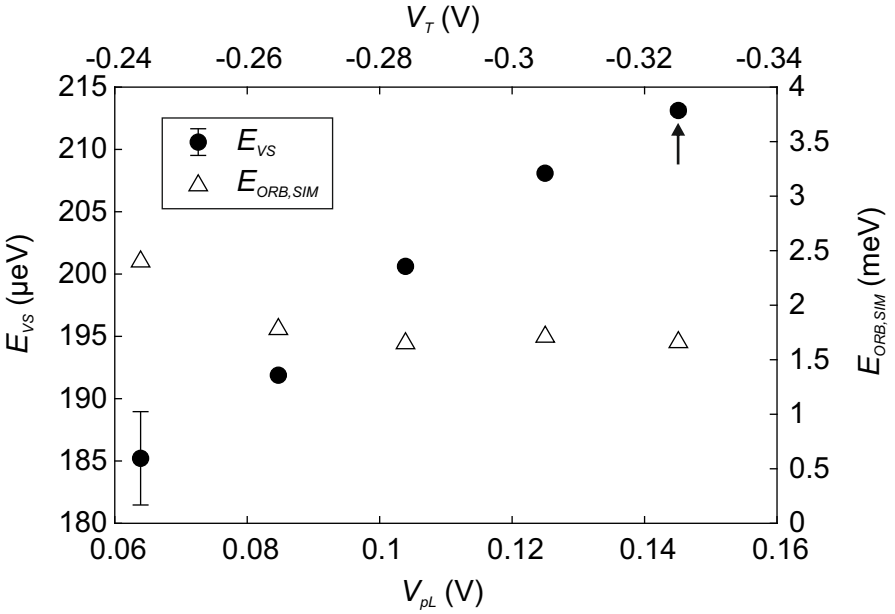

Figure 5.7. – Left y-axis: Valley splitting E_{VS} extracted via peak fits to $1/T_1$-data for five gate voltage configurations with varying V_T and V_{pL} voltages. The configuration shown in Fig. 5.5 is marked with an arrow. Right y-axis: Simulated orbital energy $E_{ORB,SIM}$ for the five experimentally applied gate voltage configurations.

5.3.1. Self-consistent Schrödinger-Poisson simulations

We set up a three dimensional self-consistent Schrödinger-Poisson simulation, using the depletion gate layout and the layer structure of the heterostructure R2159, as depicted in Fig. 3.2 b, as an input. The simulation procedure is sketched in the appendix A.3. We performed simulations for the five experimentally tested gate voltage configurations with a variation of the V_{pL} and V_T gate voltages.

Introducing a fixed charge density

In chapter 3, we discussed the presence of trap states at the semiconductor-oxide interface. In the simulations presented in this chapter, we consequently introduced a fixed charge density at this interface to account for the trap states present in the experiments. With a negative fixed charge density of $4.4 \times 10^{11}\,\mathrm{cm}^{-2}$ in the SiO_2 layer

located at the interface of the Si cap and the Al_2O_3 gate dielectric, the experimental gate voltages, which are applied in the simulation, yield a single e^- occupancy for the five simulated gate voltage configurations matching the experimental e^- occupation.

5.3.2. Orbital splitting

We find the orbital splitting to stay constant in the experiment (≈2.5 meV, see Ref. [67]) as well as in the simulation (≈1.6 meV, see the simulated orbital energies $E_{ORB,SIM}$ for the five gate voltage configurations in Fig. 5.7). Therefore, we exclude a change in the confinement potential as a cause for the variation in E_{VS}.

Electric field evaluation

The valley-splitting was found to be highly dependent on the electric field in z direction E_z [50, 72, 81, 82]. Therefore, we performed an evaluation of the out-of-plane electric field E_z in the simulations of our qubit device. Fig. 5.8 c shows E_z evaluated as a weighted average with the electron probability density used as weight. Compared to the large E_z fields reported for Si-MOS devices up to 30 MVm^{-1} [83], we find a weaker E_z around 1.3 MVm^{-1}. More importantly, we do not obtain a significant variation of E_z between the different simulated voltage configurations. This leads us to the conclusion, that it is unlikely that a change in E_z causes the experimentally measured shift in E_{VS}. Having excluded a change in the confinement potential and a variation of E_z as a likely origin for the observed shift in E_{VS}, we will find a more plausible mechanism in the following section.

Lateral displacement

From the simulations, we extract the probability $|\Psi|^2$ of an electron being found in a voxel location on the 3-dimensional simulation grid. Fig. 5.8 b shows $|\Psi|^2$ integrated over the z-coordinate as a function of the lateral x and y coordinates for $V_{pL} = 0.145$ V (top) and $V_{pL} = 0.085$ V (bottom). In this representation of the simulated electron position, we observe a shift with respect to the voltage applied to V_{pL}, as the maximum of $|\Psi|^2$ is in a different location comparing the top and bottom subfigures of Fig. 5.8 b. As the position shift is found to be mainly along the y coordinate, we plot $|\Psi|^2$ integrated over the z and x coordinates as a function of the y coordinate in Fig. 5.8 d for all five simulated (and experimentally tested) voltage configurations with the V_{pL} value indicated in the legend. Here, we see a clear shift in the electron position with respect to V_{pL}. We therefore conclude that

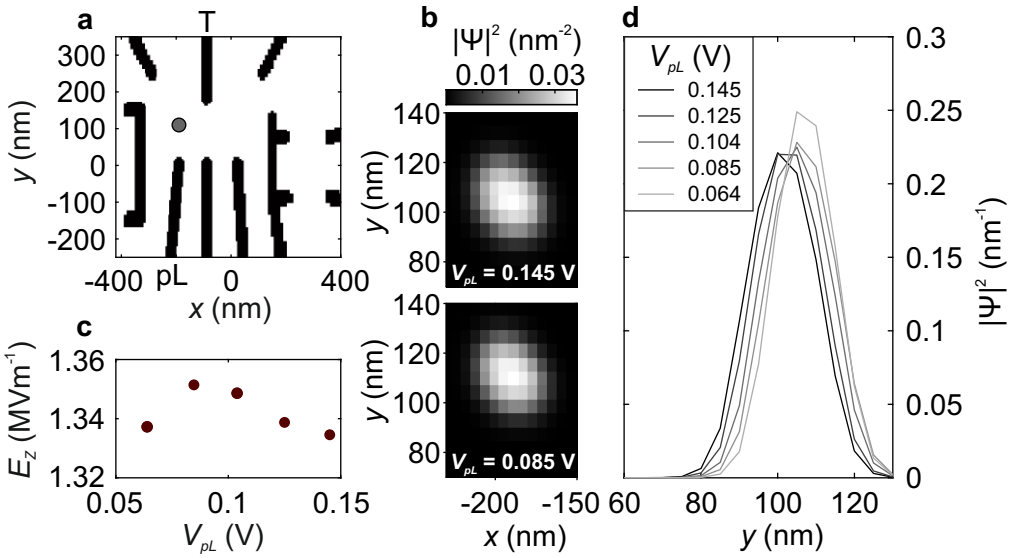

Figure 5.8. – **a** Depletion gate layer as modelled in the simulation with the depletion gates in black and the QD position indicated by the red circle. **b** Normalized $|\Psi|^2$ with respect to the simulation x and y coordinates for $V_{pL} = 0.145\,\mathrm{V}$ (top) and $V_{pL} = 0.085\,\mathrm{V}$ (bottom). **c** z-component of the electric field E_z weighted with $|\Psi|^2$ for different V_{pL}. **d** Normalized wave function probability $|\Psi|^2$ simulated for different V_{pL} with respect to the simulation y-axis. Reprinted figure with permission from [67]. Copyright 2020 by the American Physical Society.

the experimentally applied voltage configurations likely induce a lateral displacement of the electron position. We will discuss how this displacement can create a shift in E_{VS} in the following.

5.3.3. Valley splitting in proximity to a monolayer step

With the lateral displacement found in the simulation, we can think of a mechanism involving a single monolayer step in the QW interface being responsible for the E_{VS} shift. As the electron wavefunction is moved relative to such a step, the valley splitting can be reduced significantly. This is due to the fact that a monolayer step introduces a valley phase of $\theta = 2k_0 a_{Si}/4 = 0.85\pi$ with $a_{Si}/4$ being the height of a silicon monolayer and $k_0 = 0.85(2\pi/a_{Si})$ the position of the valley minimum along the Δ direction [84]. When the wavefunction comes into proximity to the step, the valley splitting is reduced from $E_{VS,\infty}$ down to $E_{VS,\infty}\cos(\theta/2)$ with $E_{VS,\infty}$ being the valley splitting without any interface step in vicinity. In Fig. 5.9 we plot the reduction in the valley splitting $E_{VS}/E_{VS,\infty}$ as a function of the wavefunction displacement with respect to a monolayer step placed at 0 nm for the case of the simulated orbital energy 1.6 meV, showing that the experimentally observed shift of 15 % in E_{VS} is plausible for a lateral displacement on the nm scale. From the data obtained in the experiment, we can not exclude the presence of multiple steps in vicinity of the electron wavefunction. We can exclude a bilayer step as the origin for the observed shift in E_{VS} as such a step would introduce a valley phase of 1.7π leading to an expected shift in E_{VS} of less than 11 %. Therefore, it is the displacement of the wavefunction relative to potentially multiple monolayer interface steps that we find most likely to be responsible for the shift of E_{VS} observed in the experiment.

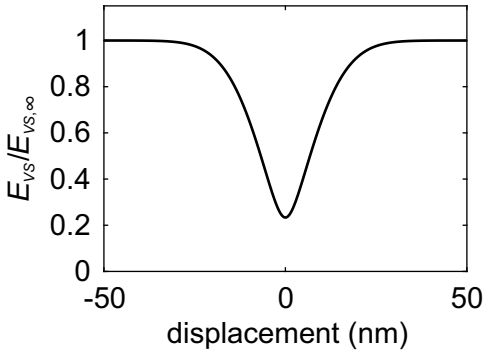

Figure 5.9. – $E_{VS}/E_{VS,\infty}$ as a function of the displacement of the electron wavefunction with respect to a monolayer step in the QW interface located at 0 nm. $E_{VS,\infty}$ represents the valley splitting far away from the interface step.

5.4. Conclusion

In this chapter, we have discussed the method of spin-to-charge conversion and accessed the rates of electrons tunneling from the reservoir onto the dot and back in order to ensure a robust readout. The $T_1(B_{ext})$ measurements showed a remarkably broad low field regime with long $T_1 > 500$ ms enabling a wide range of operating points for spin manipulation via EDSR. We extract an exceptionally large valley splitting of $E_{VS} > 200$ µs 2 to 3 times larger than the values previously reported for Si/SiGe QDs potentially induced by a sharp MBE-grown interface.

The tracking of the spin-relaxation hotspot showed a monotonous shift in E_{VS}, which we attribute to a lateral displacement with respect to monolayer steps at the QW interface. Furthermore, the robust and reproducible shift hints to a low disorder in the studied device.

More statistics as well as experiments involving atom probe tomography should bring more clarity whether the large valley splitting is a signature of our devices. A consistently large valley splitting would open a route towards elevated temperature operation of Si/SiGe qubit devices, where recently published work on Si-MOS devices has shown remarkable progress [42, 85].

The findings presented in this chapter demonstrate the first single spin characterization of the qubit platform developed at the University of Regensburg in collaboration with the RWTH Aachen.

In the following chapter, we proceed with the spin manipulation giving access to the dephasing time for quantum information stored in the electron spin degree of freedom.

6. Single spin manipulation in ^{28}Si/SiGe

In this chapter, we will explore the manipulation of the single e^- spin in the qubit device discussed in the previous chapters. We will show that the nanomagnet gradient provides a sufficiently large artificial spin-orbit coupling to demonstrate coherent driving via EDSR.

With the spin manipulation in place, we will show a preliminary characterization of the dephasing in our ^{28}Si/SiGe device. By refocusing slow noise on the measurement time scale, we will demonstrate a remarkably long coherence time in our device. Furthermore, we will give an outlook on the parameters limiting the spin coherence in our system. All measurements discussed in this chapter have been obtained in cooperation with Tom Struck and Arne Hollmann at the RWTH Aachen with more details published in Ref. [86].

6.1. Spin manipulation by electric dipole spin resonance

As depicted in Fig. 6.1, our DQD device is equipped with a cobalt nanomagnet which is placed in the same plane as the depletion gate layer. This nanomagnet is smaller compared to the micromagnets employed in devices of other groups [30, 36, 37], which leads to a single magnetic domain extending over the entire nanomagnet [40]. The nanomagnet is placed in the same plane as the metal finger gates employed for tuning the electrostatic potential and we are able to use it as an electrostatic gate by applying a voltage. Additionally, the nanomagnet adds a local magnetic field gradient which can be employed to perform all-electrical spin-manipulation via EDSR. The external magnetic field $\vec{B}_{ext}$ is oriented in-plane along the nanomagnet axis as indicated in Fig. 4.1 c. The MW pulses are applied to the gate pL enabling resonant driving via EDSR. For further details on the EDSR spin manipulation see Sec. 2.7. As discussed in chapter 5, due to the different magnet design, we see a longer T_1 time in our device compared to similar devices employing a larger magnet [70]. A possible drawback of the smaller single domain magnet is the weaker artificial spin-orbit interaction, reducing the coupling efficiency to the spin during

manipulation potentially leading to a reduced Rabi frequency in a device featuring a nanomagnet compared to devices with a micromagnet. In the following, we will explore the spin manipulation in our qubit device.

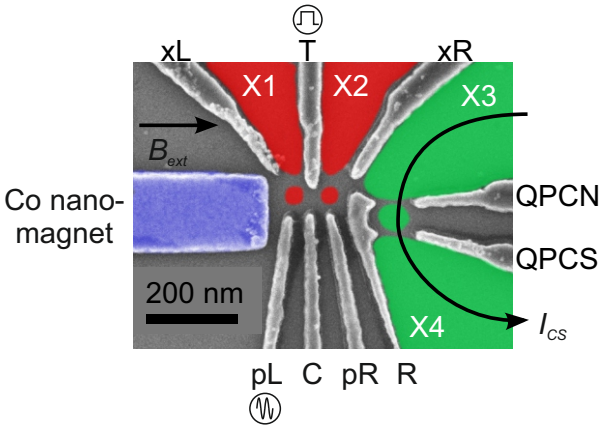

Figure 6.1. – A false-colored SEM image of the depletion gate layer of a device similar to the one discussed in this chapter. The nanomagnet is colored blue, while the reservoirs for the qubit and charge sensing parts of the device are colored red and green, respectively. The external magnetic field is oriented along the nanomagnet axis. The MW signals for spin manipulation are applied to the gate pL, while T is employed for pulses similar to the one presented in Fig. 5.1.

6.1.1. Rabi oscillation measurement

In order to show a controlled spin manipulation in our qubit device, we set out to induce Rabi oscillation via EDSR. In the SQD configuration discussed in chapter 4 we apply an external magnetic field of $B_{ext} = 668\,\mathrm{mT}$ along the nanomagnet axis (see Fig. 6.1). We find the resonance frequency by means of rapid adiabatic passage [87]. For the initialization of each experiment, the QD is loaded with an electron and we ensure that a spin-down electron is present at the beginning of the MW pulse by waiting for any spin-up electrons to relax into the $|\downarrow\rangle$ state. We then applied a MW-signal of around $f_L = 19.9\,\mathrm{GHz}$ to the gate pL, matching the Larmor-frequency at the selected magnetic field, in order to couple to the spin via EDSR and read out the spin state after the MW pulse using spin-to-charge conversion.

Fig. 6.2 shows the spin-up probability $P_\uparrow$ after the application of a MW-pulse as a function of the frequency detuning with respect to the resonance frequency f_L and the pulse duration t_{MW}, as illustrated in the inset of Fig. 6.2. We extract a

Rabi oscillation with the frequency and amplitude depending on the MW frequency detuning. With zero detuning, we observe a Rabi frequency of around 400 kHz which is quite small compared to a device with a micromagnet showing Rabi frequencies in the order of 30 MHz [36]. Although increasing the MW amplitude by a factor of ∼2.5 did increase the Rabi frequency to around 1 MHz, we did lose the spin-signal for larger MW amplitudes (compare Ref. [36]). This phenomenon can not be attributed to oscillation damping as we did not detect a roll-off of the Rabi frequency for larger MW-amplitudes. Therefore, the origin of this limitation remains a subject of ongoing experiments. The Rabi oscillations are a clear sign of coherent single-spin manipulation in our device. By adjusting t_{MW} we are able to perform deterministic rotations about one qubit axis. And through a phase shift in the MW signal introduced by quadrature control we have all-electrical all-axis control of the spin-qubit. This means that we can set $|\Psi\rangle$ to any point on the Bloch sphere. This qubit control enables us to quantify the dephasing of the single electron spins in our qubit, which we will discuss in the following section.

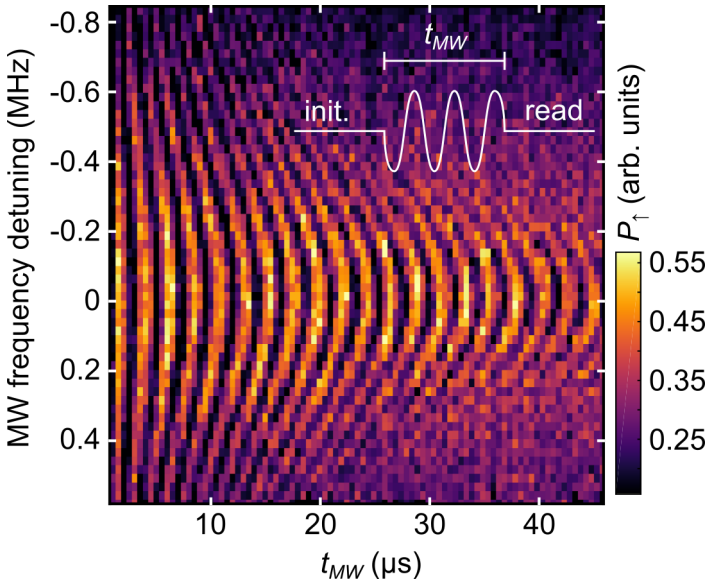

Figure 6.2. – The spin-up probability $P_\uparrow$ after a MW driving pulse as a function of the pulse length t_{MW} and the MW frequency detuning. Rabi oscillations with a frequency around 400 kHz are observed for zero detuning. Inset: schematic representation of the initialization to $|\downarrow\rangle$, the driving pulse of time t_{MW} and the spin-readout. Reprinted figure with permission from [67]. Copyright 2020 by the American Physical Society.

6.2. Dephasing time T_2^*

The dephasing time T_2^* is a measure for the loss of phase information for spins freely precessing on the equator of the Bloch sphere. The dephasing is a result of the interaction of the spin with the environment, such as fluctuating nuclear spins and charge noise. As we do only have one spin at a time, which is influenced by the environment, the measurement is repeated many times, yielding a time ensemble average of the dephasing in contrast to the space ensemble measurements in nuclear magnetic resonance (NMR).

6.2.1. Accessing dephasing with the Ramsey pulse scheme

Fig. 6.3 a shows the pulse sequence we employed for the determination of the dephasing time T_2^*. The qubit is initialized into its ground state $|\downarrow\rangle$ (Fig. 6.3 b). A MW pulse is applied to the gate pL rotating $|\Phi\rangle$ by $\pi/2$ around the x-axis of the Bloch sphere (Fig. 6.3 c). We then let the qubit evolve freely for a time of t_e (Fig. 6.3 d) and apply another $\pi/2$ pulse along the x-axis (Fig. 6.3 e). Finally, the resulting spin-state is read out (Fig. 6.3 f). We expect the spin-up probability to be described by

$$P_\uparrow(t_e) = A \exp\left(-\left(\frac{t_e}{T_2^*}\right)^2\right) \cos(2\pi\Delta f t_e) + B, \tag{6.1}$$

with $\Delta f = f_L - f_{MW}$ being the detuning of the MW frequency f_{MW} from the resonance frequency f_L. A and B are constants reflecting the qubit initialization and readout fidelity [86]. This represents an oscillation with a period in t_e depending on the MW detuning Δf with an envelope decaying exponentially with the dephasing time constant T_2^*.

6.2.2. Ramsey fringe measurement

Fig. 6.4 a shows the spin-up probability after applying the previously discussed pulse scheme, as a function of t_e and the laboratory time t. Each data point represents an average over 5 single-shot measurements. The measurement time for one line was roughly 7 s and the total measurement time was 18 h.

In order to extract the dephasing time, we average a subset of these traces resulting in a measurement time of $t_m = 10$ min for the data shown in Fig. 6.4 b. We clearly observe the oscillation with respect to t_e and fit Eq. 6.1 to extract $T_2^* = 18$ µs for this measurement time of 10 min. This value is remarkably close to the 20 µs (obtained

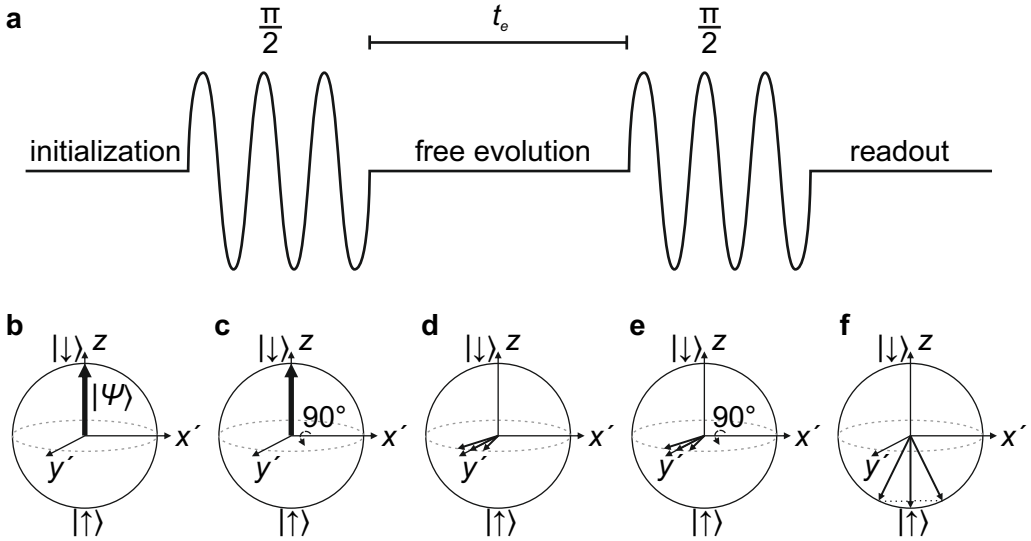

Figure 6.3. – Ramsey pulse sequence: **a** After initialization to $|\downarrow\rangle$, a $\pi/2$ pulse is applied, bringing $|\Psi\rangle$ into superposition of $|\downarrow\rangle$ and $|\uparrow\rangle$. The spin is freely evolving and dephasing for the time t_e, after which a second $\pi/2$-pulse allows to measure the degree of dephasing in the $|\downarrow\rangle, |\uparrow\rangle$ basis. **b-f** Representation of the pulse scheme on the Bloch sphere in the rotating frame of reference.

over a shorter measurement time $t_m = 98\,\mathrm{s}$) reported for a ^{28}Si/SiGe spin qubit in a QW material with 800 ppm of ^{29}Si and with a different magnet concept [36]. For another comparable device also employing a micromagnet T_2^* up to 10.4 µs have been reported for $t_m = 15\,\mathrm{min}$ lying in the same order of magnitude but slightly smaller [37]. In Ref. [86], we show that the charge noise in our device is most likely limiting the dephasing times observed in our qubit device. This charge noise limiting implies, that the reduction of nuclear spins in the vicinity of the qubit that we expect to obtain from our 60 ppm ^{29}Si source crystal, compared to the commonly used 800 ppm ^{29}Si material, does have no effect until charge noise is reduced significantly. As the reduction of charge noise is subject of ongoing research in our group and in the qubit community, one can imagine the hyperfine interaction of the spin qubit with adjacent nuclear spins to become the limiting mechanism once again. In this case, we would expect an impact of the higher purity source material towards longer qubit dephasing times.

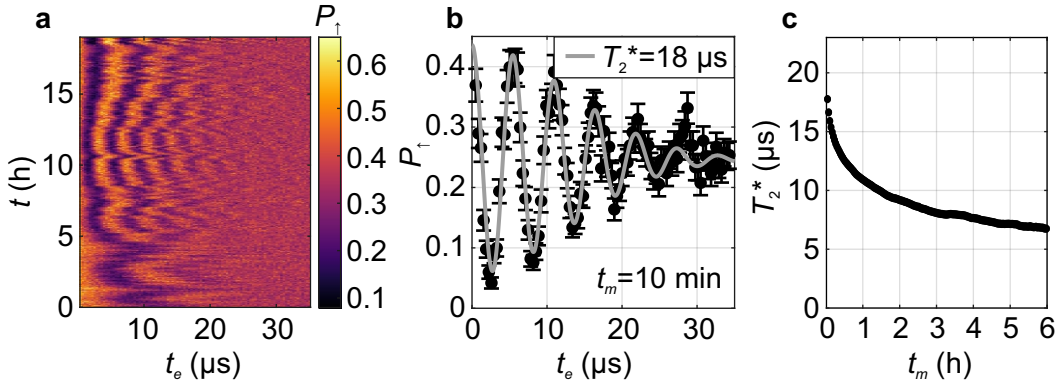

Figure 6.4. – Ramsey fringe measurement: **a** The spin-up probability $P_\uparrow$ after a Ramsey pulse sequence, as depicted in Fig. 6.3 a, as a function of the evolution time t_e over a total measurement time of 18 h. Each data point consists of 5 single-shot measurements with each line corresponding to a measurement time of 7 s. **b** The average of a subset of the data shown in **a** spanning a total measurement time of $t_m = 10$ min. A fit to Eq. 6.1, depicted in gray, yields $T_2^* = 18$ µs. **c** The average fitted T_2^* time for overlapping subsets of equal t_m as a function of the individual subset lengths t_m, representing the measurement time. With increasing t_m a decrease in T_2^* is observed. Adapted from [86] under the CC BY 4.0 license.

6.2.3. Extracting T_2^* dependent on measurement time

We partition the data shown in Fig. 6.4 a into subsets overlapping by 25 lines, with each subset covering a measurement time t_m. We fit Eq. 6.1 to each subset and average the resulting T_2^* times for all subsets with the same t_m. Fig. 6.4 c shows the average T_2^* as a function of the measurement time t_m covered by an individual subset. We observe a clear decrease in the extracted T_2^* times as t_m increases. This is expected, as a longer measurement time includes the interaction with noise of lower frequency.

One important takeaway from the data shown in Fig. 6.4 c is that T_2^* is a poor figure of merit for qubit characterization without the statement of the measurement time t_m over which the data was acquired. A better benchmark is the decoherence time T_2^{echo} that is independent of t_m and which we will discuss in the following section.

6.3. Refocusing slow noise by Hahn echo

We are able to suppress quasi-static noise by a slight modification of the Ramsey pulse scheme shown in Fig. 6.3 a. We introduce a refocusing π-pulse in the middle of the free evolution phase, as illustrated in Fig. 6.5 a. This type of pulse sequence was developed in the NMR context and is commonly referred to as Hahn spin echo sequence. In our experiment, we set the π rotation around the same axis as the $\pi/2$ rotations. We start with the same situation as for the Ramsey pulse sequence as we initialize to a $|\downarrow\rangle$ state, perform a $\pi/2$-pulse and let the spins evolve (Fig.6.5 b). After an evolution of $t_e/2$ the π-pulse inverts the distribution of dephasing spins (Fig. 6.5 c). Therefore, the spins which undergo a slower precession around the Bloch sphere (dark arrow in Fig. 6.5 b and c) z-axis are given a head start for the second free evolution time of $t_e/2$ and vice versa for spins with fast precession (light gray arrow in Fig.6.5 b and c) which are set back by the π pulse. This is effectively canceling any slow noise with respect to the measurement time scale at the end of the second free evolution (Fig.6.5 d). The last $\pi/2$-pulse rotates the spins into the z axis where the readout is performed. As indicated in Fig.6.5 e, in the case that the refocusing is successful, we expect a $|\downarrow\rangle$ state to be present at the readout phase.

Fig. 6.6 shows the spin-up probability $P_\uparrow$ after the application of a Hahn echo sequence as a function of the total evolution time t_e. Each data point is an average of 5000 single-shot measurements. We fit the data points using

$$P_\uparrow(t_e) = a\left(1 - \exp\left(-\left(\frac{t_e}{T_2^{\text{echo}}}\right)^{\alpha+1}\right)\right) + b, \tag{6.2}$$

with T_2^{echo} representing the Hahn echo decoherence time and α representing the frequency dependence of $1/f^\alpha$ noise in the regime around $f = 1/T_2^{\text{echo}}$. This equation yields a good fit with $T_2^{\text{echo}} = (128 \pm 2)\,\mu\text{s}$, which, to our knowledge, is significantly longer compared to T_2^{echo} times reported for ^{28}Si/SiGe qubit devices with a micromagnet and an isotopic purification of 800 ppm ^{29}Si with 99 µs by Yoneda et al. [36] and 109 µs by Sigillito et al. [37]. This suggests a lower noise level coupling to our qubit in the probed frequency regime of 7.8 kHz. We find $\alpha = 1.00 \pm 0.07$ indicating a $1/f$ frequency dependence for the noise coupling to the qubit around the frequency of 7.8 kHz. A more detailed analysis of the noise limiting the qubit coherence in our device can be found in Ref. [86]. It is possible to add even more π-pulses into the sequence in order to extend the coherence times further. Such a Carr-Purcell-Meiboom-Gill (CPMG) sequence allows to probe higher frequency noise

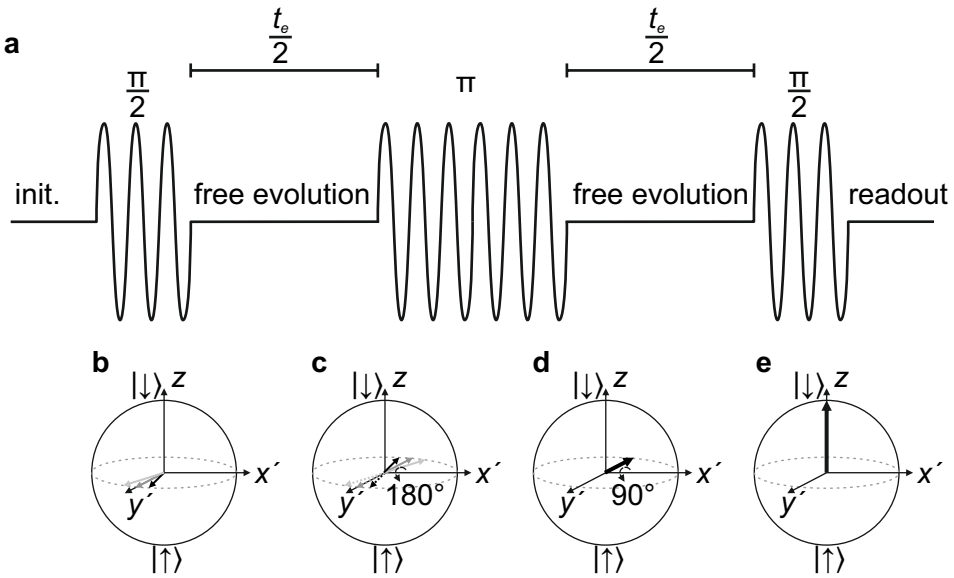

Figure 6.5. – Hahn spin echo pulse sequence: **a** A schematic representation of the pulse sequence, resembling the Ramsey pulse scheme shown in Fig. 6.3 a, but with a π-pulse inserted in the middle of the evolution time t_e. **b-e** Representation of the spin refocusing mechanism on the Bloch sphere in the rotating frame of reference.

coupling to the qubit, which is a topic of interest for ongoing experiments in our collaboration with the RWTH Aachen University.

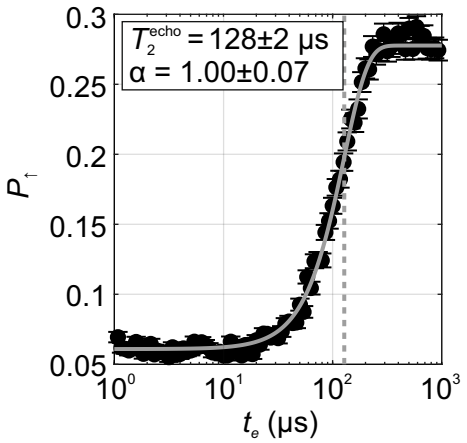

Figure 6.6. – Hahn echo measurement: the spin-up probability $P_\uparrow$ after applying a Hahn echo pulse sequence, as depicted in Fig. 6.5, as a function of the total free evolution time t_e. By fitting with Eq. 6.2, we extract $T_2^{\text{echo}} = (128 \pm 2)\,\mu\text{s}$ and $\alpha = 1.00 \pm 0.07$. Adapted from [86] under the CC BY 4.0 license.

6.4. Conclusion

In this chapter we have shown coherent single spin manipulation using EDSR with artificial spin-orbit coupling provided by the nanomagnet's transversal field gradient. This demonstration marks the first single e^- spin manipulation in the ^{28}Si/SiGe qubit platform developed at the University of Regensburg in cooperation with the RWTH Aachen. We studied the dephasing in our isotopically purified ^{28}Si/SiGe qubit device yielding $T_2^* = 18\,\mu\text{s}$ for a measurement time of 10 min. Due to charge noise limiting the qubit dephasing time [86], we found no significant improvements in T_2^* within our device grown with a 60 ppm ^{29}Si source material compared to devices featuring 800 ppm ^{29}Si QW layers [36, 37]. In the future, if charge noise is successfully reduced, the hyperfine interaction could become the limiting factor once again, creating the need for higher purity qubit host material. We extracted the dependence of T_2^* on the measurement time, finding a monotonously falling T_2^* with increasing measurement time. This proves our point, that a statement of T_2^* as a figure of merit is only valid in conjunction with a statement of the measurement time. Refocusing slow noise with a Hahn echo sequence, we extracted $T_2^{\text{echo}} = (128 \pm 2)\,\mu\text{s}$, which is significantly larger than previously reported values for ^{28}Si/SiGe spin qubit devices [36, 37], indicating less noise coupling to our qubit in the probed frequency regime. Some of the anticipated future experiments will focus on qubit operation at

elevated temperatures, where the novel charge sensor concept that we explore in the next chapter might open new opportunities.

7. Asymmetric sensing dot

In this chapter we will discuss a concept of a new kind of charge sensor. This sensor leverages the possibility of engineering the capacitive coupling of a SQD to one of the two electron reservoirs. Using this sensor we expect to achieve a larger SNR compared to a conventional SQD charge sensor and with this a larger readout bandwidth.

7.1. Concept of a new kind of charge sensor

7.1.1. Enhancement of signal-to-noise with a transistor

In the previous chapters, a conventional SET charge sensor with a constant V_{SD} bias was employed to detect a small change in the electrostatic potential, for example originating from the tunneling of an electron from the qubit QD to the reservoir. The change in the potential induces a significant change in the current I_{CS} flowing through the charge sensor. This I_{CS} is amplified via a transimpedance amplifier at room temperature. This method works quite reliably, but comes with a drawback: the SNR can be quite low, leading to integration times in the order of milliseconds. Compared to the gate times in the order of nanoseconds [88], this long readout time is detrimental for an efficient quantum error correction where the readout time should be on the order of the time required to perform quantum gates. Especially for high temperature qubits in silicon operated above 1 K a large SNR could improve the readout fidelity [42].

It is possible to enhance the readout bandwidth with RF reflectometry readout combined with cryogenic amplification [89–91], but this technique comes at the expense of bulky components mounted in the cryostat, limiting the scaling to larger numbers of qubits.

To enhance the baseband SNR of a charge sensor, one may implement a circuit as schematically depicted in Fig. 7.1 a which is derived from existing cryogenic amplification concepts [92, 93]. A constant current I_S is driven through a conventional SQD at a temperature of 40 mK indicated by the variable resistance R_S. R_S is modified by changes in the electrostatic potential at the SQD position. Using the

rising or falling slope of a Coulomb blockade peak, R_S varies significantly even for small changes in the electrostatic potential. The voltage $V_S = I_S \cdot R_S$ is applied to the gate of a high electron mobility transistor (HEMT) at a temperature of 1 K. The current flowing through the HEMT I_{HEMT} is consequently modulated by the voltage across the charge sensor V_S. V_S is modulated by changes in R_S induced by corresponding changes in the electrostatic potential, for example an electron entering or leaving a nearby qubit-QD. I_{HEMT}, carrying the amplified signal, may be measured with a standard room-temperature operational amplifier circuit. The key point of using the HEMT instead of the standard constant bias SQD combined with a room-temperature current measurement, is the low-temperature amplification of the signal present on V_S into the output signal, represented by I_{HEMT}, generating a larger SNR even when a conventional SQD charge sensor is employed.

7.1.2. Conventional quantum dot charge sensor

Fig. 7.1 b shows a schematic illustration of a SQD which is commonly used as a charge sensor in semiconductor host qubit devices and has also been used for the spin qubit measurements discussed in the previous chapters. The QD is shown in dark gray. The drain and source reservoirs are labeled D and S, respectively. The distance to both reservoirs is equal, yielding equal capacitive coupling from the QD to the reservoirs. Fig. 7.1 c shows a schematic Coulomb blockade diagram of the current through the QD as a function of the voltage across the sensor V_{SD} and the electrostatic potential, in this case influenced by the plunger gate voltage V_{pg} as indicated in Fig. 7.1 b. The blue regions indicate non-zero current flow with an initial configuration of the electrostatic potential. The white regions indicate zero current flow, where the charge sensor is in Coulomb blockade (see Sec. 2.4.1 and 2.4.2). The green dot represents the working point set by driving a constant current I_S through the sensor as described in 7.1.1. The voltage across the sensor may be described as $V_{S1} = I_S \cdot R_{S1}$ where R_{S1} is the resistance of the sensor in the initial electrostatic potential. The dark gray regions in Fig. 7.1 c indicate the regions of non-zero current flow after a shift in the electrostatic potential. As I_S is kept constant we expect a change in the voltage across the sensor $V_{S2} = I_S \cdot R_{S2} \neq V_{S1}$ with R_{S2} being the resistance of the sensor after the shift in the electrostatic potential, the new working point is indicated by the red dot in Fig. 7.1 c. The change of the voltage $\Delta V_S = V_{S2} - V_{S1}$ induced by the change in the electrostatic potential is indicated by the black arrow in Fig. 7.1 c. ΔV_S is the signal amplitude which is amplified by the circuit discussed in 7.1.1.

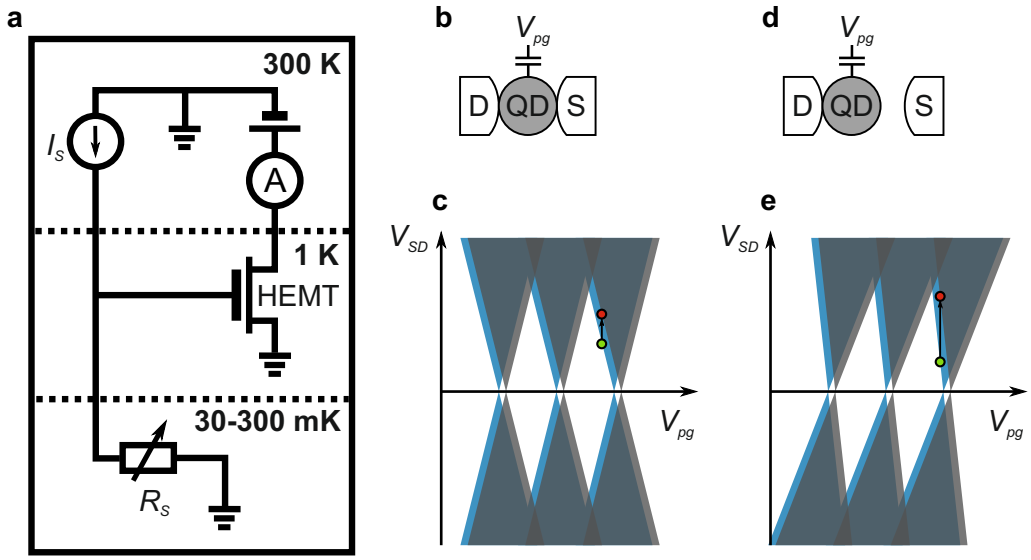

Figure 7.1. – **a** Electronic circuit schematic proposed to enhance SNR with a constant current I_S driven through the charge sensor R_S generating the voltage $V_S = I_S \cdot R_S$ applied to the HEMT gate. **b** Illustration of a conventional sensing dot on the basis of a SQD. The source and drain reservoirs are labeled S and D, respectively. The capacitively coupled plunger gate is labeled with V_{pg}. **c** Schematic representation of a current measurement through a conventional QD as a function of the bias voltage V_{SD} and the plunger gate voltage V_{pg}. The blue and gray regions show regions of non-zero current flow prior and after a shift in the electrostatic potential, respectively. The white regions form a symmetrical Coulomb diamond pattern. The green and red dots indicate the working points prior and after the potential shift. The length of the arrow connecting the green and red dots corresponds to the voltage swing ΔV_S. **d** Schematic of an ASD with a reduced capacitive coupling of the source reservoir to the QD. **e** Similar schematic as shown in c, but for an ASD device, with a reduced source capacitive coupling, leading to a tilted Coulomb diamond pattern.

7.1.3. Increasing the voltage swing

In order to increase the voltage swing ΔV_S, we propose a new concept of charge sensing schematically depicted in Fig. 7.1 d, where the drain reservoir is kept at the same distance to the QD compared to Fig. 7.1 b, while the source reservoir is moved away from the QD. This results in an asymmetrical capacitive coupling of the source and drain reservoirs onto the dot $C_S \ll C_D$ with C_S and C_D being the source and drain capacitance to the QD, respectively. Such an asymmetric coupling leads to a tilt in the white Coulomb blockade regions, as schematically depicted in Fig. 7.1 e. The same shift in the electrostatic potential as shown in Fig. 7.1 c should produce a larger ΔV_S indicated by the larger black arrow in Fig. 7.1 e. Note, that the sensor has to be tuned to the right initial working point in order to access this advantage. Just as in the case of the conventional charge sensor, the larger ΔV_S signal of the asymmetric charge sensor may be amplified by the HEMT circuit discussed in section 7.1.1. In the following section we will discuss one possible approach to decrease the source capacitance to achieve the condition $C_S \ll C_D$.

7.2. Device layout and engineering of the electrostatic potential

7.2.1. Decreasing capacitive coupling

A naive approach to decrease C_S would involve increasing the thickness of the tunnel barrier and consequently the distance between the QD to the source reservoir. This would lead to a reduction of C_S, since the capacitance is assumed to be dependent on the distance d between the capacitor plates according to $C_S = \epsilon_0 \epsilon_r \frac{A}{d}$, with the vacuum permittivity ϵ_0, the dielectric constant of the insulating material ϵ_r and the area of the capacitor plates A. However, by increasing the tunnel barrier thickness, the tunnel rate through the barrier gets reduced to a point where it becomes impossible to measure any significant current flow through the sensor with a reasonable V_{SD}. Consequently, we would like to conserve the thickness of the tunnel barriers as they are defined in a conventional QD, in order to retain a large enough sensor conductivity. We propose the introduction of a potential landscape as schematically depicted in Fig. 7.2 a, where we show the electrostatic potential as a function of the position x across the axis spanning the drain reservoir over the QD to the source reservoir. The side of the drain reservoir is unaltered compared to a conventional sensor QD. The thickness and height of the tunnel barriers are

set in a range where the tunnel current through the sensor is easily detectable. In order to increase the distance from the QD to the source reservoir, the key idea of our novel sensing concept is to introduce a slide potential which smoothly decreases from the QD towards the source reservoir. Fig. 7.2 a shows the Fermi energies of the drain and source $E_{F\ drain}$ and $E_{F\ source}$, respectively, for the case of a large V_{SD} of $\sim 10\,\mathrm{mV}$. As $E_{F\ source}$ is below the electrostatic potential of the slide region, we expect to achieve an increased distance between the source reservoir and the QD while keeping the current in the same order as for a conventional sensor QD. Due to the increased distance, we would realize $C_S \ll C_D$, resulting in tilted Coulomb diamonds as depicted in Fig. 7.1 e.

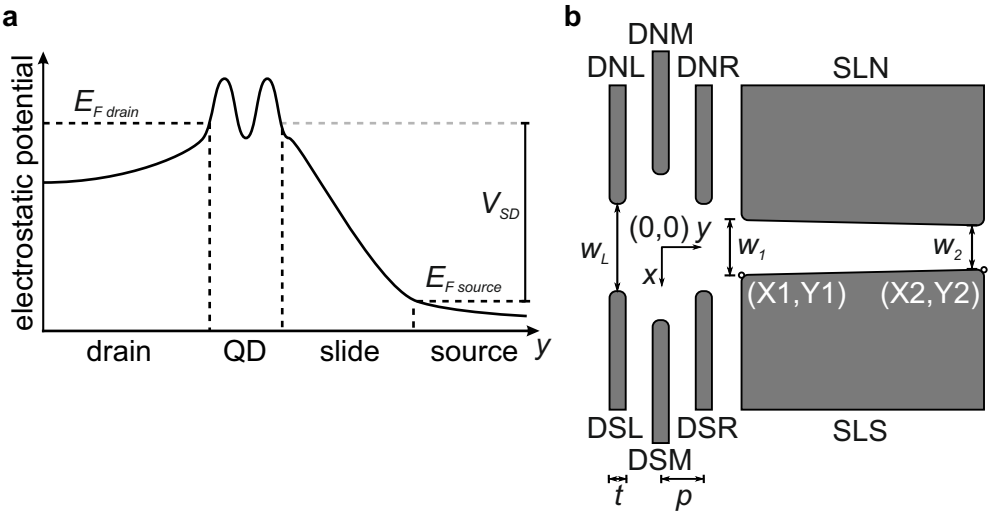

Figure 7.2. – **a** Schematic representation of the electrostatic potential as a function of the y coordinate across an ASD device. **b** Illustration of the geometry output obtained from the COMSOL simulations done by Josias Old at RWTH Aachen University [94]. The gate layout is designed to be symmetric with respect to the y-axis. The QD depletion gate thickness and the distance between QD depletion gates are labeled t and p, respectively. All dimensions and the coordinates of the slide gate pair SLN-SLS are given in Tab. 7.1.

From COMSOL simulations performed by Josias Old at the RWTH Aachen University [94], we have designed an initial gate layout geometry schematically depicted in Fig. 7.2 b. The aim of these simulations was to find a depletion gate layout acting below a global accumulation gate, that forms the potential landscape sketched in Fig. 7.2 a. For this first generation of ASD devices we have chosen a layout constraint of symmetry with respect to the y-axis in Fig. 7.2 b. The layout

was set up to form a single QD using the gate pairs DNL-DSL and DNR-DSR to deplete the underlying 2DEG to form the left and right tunnel barriers, respectively. The gate pair DNM-DSM is meant to couple primarily capacitively onto the QD in order to shift the electro-chemical potential of the QD. The slide potential is formed by the slide gate pair SLN-SLS placed on the source reservoir side of the QD. These gates have a distinct shape in order to create the steady decrease in the electrostatic potential from nearby the QD to the source reservoir. The precise dimensions of the gates were subject to the optimization process during the device simulation [94].

The coordinates obtained for the slide gates SLN and SLS as well as the dimensions for the QD depletion gates as denoted in Fig. 7.2 b are given in Tab. 7.1. Here, w_i with $i = L, M$ and N is the width of the channel formed between the left (DNL-DSL), middle (DNM-DSM) and right (DNR-DSR) QD depletion gates, respectively. The gap between the slide gates (SLN-SLS) is denoted by the widths w_1 and w_2 for the gap dimensions closer and further from the QD, respectively. Additionally the voltages applied to the depletion gates in the optimized simulation for a global accumulation gate voltage of $V_{ag} = 1.05\,\mathrm{V}$ are presented in Tab. 7.1, where V_L, V_M, V_R and V_{SL} correspond to the voltages symmetrically applied to the gate pairs DNL-DSL, DNM-DSM, DNR-DSR and SLN-SLS, respectively. Note, that the voltage V_L applied to gates acting primarily on the left tunnel barrier is significantly more negative than the voltage V_R mainly tuning the right tunnel barrier. This is explained by the presence of the slide gates in proximity of the right tunnel barrier influencing not only the slide potential region but increasing the right tunnel barrier as well.

7.2.2. Fabrication optimization

In order to reach a functional depletion gate design, starting from the geometry obtained from the simulation process, we performed an optimization of the EBL process parameters. For this, we used a test sample, with a similar layer structure as the one intended to be used for our ASD samples. Standard EBL and metallization was employed to pattern the depletion gate layer (see A.4 for details).

This process allows a detailed patterning of gate metal in areas defined in a CAD file. Each of these areas may require a different electron dose. For example, we found a strong dependence of the required electron dose on the size of the area to be exposed. Fig. 7.3 a shows a SEM image of the depletion gate layer at an early stage of the optimization process. Due to the well-known proximity effect the gates DSL, DSR, DNL and DNR are discontinuous, while the gates DSM and DNM are wider than intended. Furthermore, the gates SLN and SLS have a narrow connection line

gap dimension	(nm)	voltages	(V)
w_L	160	V_L	-0.14
w_M	270	V_M	0.78
w_R	160	V_R	0.48
w_1	100	V_{SL}	0.517
w_2	80		
t	30		
p	80		
slide coordinates	**(nm)**	**voltage**	**(V)**
X1	50	V_{SL}	0.517
Y1	150		
X2	40		
Y2	600		

Table 7.1. – Dimensions and voltages in the simulation for the geometry depicted in Fig. 7.2 b.

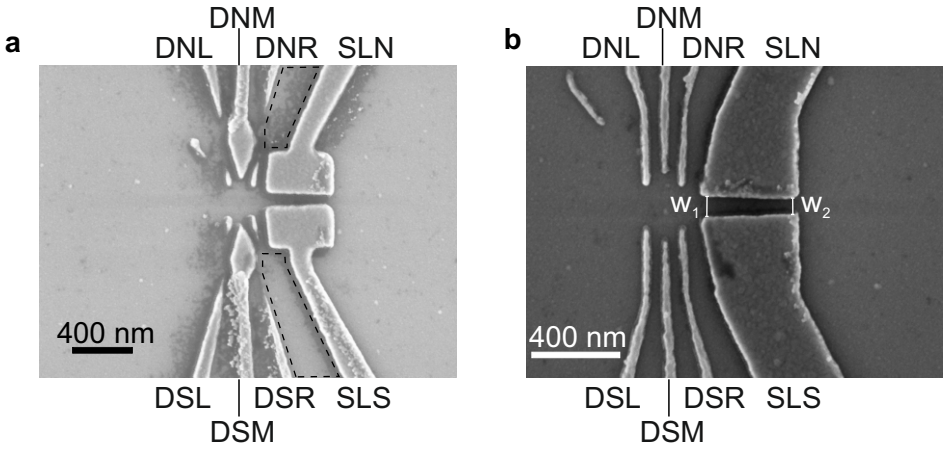

Figure 7.3. – Optimization of the EBL fabrication. **a** SEM image of an early fabrication recipe with discontinuous gates and unwanted reservoirs indicated by the dashed black lines. **b** SEM image of the optimized fabrication recipe, with the slide gate gap sizes w_1 and w_2.

w_1 (nm)	w_2 (nm)	Δw_1 (%)	Δw_2 (%)	Remarks
96.50	61.30	-3.50	-23.38	functional
94.60	74.20	-5.40	-7.25	functional
94.60	70.50	-5.40	-11.88	1 gate probably broken
96.50	66.80	-3.50	-16.50	functional
96.50	66.90	-3.50	-16.38	3 gates broken
94.60	68.70	-5.40	-14.13	1 gate broken
89.00	70.50	-11.00	-11.88	functional
94.60	63.10	-5.40	-21.13	functional
94.60	65.00	-5.40	-18.75	functional
94.61	**67.44**	**-5.39**	**-15.69**	

Table 7.2. – Slide gate gap widths w_1 and w_2 and their deviations Δw_1 and Δw_2 from the target gap dimensions $w_1 = 100\,\text{nm}$ and $w_2 = 80\,\text{nm}$ for nine samples fabricated with the optimized recipe. A mean value is given at the bottom for each column in a bold font. Remarks about the potential device functionality are noted in the rightmost column.

potentially allowing for reservoirs to form in unintended locations, indicated by the dashed lines in Fig. 7.3 a.

A series of dose factor adjustments in the CAD file, with feedback obtained by SEM images after each optimization step, led to a reproducible, high-yield fabrication process with one exemplary result shown in Fig. 7.3 b. Here, all gates are connected and well defined. The connection lines of SLN and SLS are wider compared to Fig. 7.3 a which should eliminate the possibility of unintended reservoir formation.

7.2.3. Feedback to the simulation

We extracted channel widths of $w_1 = 94.6\,\text{nm}$ and $w_2 = 74.2\,\text{nm}$ for the sample shown in Fig. 7.3 b from SEM. As these dimensions differ from the target values of $w_1 = 100\,\text{nm}$ and $w_2 = 80\,\text{nm}$, we fed back the measured dimensions to the simulation, performed by Malte Neul at the RWTH Aachen University, in order to get an insight into the consequences induced by this smaller gap size. Fig. 7.4 shows the electrostatic potential across the ASD for the target slide channel width of $w_1 = 100\,\text{nm}$ and $w_2 = 80\,\text{nm}$ in red with $V_{SL} = 0.517\,\text{V}$. Shown in blue, the electrostatic potential with the same slide gate voltage for the extracted dimensions $w_1 = 94.6\,\text{nm}$ and $w_2 = 74.2\,\text{nm}$ is plotted. It is apparent, that the tunnel barrier between the QD and the source reservoir is significantly wider than intended, possibly leading to a reduction in the tunneling current through the ASD device. As shown

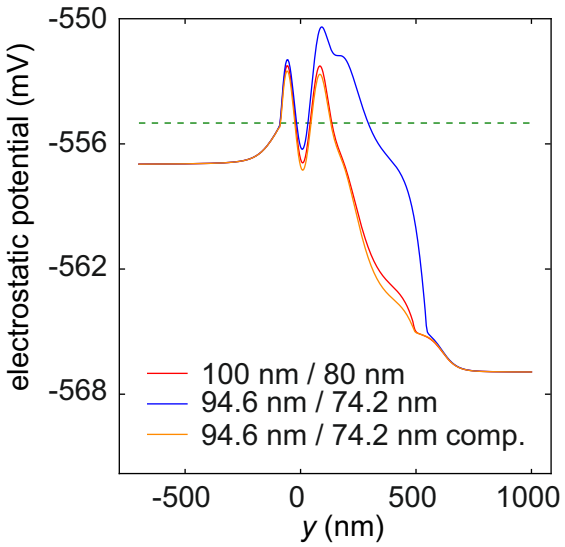

Figure 7.4. – Simulated electrostatic potential across the ASD device for the target slide channel width of $w_1 = 100\,\text{nm}$ and $w_2 = 80\,\text{nm}$ with $V_{SL} = 0.517\,\text{V}$ (red line), the experimentally determined $w_1 = 94.6\,\text{nm}$ and $w_2 = 74.2\,\text{nm}$ with $V_{SL} = 0.517\,\text{V}$ (blue line) and the experimentally determined $w_1 = 94.6\,\text{nm}$ and $w_2 = 74.2\,\text{nm}$ with a $V_{SL} = 0.526\,\text{V}$ voltage compensation. The simulations have been performed by Malte Neul RWTH Aachen University.

in orange, by an adjustment of the slide gate voltage to $V_{SL} = 0.526\,\mathrm{V}$, it is possible to tune the electrostatic potential in such a way, that the tunnel barrier between the QD and the source reservoir as well as the slope of the slide potential are restored to match the potential obtained with the target slide gate dimensions, manifested in the coinciding orange and red curves in Fig. 7.4.

Tab. 7.2 shows the slide channel widths w_1 and w_2 as well as their deviations Δw_1 and Δw_2 from the target values $w_1 = 100\,\mathrm{nm}$ and $w_2 = 80\,\mathrm{nm}$ for a total of 9 samples, all fabricated with the same optimized recipe. The gap widths were evaluated by SEM imaging as shown in Fig. 7.3 b and the bold numbers represent a mean value for the respective column. Since $\Delta w_2 > \Delta w_1$ it is probable that the smaller gap w_2 is more sensitive to effects altering the electron beam exposure. Although the values of the gap sizes tend to come out smaller than intended, the overall yield is 66 % for the sample size of 9 e-beam written structures, which is a good result for a proof-of-concept fabrication.

Since we showed that a slight reduction in the gap widths w_1 and w_2 may be compensated by tuning V_{SL}, we decided to fabricate proper ASD samples with this optimized recipe, to realize the first demonstration of this ASD concept in silicon.

7.3. Instabilities in ASD devices

We fabricated 12 samples with the process introduced in 7.2. Six samples featuring the new slide gate pair SLN-SLS are based on the Si/SiGe heterostructure R2138 (see Fig. 3.2 a) and were fabricated in a first run. All six devices belonging to this first run show instabilities over time with respect to the current through the sample at constant bias and gate voltages. Since these instabilities do not allow for a reproducible characterization of the device properties such as a determination of the source capacitive coupling C_S, we fabricated a second run based on the different Si/SiGe heterostructure R2160 with four devices including the slide pair SLN-SLS and two devices as test structure QD devices without the slide gate pair SLN-SLS. For the second run, we observe a similar instability in the current through the devices for the structures containing the slide gate pair SLN-SLS. One of the two test structures without slide gates SLN-SLS showed a more stable behavior which allowed measurements without thermal cycling for several days, while the other test structure has a broken DSL gate inducing instabilities [55]. One possible explanation for the instabilities mainly observed in devices containing slide gates is the promotion of charge reconfigurations into the trap states discussed in chapter 3. It is possible that

the larger area of the slide gates combined with a typically positive V_{SL} (compare table 7.1) is favorable to induce the charge transfer process into the trap states. This hypothesis should be tested by performing biased cooling experiments with a negative voltage applied to the slide gates during the cool-down. After the cool-down, we would expect that V_{SL} could be set close to 0 V while still forming the desired slide potential. This would potentially decrease the charge reconfigurations due to a smaller voltage difference of the slide gates and the QW during the measurement.

One device containing the slide gates, R2160A5MIV, did not show any sign of electron accumulation in the form of a significant current flow when V_{ag} was increased from $V_{cd} = 0\,\mathrm{V}$ at a temperature of $T \approx 300\,\mathrm{mK}$. This was likely caused by a disconnected DSL gate which acts as a charged metallic island that depletes the underlying 2DEG when the device is cooled-down to 300 mK. As already discussed in section 3.5, we may employ the illumination of the sample in order to modify the occupation of the trap states in a way that accumulation is achieved for a small increase of V_{ag}, independent of the voltage applied to the gate during illumination. We expect this mechanism to work whether the gates are connected or not, as the charge transfer is mainly driven by the incoming photons. With this consideration we chose to illuminate the device with a red LED for 1 min at a current of $I_{LED} = 50\,\mu\mathrm{A}$. This illumination process led to a significant current flow through the device as soon as V_{ag} was increased. We found this behaviour to be independent of the voltages that are applied to the depletion gates and the accumulation gate, in the same fashion as already discussed in section 3.5.1. We therefore chose to illuminate the device at $V_{ag} = -0.5\,\mathrm{V}$, $V_{SL} = 0\,\mathrm{V}$ and $V_D = 0.6\,\mathrm{V}$, with V_D being the voltage applied to the QD depletion gates, unless noted otherwise.

We continued to measure this sample after illumination and experienced a more stable behaviour with stable measurement periods of three to four days compared to other devices including the slide gates SLN-SLS. In the case when the current through the sample was decreasing significantly over time, we illuminated the device at specific gate voltages, in order to restore the initial conditions, without the need for a thermal cycle to room temperature for this sample (R2160A5MIV).

7.4. Asymmetric Coulomb diamonds

In this section, we will explore the functionality of the ASD device R2160A5MIV with respect to a decreased source capacitive coupling. We may quantify this coupling by measuring the current through the sensing dot as a function of V_{SD} and the varying

electrochemical potential tuned by a plunger gate in proximity to the QD as plotted in Fig. 7.1 c and e. This leads to diamond shaped regions where the current flow is suppressed due to Coulomb blockade (see Fig. 2.7 in Sec. 2.4.2). We are using the a configuration where the reservoir without slide gates, in this chapter denoted as drain, is grounded and the bias is applied on the reservoir next to the slide gate pair SLN-SLS, denoted as source in this chapter.

In the measurements discussed in this chapter the bias voltage V_{SD} is applied to the source contact, while the drain contact is grounded using a transimpedance amplifier, as schematically depicted in Fig. 7.5. The output voltage of the transimpedance amplifier, which is proportional to the current through the ASD device, is digitized by a voltmeter. For further information on the setup, see A.2.3.

In the case of a grounded drain contact and V_{SD} applied asymmetrical on the source reservoir, the borders of the Coulomb blockade regions are described by

$$m_- = \frac{C_{pg}}{C_S} \tag{7.1}$$

as negative slope and

$$m_+ = \frac{C_{pg}}{C - C_S} \tag{7.2}$$

as positive slope with C_{pg} the capacitive coupling of the plunger gate to the QD, C the self-capacitance of the QD and C_S the capacitive coupling of the source reservoir to the QD (see Sec. 2.4.2). The lever arm of the source reservoir onto the QD electrochemical potential is given by

$$\alpha_S = \frac{C_S}{C} = \frac{|m_+|}{|m_+| + |m_-|}. \tag{7.3}$$

7.4.1. Proof of concept by slide gate variation

Fig. 7.6 shows measurements of the current through the sample as a function of V_{SD} and V_{DNR} while V_{SL} is varied from $V_{SL} = 50\,\mathrm{mV}$ (a) to $V_{SL} = -20\,\mathrm{mV}$ (d). In this device we used the DNR gate as the plunger gate which tunes the QD electrochemical potential, since the DNM-DSM gate pair did not perform well as plunger gates in this device. One has to keep in mind, that the gate DNR may have a significant impact on the tunnel barrier of the QD on the side of the source reservoir.

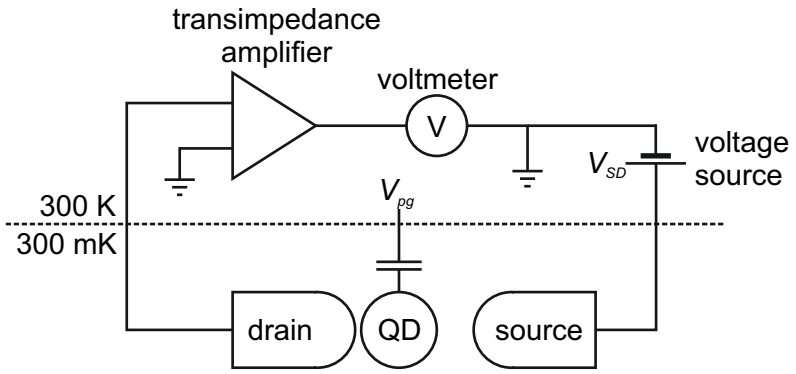

Figure 7.5. – Schematic representation of the ASD measurement setup. The source of the ASD device is connected to a programmable voltage source providing the source-drain bias voltage V_{SD}. The current flowing towards ground is measured via a transimpedance amplifier, which outputs a voltage proportional to the current flowing through the ASD sample. This voltage is measured by a standard digital voltmeter. The plunger gate is capacitively coupled to the QD. The voltage source providing V_{pg} applied to the plunger gate as well as the voltage sources and couplings for all other gates are omitted for clarity.

We manually select a range in V_{DNR} considered for the slope extraction. Note that we choose the last slope of each measurement in order to get comparable results. An extraction on a Coulomb diamond would be prone to error due to smaller V_{DNR} range compared to the available range for the last visible slope. We find the data point with a current value closest to $I_{thr} = 0.1\,\mathrm{nA}$ for each column of data points with a fixed V_{DNR}. These points are marked by the x-symbols in Fig. 7.6, lying on the border of the Coulomb blockade regime. To extract m_- and m_+, the negative and positive slopes of the Coulomb blockade borders, respectively, we perform a linear regression to the threshold data points.

Fig. 7.7 a reports the extracted slopes m_- and m_+, with the standard deviation of the fit as error bars, for the four measured V_{SL} shown in Fig. 7.6. Using Eq. 7.3, we calculate the source lever arm α_S for each of the four V_{SL} as shown in Fig. 7.7 b. The lever arm α_S, and with this the capacitive coupling of the source reservoir to the QD, is found to decrease for more negative V_{SL}. Comparing the largest and lowest observed values $\alpha_S(V_{SL} = 50\,\mathrm{mV}) = 0.218 \pm 0.006$ and $\alpha_S(V_{SL} = -20\,\mathrm{mV}) = 0.069 \pm 0.009$ yields a reduction of α_S by more than a factor of 3 just by tuning V_{SL}. This is an indication, that the potential created by the slide gate pair SLN-SLS is raised towards more negative V_{SL} leading to a larger distance of the source reservoir to

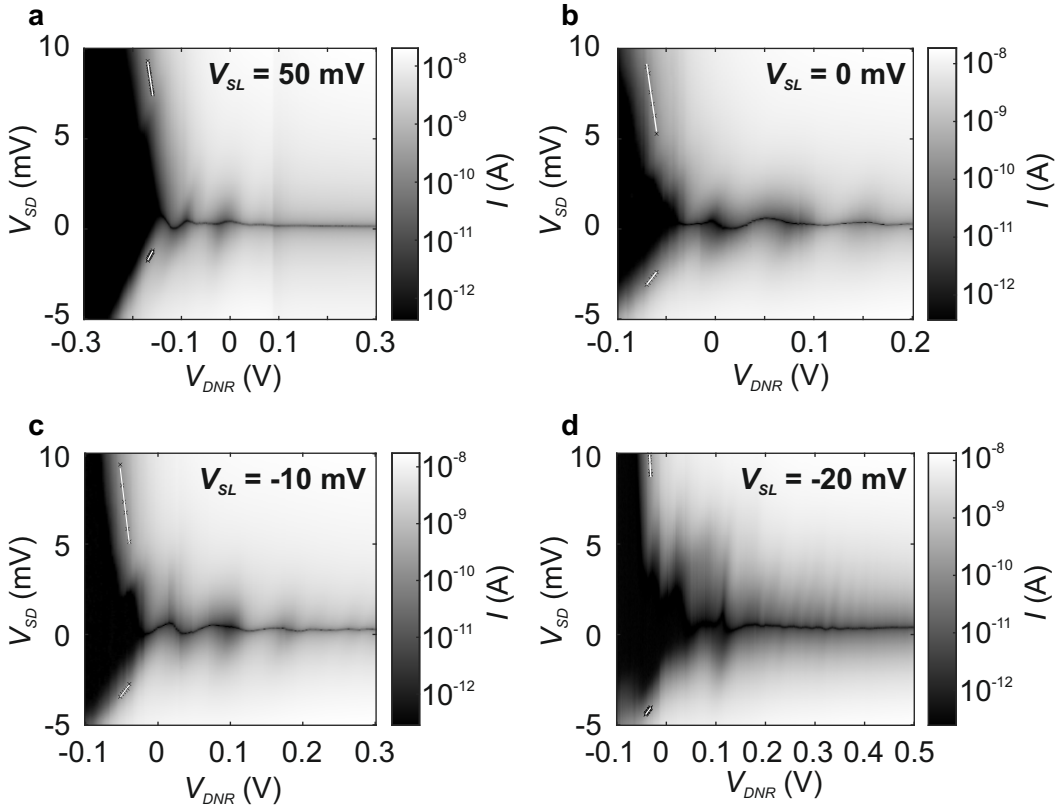

Figure 7.6. – Current through the ASD device as a function of the bias voltage V_{SD} and the gate voltage V_{DNR}. The drain reservoir is grounded while the bias is applied to the source reservoir which is adjacent to the slide gate pair SLN-SLS. The x-symbols mark the data points lying closest to the threshold current $I_{thr} = 0.1\,\mathrm{nA}$ and the solid lines mark the linear regression fit results. We apply a different V_{SL} in each measurement: **a** $V_{SL} = 50\,\mathrm{mV}$ **b** $V_{SL} = 0\,\mathrm{mV}$ **c** $V_{SL} = -10\,\mathrm{mV}$ **d** $V_{SL} = -20\,\mathrm{mV}$.

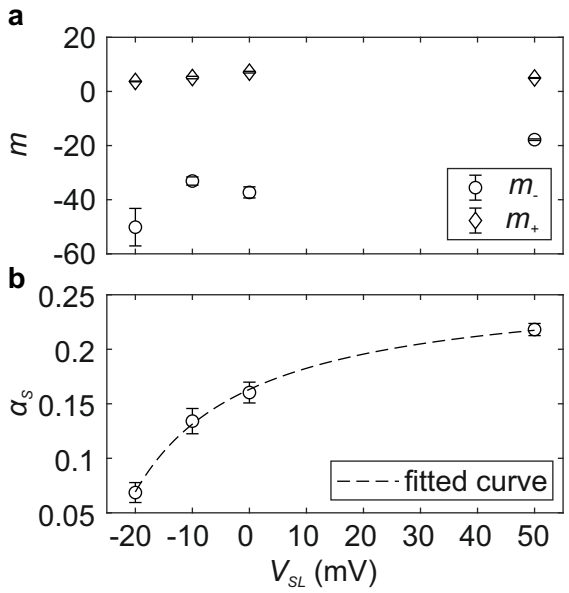

Figure 7.7. – **a** Positive and negative slopes m_+ and m_- as a function of V_{SL} as extracted by a linear regression to the points marked with x-symbols in Fig. 7.6. **b** Source lever arm α_S as a function of V_{SL} calculated from the m_+ and m_- shown in a, according to Eq. 7.3. The dashed line shows a fit to the α_S data according to Eq. 7.5.

the QD d_{S-QD}. The simulations found a capacitance ratio of $\frac{\alpha_D}{\alpha_S} = \frac{C_D}{C_S} = 5.5$, with $\alpha_D = \frac{C_D}{C}$ being the drain lever arm and C_D the drain to QD capacitance [94]. This capacitance ratio may be compared to the factor 3 change in α_S under the assumption, that V_{SL} does not change α_D significantly. The change in α_S observed experimentally is slightly lower than the simulated capacitance ratio, which will be discussed later in this section. The source capacitive coupling is expected to scale roughly inversely to d_{S-QD} assuming a plate capacitor model, and we assume a linear increase of d_{S-QD} with respect to a change V_{SL}. This would imply that the source lever arm scales with

$$\alpha_S \propto \frac{1}{V_{SL}}. \tag{7.4}$$

The dashed line in Fig. 7.7 b shows a fit to the α_S data using

$$\alpha_S(V_{SL}) = \frac{a}{V_{SL} + b} + t, \tag{7.5}$$

with the fitting parameters a, b and t. The fit matches the experimental data well, although a larger data set would be helpful to get a more solid verification of our hypothesis. As the device required illumination after a charge reconfiguration, it was not possible to obtain additional α_S data with other V_{SL} for this configuration.

For comparison, the extraction of the source lever arm on the conventional SQD charge sensor data of a DQD device studied in earlier work in our group [40] yields a value of $\alpha_S = 0.42 \pm 0.01$ for a comparable measurement configuration with the drain reservoir grounded and the bias voltage applied to the source reservoir (see Fig. A.1). This value for α_S is larger by more than a factor of 6 compared to the lowest $\alpha_S = 0.069 \pm 0.009$ found in our ASD device, which is another indication that the reduction of the source capacitive coupling has been achieved as this factor of 6 lies close to the simulated capacitance ratio of 5.5. For the data shown in Fig. 7.7 b, even the largest value with $\alpha_S = 0.218 \pm 0.006$ lies below the value obtained for the conventional QD charge sensor, potentially because the slide potential still has an effect even for the largest V_{SL} shown in Fig. 7.7 b.

7.4.2. Slide potential variation

In Fig. 7.8 the simulated electrostatic potential across the ASD device is shown for three different V_{SL}. Comparing the crossing points of the three potential curves with $E_{F\ source}$, marked by the circles, it is apparent that for lower (higher) V_{SL}, the simulations predict an increased (decreased) distance of the source reservoir to the

QD d_{S-QD}. This is in excellent agreement with the reduced (increased) α_S observed experimentally for a more negative (positive) V_{SL}, corresponding to an increased (decreased) d_{S-QD}, in the previous section.

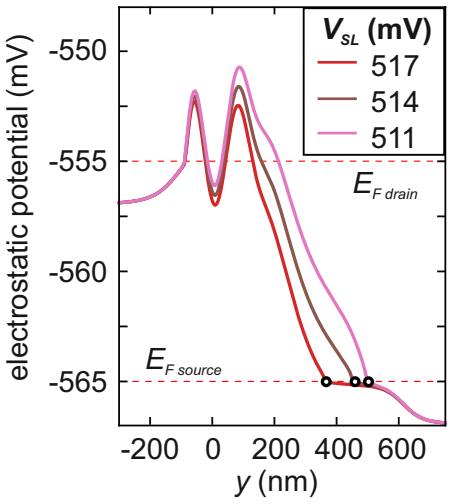

Figure 7.8. – Simulated electrostatic potential as a function of the y-coordinate as indicated in Fig. 7.2 b for three different V_{SL}. The upper and lower dotted lines indicate $E_{F\ drain}$ and $E_{F\ source}$, respectively. The crossing points of the potential curves with $E_{F\ source}$ are marked by the circles. Simulations performed by Josias Old at RWTH Aachen University [94].

7.5. Conclusion and outlook

In this chapter, we have introduced the concept of a new kind of charge sensor, the ASD based on the reduction of the capacitive coupling of the source reservoir to the sensor QD. We discussed that simulations done at the RWTH Aachen suggest that an electrostatic potential can be engineered where the tunnel rates through the QD barriers are kept constant while decreasing the source capacitive coupling. This electrostatic potential landscape is mainly shaped by the introduction of an additional slide gate pair SLN-SLS in between the QD and the source reservoir. The optimization of the fabrication process has been discussed. We experimentally showed that we can achieve a variation of the source lever arm by more than a factor of three just by tuning the slide gate voltage. The smallest source lever arm observed on our ASD device is smaller by a factor of 6 compared to the source lever arm measured on a conventional sensing dot studied in earlier work in our

group also matching the simulated capacitance ratio of 5.5. We see this as a first proof of principle for the ASD concept in silicon and look forward to the results on more advanced ASD designs with adjacent DQD devices, depicted in Fig. 7.9, already fabricated and currently under test, giving insight on the SNR and the back-action of the sensor on the adjacent qubit. This new device generation employs a longer slide potential compared to the generation studied in this thesis, potentially offering a further reduction of the capacitive coupling to the reservoir. Additionally, a more sophisticated transimpedance amplifier, which is ready to be used in future experiments would allow us to select the reservoir we apply the V_{SD} bias to without the need of cutting and making electrical connections. This would enable the probing of the source and drain capacitive couplings on the same electrostatic configuration and therefore a direct measurement of the capacitance ratio.

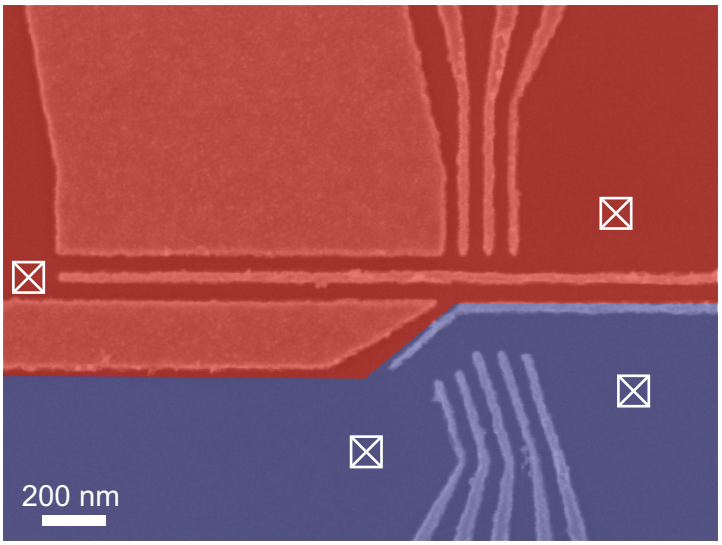

Figure 7.9. – SEM image of the next generation ASD depletion gate layer fabricated by Inga Seidler at the RWTH Aachen. This type of device including a DQD region (blue part) adjacent to the ASD region (red part) is characterized in ongoing work at the University of Regensburg. The crossed white boxes indicate the electron reservoirs.

8. Conclusion and Outlook

In this thesis, we studied MBE-grown Si/SiGe heterostructures and their application in a gate-defined spin-qubit device.

We showed an excellent homogeneity of the mobility and charge carrier density as a function of the accumulation gate voltage over 1.5 mm of active Hall bar region. Furthermore, we confirmed the interface trap state model developed in [40, 54] with a detailed biased cool-down experiment and extended the model to describe the characteristic behavior we observed when the samples are illuminated at cryogenic temperatures. We found the illumination to create an electrostatic configuration in the sample, which lead to an immediate increase in current when the accumulation gate voltage was increased, independent of the voltage applied during illumination. The electron mobility was found to decrease upon illumination, most likely due to the creation of a secondary conduction channel. Based on these findings, we suggest to use the illumination of samples with care, especially for qubit devices, where a secondary conduction channel would hamper the qubit operation. As our understanding of the illumination process is still in its infancy, we suggest to perform more illumination studies with heterostructures featuring varying SiGe spacer thicknesses and to analyze the influence of the illumination intensity in more detail.

Turning towards our ^{28}Si/SiGe spin qubit device based on a heterostructure grown by means of MBE using an isotopically purified source of solid ^{28}Si with 60 ppm of remaining ^{29}Si, we discussed the initial tuning of the device. Here, we found instabilities in the current, which we attributed to charge reconfigurations after the initial charge carrier accumulation following the cool-down. After these initial instabilities and gate voltage adjustments, we observed a well-defined SQD in the charge sensing part of the device with many Coulomb oscillations enabling a sensitive chage state readout in the qubit region. The first charge stability diagram discussed in this thesis showed indications for a multitude of QDs formed in our device. By tuning of the depletion gate voltages, eliminating QDs forming under one gate and cutting the coupling to one of the two qubit region electron reservoirs, we reached a SQD configuration in the qubit region. The last detected charge transition, which

we attributed to the change from zero to single electron occupation, showed signs of a tunable tunnel barrier to the electron reservoir. This tunability is essential for the spin-to-charge conversion readout technique.

We quantified the tunnel rates for electrons entering and leaving the qubit SQD during the spin-to-charge conversion "read" phase and found them to be well suited for our readout configuration. Varying the load time in this pulse, we observed an exponential decay of the spin-up fraction attributed to the spin relaxation into the spin-down ground state with a time constant T_1. We found a large and constant $T_1 > 0.5\,\mathrm{s}$ for the low magnetic field regime below 1.6 T and a monotonous increase in the relaxation rate in the high field regime above 2 T. In between these regimes, we observed a sharp peak in the relaxation rate. We attributed this peak to the increased spin-relaxation due to a mixing of the valley- and spin-split states $|-,\uparrow\rangle$ and $|+,\downarrow\rangle$ when the Zeeman-splitting is equal to the valley splitting. Using this precise measure, we found an extraordinarily large valley splitting of $(213.1 \pm 0.3)\,\mu\mathrm{eV}$ in our device, which is 2 to 3 times larger than the values previously reported for Si/SiGe spin qubit devices [28, 30, 70, 74–80]. As the valley splitting is influenced by the quality of the QW interface, it is possible that the MBE-growth provides a sharper interface compared to chemical vapor deposition (CVD)-growth. This would explain the large valley splitting we observed in our device, but further valley splitting studies on MBE-grown heterostructures are required to confirm this hypothesis. We observed a robust and reproducible shift in the valley splitting of $(15 \pm 2)\,\%$ in response to a change in the gate voltage configuration. Using self-consistent Schrödinger-Poisson simulations, we excluded the variation of the out-of-plane electric field as a cause for the observed variation in valley splitting. We found a lateral displacement of the electron wavefunction relative to monolayer steps in the QW interface as the most plausible explanation for the tunability of the valley splitting. We suggest further experiments on MBE-grown Si/SiGe devices in order to gather more statistics on the valley splitting across multiple devices as a consistently large valley splitting would open the route towards qubit operation at elevated temperatures at around 1 K.

We have shown the all-electrical coherent spin manipulation via EDSR by employing the nanomagnet's magnetic field gradient to provide an artificial spin-orbit coupling in our device. With the manipulation in place, we extracted the dephasing time of 18 µs for a measurement time of 10 min and we further observed a strong dependence of the dephasing time on the measurement time, with short measurement times yielding the longest dephasing times. We eliminate this measurement time dependence by performing a Hahn echo sequence, mitigating quasi static noise on the measurement

time scale. We found a significantly longer $T_2^{\text{echo}} = 128\,\mu\text{s}$ compared to the values of up to 109 µs [37] for ^{28}Si/SiGe devices reported in the literature. This indicates less noise coupling to our qubit in the 7.8 kHz frequency regime. We suggest further experiments employing CPMG pulse sequences to probe higher frequency noise coupling to our spin qubit. Furthermore, a fidelity estimation by means of randomized benchmarking would give further insight into the level of control achievable in our device and experimental setup. As we found our device to be charge noise limited in Ref. [86], we suggest to consider changing the magnet design in order to reduce the coupling of charge noise onto the spin qubit. This however is always a tradeoff between the level of qubit control and the achievable coherence.

Our group is already working towards elevated temperature qubit operation using Pauli spin blockade as a readout mechanism. This method benefits from a large valley splitting yielding a large singlet-triplet splitting and it would be favorable to have a large SNR and high bandwidth charge sensing in order to resolve spin-signals at higher temperatures.

In the last part of this thesis, we showed the proof-of-concept design, fabrication and measurement of a new kind of charge sensor, leveraging the tunability of the capacitive coupling of a reservoir to the sensor QD to obtain a large SNR. We found a tunability of the capacitive coupling by a factor of 3 induced by a variation of the voltage applied to the newly introduced slide gates. These gates are intended to effectively manipulate the distance of the reservoir to the sensor QD while keeping the tunnel barriers of the QD constant. Current research in our group concentrates on the next generation of devices with such a new asymmetric charge sensor placed next to a DQD, enabling the study of the charge sensing performance such as the SNR and the bandwidth of the readout circuit. Such a device would also give access to the sensor's back-action on the spin qubit, as the concept requires fairly high bias voltages on the sensor resulting in phonon emissions potentially interacting with the spin qubit. If the SNR is enhanced as expected, this kind of device would be a prime candidate for the demonstration of elevated temperature spin qubit operation in Si/SiGe devices.

A. Appendix

A.1. Determination of source lever arm of conventional charge sensor

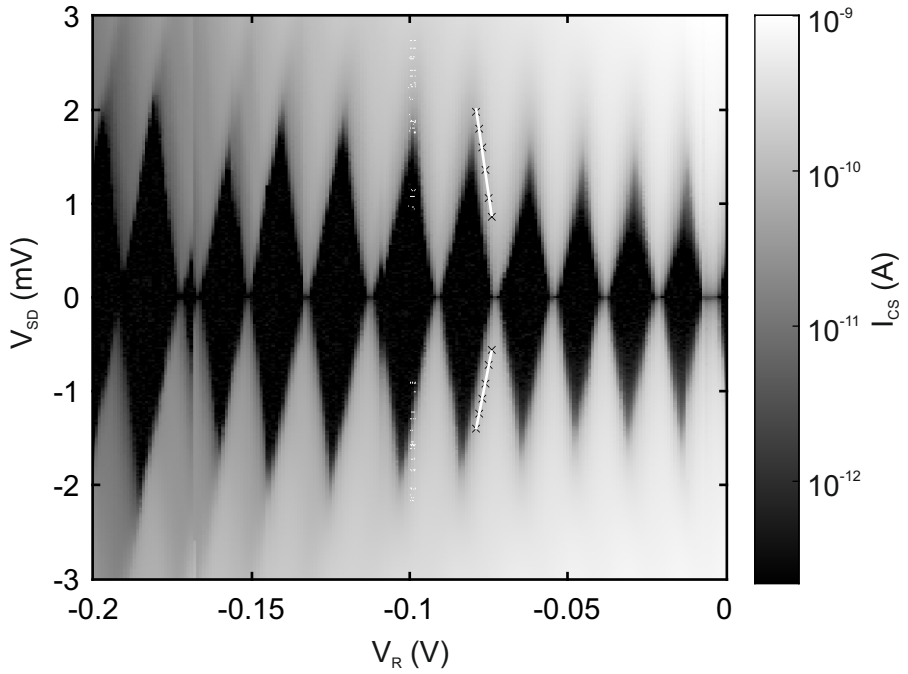

Figure A.1. – Current through the charge sensor of the device R2140E1MVI as a function of the bias voltage V_{SD} applied to one reservoir and the gate voltage V_R tuning the electrostatic potential of the sensor dot. The linear regression to the data points closest to a $I_{thr} = 0.1\,\mathrm{nA}$ (marked with x-symbols) yield $m_- = -0.23 \pm 0.009$ and $m_+ = 0.169 \pm 0.003$. With Eq. 7.3 a source lever arm of $\alpha_S = 0.42 \pm 0.01$ is obtained. This device has already been discussed in previous work in our group [40].

A.2. Measurement setup information

A.2.1. He dewar with magnet insert

The Si/SiGe Hall bar samples discussed in chapter 3 were measured in a liquid ^{4}He-dewar with a superconducting magnet insert. The base temperature was kept around 1.5 K by pumping the magnet insert enclosing the sample rod. No filtering was applied in these measurements obtained with standard low frequency lock-in techniques, employing EG&G Model 7260 DSP lock-in amplifiers for current supply and voltage measurements. A Yokogawa GS200 dc voltage source was used for the accumulation gate voltage supply.

A.2.2. Dilution refrigerator setup

The device studied in the chapters 4, 5 and 6 was measured in an Oxford Triton dilution cryostat at a base temperature of 40 mK. The dc lines were filtered by π-filters with a cut-off frequency of 5 MHz at room temperature followed by a copper-powder filter (attenuation of 60 dB at 3 GHz and 80 dB at 12 GHz) and RC low-pass filters at base temperature. We employed RC filters with 10 kHz cut-off frequency for the electron reservoirs and the gates intended for fast control, while all other gates were filtered with a cut-off frequency of $\sim$0.68 kHz. The electron temperature was determined to 114 mK. The voltage pulses are applied by a Tabor Electronics WX2184C arbitrary waveform generator. The MW signals employed for spin-manipulation are created in a Rhode & Schwarz SMW200A signal source. The charge sensor signal is amplified at room temperature using a I-V converter SP983C by Basel Precision Instruments. The amplified output voltage is digitized by an AlazarTech ATS9440 ADC card in the measurement PC.

A.2.3. ^{3}He-cryostat

The ASD measurements presented in chapter 7 were performed in a ^{3}He-cryostat with a base temperature around 300 mK. The electron temperature could not be determined precisely but we have evidence that the wiring solution in place during the measurements led to a higher electron temperature in the order of 1 K. The electrical measurement setup is shown in Fig. 7.5 of chapter 7. The transimpedance amplifier employed in the measurements is a Femto DLPCA-200 low noise, variable gain current amplifier. The voltage signal from the transimpedance amplifier was

digitized by a Keithley 2000 DMM. The dc voltage sources for the source reservoirs and the electrostatic gates were the models GS200 and 7651 from Yokogawa.

A.3. Simulation details

The simulation procedure employed in chapter 5 is roughly sketched out in the following, see [95] for details. We start the simulation with an initial guess for the electrostatic potential $\phi(\vec{r})$. The simulation is performed by solving the time-independent Schrödinger equation

$$H\Psi(\vec{r}) = E\Psi(\vec{r}), \tag{A.1}$$

with E being the eigenenergy, $\Psi(\vec{r})$ the electron wave-function and H the Hamiltonian

$$H = -\frac{\hbar^2}{2m}\nabla^2 + \phi(\vec{r}). \tag{A.2}$$

The eigenvalues and the corresponding eigenfunctions are used to calculate the new charge carrier density $\rho(\vec{r})$, which is inserted into the Poisson equation to calculate the updated electrostatic potential

$$\Delta\phi(\vec{r}) = \frac{\rho(\vec{r})}{\epsilon(\vec{r})}, \tag{A.3}$$

with the permittivity $\epsilon(\vec{r}) = \epsilon_r(\vec{r})\epsilon_0$. The potential $\phi(\vec{r})$ is again inserted into the Schrödinger equation. This process is repeated several times until the desired convergence and accuracy is reached. For a more stable convergence, the new potential $\phi_{out}^{(n)}(\vec{r})$ may be mixed with the previous potential $\phi_{in}^{(n)}(\vec{r})$

$$\phi_{in}^{(n+1)}(\vec{r}) = \phi_{in}^{(n)}(\vec{r}) + f\left(\phi_{out}^{(n)}(\vec{r}) - \phi_{in}^{(n)}(\vec{r})\right), \tag{A.4}$$

with n being the number of the current iteration and f the mixing factor determining the convergence and stability of the simulation [95].

A.4. Details on the fabrication

A.4.1. Hall bar samples

The fabrication of the Hall bar samples discussed in chapter 3 consists of the following steps:

1. Define the mesa region with optical lithography
2. Etch the mesa
3. Lift-off the resist covering the mesa
4. Define ion implantation regions for ohmic contacts with optical lithography
5. Ion implantation step including lift-off performed by Prof. K. Sawano at Tokyo City University
6. Define the bond pads with optical lithography
7. Metallize the bond pads with 20 nm Ti and 100 nm Au
8. Lift-off the metallized resist
9. Apply a 30 nm Al_2O_3 insulator layer using ALD
10. Define the accumulation gate with optical lithography
11. Metallize the accumulation gate with 20 nm Ti and 120 nm Au
12. Lift-off the metallized resist

A.4.2. DQD and ASD devices

The following steps are involved in the processing of the DQD device discussed in the chapters 4-6 and the ASD device discussed in chapter 7:

1. Define the mesa region with optical lithography
2. Etch the mesa
3. Lift-off the resist covering the mesa
4. Define ion implantation regions for ohmic contacts with optical lithography
5. Ion implantation step including lift-off performed by Prof. K. Sawano at Tokyo City University
6. Define the ohmic contact bond pads with optical lithography
7. Metallize the ohmic contact bond pads with 20 nm Ti and 100 nm Au
8. Lift-off the metallized resist

9. Apply a 20 nm Al_2O_3 insulator layer using ALD
10. Define the gate lines with optical lithography (LOR3A recipe)
11. Metallize the gate lines with 20 nm Ti and 100 nm Au
12. Lift-off the metallized resist
13. Define the dot-defining gates with EBL
14. Metallize the dot-defining gates with 5 nm Ti and 35 nm Au
15. Lift-off the metallized PMMA
16. Define the nano-magnet with EBL
17. Metallize the nano-magnet with 3 nm Ti, 50 nm Co and 3 nm Au
18. Lift-off the metallized PMMA
19. Apply a 80 nm Al_2O_3 insulator layer using ALD
20. Define the accumulation gates with EBL
21. Metallize the accumulation gates with 10 nm Ti and 80 nm Au
22. Lift-off the metallized PMMA
23. Etch the Al_2O_3 in the outer regions of the gate lines and the ohmic contact bond pads

A.4.3. Optical lithography recipe

The Hall bar sample structures discussed in chapter 3 as well as the outer DQD and ASD device structures such as the mesa, ion implantation regions, ohmic contacts and gate lines are fabricated using the technique of optical lithography.

1. Cleaning of the sample:
   - 5 min acetone bath
   - 1 sec ultrasonic bath (only for unstructured samples)
   - 1 min isopropanol bath
   - Blow sample with N_2 gun

2. Application of the photosensitive resist:
    - Set spinner to 8000 rpm, 30 sec and 2000 rpm/ sec acceleration
    - Place sample on cleaned vacuum chuck and turn on vacuum
    - Place one drop of Shipley S1813 or Shipley S1805 resist next to the sample and cover the sample with resist
    - Start spinner and wait for spinning to complete
    - Inspect the sample for inhomogeneities resulting in colored stripes. If no or little stripes are visible continue, else clean sample and repeat application of resist
    - Soft bake: Place sample for 4 min (S1813) or 2 min (S1805) on 90 °C hotplate
3. Expose the sample:
    - Load appropriate mask and sample into mask aligner
    - Align mask with sample and reduce distance of mask and sample
    - Expose sample with ultra violet (UV) light for 84 sec (S1813) or 42 sec (S1813)
4. Develop the exposed regions:
    - Prepare 20 ml of 1:3 AR300-26:H_2O developer in beaker
    - Stir beaker during developing on magnetic mixer
    - Open valve for cascade rinsing
    - Develop the sample for 40 sec(S1813) or 20 sec(S1805) with changing positions in beaker
    - Stop development process by cascade rinsing sample for about 10 sec
    - Inspect under microscope if exposed resist is completely removed, if not try a few seconds of post-developing
    - Hard bake for 3 min 35 sec on 120 °C hotplate (only prior to mesa or Al_2O_3 etching)

A.4.4. Gate lines with LOR3A resist

A very clean lift-off with no residual metal fringes left on the sample may be achieved with a layer of LOR3A resist placed below the photosensitive resist. This layer

of non-photosensitive LOR3A develops fast as soon as the photosensitive resist is fully removed. This leads to an undercut edge resulting in a clean lift-off after metallization.

- Cleaning of the sample:
  - 5 min acetone bath
  - 1 sec ultrasonic bath (only for unstructured samples)
  - 1 min isopropanol bath
  - Blow sample with N_2 gun
- Prebake at 120 °C for 5 min
- Application of the LOR3A resist:
  - Set spinner to 8000 rpm, 45 sec and 2000 rpm/ sec acceleration
  - Place sample on cleaned vacuum chuck and turn on vacuum
  - Place one drop of LOR3A resist next to the sample and cover the sample with resist
  - Start spinner and wait for spinning to complete
  - Inspect the sample for inhomogeneities resulting in colored stripes. If no or little stripes are visible continue, else clean sample and repeat application of resist
  - Bake LOR3A: Place sample for 4 min on 120 °C hotplate
- Proceed with the application of photosensitive resist and UV exposure.
- Develop the sample in MF-26A metel-ion free developer solution. The development time depends on the type of photosensitive resist used (25s for Shipley S1805)
- Avoid contact to acetone while LOR3A is present on the sample. The lift-off after metallization is performed in a 5 min 60 °C Remover PG bath.

A.4.5. Lift-off procedure

1. Place sample for 5 min in acetone bath (on 90 °C hotplate for PMMA lift-off) using syringe to squirt acetone at sample surface lifting-off resist (If using LOR3A recipe substitute acetone with Remover PG at 60 °C, see A.4.4)

2. Check sample under microscope (still immersed in acetone): if the entire resist is removed continue, else repeat the first step
3. Clean sample in 1 min isopropanol bath
4. Blow sample with N_2

A.4.6. Etching recipe

1. Prepare etching solution
   - Mesa etching:
     - Add 2 ml of hydrofluoric acid (HF) (40 %) to 158 ml of filtered H_2O
     - Mix 20 ml of resulting HF (0.5 %) with 90 ml of HNO_3 (96 %)
     - Stir the etching solution
   - Al_2O_3 etching:
     - Add 20 ml of HF (5 %) to 80 ml of filtered H_2O resulting in HF (1 %)
     - Stir the etching solution
2. Etch the sample:
   - Immerse sample in etching solution using tweezers for 1 min 30 sec (mesa etching) or 1 min 40 sec (Al_2O_3 etching)
   - Move sample through solution during the process for homogeneous etching
   - Stop etching in two consecutive H_2O baths
   - Clean of residual H_2O with N_2 gun

A.4.7. Metallization recipe

1. Prepare evaporation facility
   - Vent and open vacuum chamber
   - Load evaporation metals into thermal and electron beam evaporators
   - Close vacuum chamber and switch on rotary vane pump[1]
2. Remove SiO_2 oxide layer with HF-dip:
   - Add 10 ml of HF (40 %) to 70 ml of filtered H_2O resulting in HF (5 %)

[1] Only applies if SiO_2 needs to be removed i.e. when ohmic contact pads are applied

- Immerse sample for 30 sec in prepared HF

3. Mount the sample and evacuate the chamber:
   - Vent and open vacuum chamber
   - Mount the sample into vacuum chamber
   - Continue according to the evaporation manual to evacuate chamber
4. Evaporate required layers of metal (according to manual)
5. Vent the vacuum chamber and remove sample (according to manual)

A.4.8. Atomic layer deposition recipe

The insulator layers in this thesis have been applied in a Savannah ALD system.

1. Set process temperature to 300 °C
2. Use trimethylaluminium (TMA) as precursor
3. Select recipe for 20 nm of Al_2O_3 at 300 °C with 4 sec purge time
4. Adjust number of cycles according to desired insulator thickness where 200 cycles correspond to thickness of 20 nm

A.4.9. Electron beam lithography recipe

The inner DQD and ASD device structures, the depletion gate lines, the nano-magnet and the accumulation gate are fabricated using the EBL technique. Most of the EBL processing procedure was adapted from the description given in [96]. However, some parameters have been changed, which are covered in the following recipe:

1. Cleaning of the sample:
   - 3 min acetone bath on 150 °C hotplate
   - Transfer under isopropanol stream into 1 min isopropanol bath
   - Blow sample with N_2
2. Application of the resist:
   - Set spinner phases to:
     1) 800 rpm, 3 sec and 4000 rpm/ sec acceleration

2) 5000 rpm, 40 sec and 1000 rpm/ sec acceleration

- Blow unused glass pipette with N_2
- Suck small amount of PMMA into glass pipette with no air enclosed
- Start spinner and apply about 3 consecutive drops of PMMA during phase 1
- Wait for spinning to complete and inspect for inhomogeneities: If sample has even color continue, else clean sample and repeat application of resist
- Place sample on microscope slide and bake for 2 min on 150 °C hotplate
- Place sample on cool microscope slide to stop baking
- Spin-on experimental conductive resist from All-Resist for 50 sec at 4000 rpm with acceleration of 800 rpm/ sec
- Place the sample for 2 min on 90 °C hotplate

3. Build sample into SEM
4. Pump SEM chamber until pressure reaches 5×10^{-5} mbar
5. Set voltage to 25 kV, turn extra high tension (EHT) on and increase voltage to 30 kV in steps of 1 kV/ min
6. Set $z = 45.7$ mm and position over Faraday-cup
7. Use SE2 Detector and set working distance (WD) to 6.7 mm
8. Adjust the x- and y-aperture values using the wobble feature
9. Set stigmation values to $x = 8.3\,\%$ and $y = -1.8\,\%$
10. Position in middle of Faraday-cup hole and set to 1000 k× magnification
11. Measure beam current with eLitho program
12. Prepare eLitho files with structures to be written
13. Adjust the sample to eLitho coordinate system by moving to at least 3 alignment crosses and picking the corresponding points in eLitho (blank beam when moving between the crosses)
14. Set 200 k× magnification and position in spot where no structures are to be written

15. Set Spot option
16. Unblank beam for 10 sec to burn contamination dot and unset Spot option
17. Try to adjust WD and stigmation values until contamination dot is visible
18. If the dot is roundly shaped with a diameter in the order of a few 10 nm the SEM is adjusted correctly, else try burning another dot in 4 mm distance
19. Expose sample according to loaded eLitho file
20. Finer adjustment is done via adjustment marks patterned on sample in prior optical or electron beam lithography steps: In the adjustment dialog pick the marks appearing in the preselected unmasked areas
21. To achieve even finer adjustment, the above step may be performed with two separate sets of adjustment marks and masks
22. Remove sample from SEM
23. Immerse sample for 2 min in deionized H_2O if conductive resist has been used
24. Develop sample for 1 min 15 sec in AR 600-56 while rocking the beaker slightly
25. Dip the sample into isopropanol and blow with N_2
26. Bake for 1 min 30 sec on a 90 °C hotplate

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Acronyms

2DEG two dimensional electron gas. 7, 9, 10, 23, 24, 26–28, 47, 50, 88, 93

ALD atomic layer deposition. 23, 48, 108, 109, 113

ASD asymmetric sensing dot. 85, 87, 88, 90–96, 98–100, 106, 108, 109, 113, 129, III

CPMG Carr-Purcell-Meiboom-Gill. 79, 103

CS charge sensing. 47, 48, 50–53

CVD chemical vapor deposition. 102

DQD double quantum dot. 15–17, 47–54, 73, 98, 100, 103, 108, 109, 113

$E_{1st\ sb}$ energy of the first 2D subband. 26, 28, 30, 32, 39–41

E_F Fermi energy. 26, 30, 32, 38–41, 59

EBL electron beam lithography. 47, 49, 88, 89, 109, 113

EDSR electric dipole spin resonance. 3, 18, 19, 47, 66, 71, 73, 74, 81, 102

EHT extra high tension. 114

HEMT high electron mobility transistor. 84–86

HF hydrofluoric acid. 112, 113

LED light-emitting diode. 38–44, 93

MBE molecular beam epitaxy. 2, 21–23, 45, 47, 66, 71, 101, 102

MIT metal-insulator transition. 30, 39, 41

MOS metal oxide semiconductor. 2, 68, 71

MW microwave. 18, 73–76, 106

n_{QW} 2D charge carrier density in the QW. 26, 30, 32

n_{sat} saturation density. 30

NMR nuclear magnetic resonance. 76, 79

PMMA poly(methyl methacrylate). 49, 109, 111, 114

QD quantum dot. 2, 10, 13–16, 18, 19, 23, 40, 45, 47, 49, 50, 52–54, 57, 59, 62, 63, 71, 74, 83–88, 90, 92–95, 98, 99, 101, 103

QW quantum well. 2, 5, 7, 8, 21, 23, 24, 26–30, 32, 35, 39–43, 45, 47, 52, 64–66, 70, 71, 77, 81, 93, 102, 128

SdH Shubnikov-de Haas. 26, 28

SEM scanning electron microscopy. 47–50, 74, 88–90, 92, 100, 114, 115

SET single electron transistor. 47, 50–52, 83

SNR signal-to-noise ratio. 2, 3, 83–85, 100, 103

SQD single quantum dot. 10–18, 47, 50–54, 57, 58, 60, 61, 74, 83–85, 98, 101, 102

TEM transmission electron microscopy. 66

UHV ultra high vacuum. 21

UV ultra violet. 110, 111

VS virtual substrate. 23

WD working distance. 114, 115

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