Array stamping of carbon nanotubes and quantum transport in low-dimensional carbon nanotube-TMDC devices



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List of Abbreviations

0D	zero-dimensional			
1D	one-dimensional			
2D	two-dimensional			
3D	three-dimensional			
2DEG	two-dimensional electron gas			
ABS	Andreev bound state			
\mathbf{AC}	alternating current			
AFM	atomic force microscope			
ALD	atomic layer deposition			
BCS	Bardeen-Cooper-Schrieffer			
BKT	Berezinskii–Kosterlitz–Thouless			
\mathbf{BZ}	Brillouin zone			
CB	Coulomb blockade			
сс	contact configuration			
CDW	charge density wave			
CNT	carbon nanotube			
\mathbf{CPS}	Cooper pair splitter			
CVD	chemical vapor deposition			
\mathbf{CVT}	chemical vapor transport			
DC	direct current			
DOS	density of states			
EBL	electron beam lithography			
\mathbf{ED}	electron diffraction			
\mathbf{GL}	Ginzburg and Landau			
GPIB	general purpose interface bus			
HS	hot spot			
$\mathbf{J}\mathbf{J}$	Josephson junction			
\mathbf{MF}	Majorana fermion			

MFC	mass flow controller			
MIBK	methyl isobutyl ketone			
MWCNT	multi wall carbon nanotube			
OL	optical lithography			
\mathbf{PC}	polycarbonate			
PDMS	polydimethylsiloxane			
PECVD	plasma-enhanced chemical vapor deposition			
PMMA	polymethyl methacrylate			
\mathbf{PS}	phase slip			
PSC	phase slip center			
\mathbf{PSL}	phase slip line			
$\mathbf{Q}\mathbf{D}$	quantum dot			
QPS quantum phase slip				
RF radio frequency				
RIE reactive ion etching				
SB Schottky barrier				
\mathbf{SBT}	Skocpol, Beasly and Tinkham			
SEM	scanning electron microscope			
SET	single electron transistor			
SO	spin-orbit			
SOC	spin-orbit coupling			
SOI	spin-orbit interaction			
\mathbf{STM}	scanning tunneling microscope			
SWCNT	single wall carbon nanotube			
\mathbf{TB}	tight binding			
TEM	transmission electron microscope			
TMDC	transition metal dichalcogenide			
\mathbf{TV}	television			
UV	ultraviolet			
vdW	van der Waals			

1. Introduction

Although several groups have reported on carbon nanotube (CNT) structures since 1952 [2, 3, 6, 10, 16, 22], Iijima's investigation in the 1990s is generally considered to be the birth of CNT research. In 1991, he first analyzed in detail the helix structure of the multi-walled [23, 24], and two years later the single-walled form via electron diffraction (ED) and high resolution transmission electron microscope (TEM) images [27, 28]. Since then, they where studied excessively in theoretical and experimental works. Due to their extraordinary properties, mostly dictated by their structural geometry, they are of great interest to science [29, 45, 48, 54, 58, 82, 123, 186, 215] and industry alike [159].

CNTs combine properties of two-dimensional (2D) graphene with their one-dimensional (1D) structure and represent the prototype of a 1D quantum wire. Graphene is a zero-gap semiconductor [80, 120, 203], whereas CNTs are either metallic or semiconducting with varying band gaps depending on their chiral index [58, 109]. They have a high tensible strength and Young's modulus up to 1 TPa [33, 58, 95]. In absence of scattering, CNTs can stand incredible high current densities of almost a billion $\frac{A}{cm^2}$ [56]. Several experiments on quantum dot (QD) devices based on CNTs attached with normal [83], ferromagnetic [88, 143, 179, 181] and superconducting contacts [180, 206] were reported. In such experiments effects as Fabry Perot [63, 199] and Kondo physics [75, 133, 230], noise measurements [230, 233, 260] and nanomechanics [105, 231] were reported. Furthermore, Cooper pair splitters (CPSs) can be realized [121].

Majorana fermions (MFs) are particles which are identical to their antiparticles and are predicted to appear pairwise in topological superconductors. Theoretically, particles of Majorana character were predicted as early as 1937 and they are promising candidates in fault-tolerant quantum computing applications [19, 249, 258]. Since then, promising material systems, that can host MFs, have been sought. First of all, different layouts of inorganic nanowires in close proximity with a superconductors were proposed [60, 124, 140]. In parallel, also setups using CNTs, as genuinely 1D quantum nanowires, were considered as hosts of MFs at the ends of the tube when proximitized with a superconductor [142, 157, 238, 269]. For this purpose, the CNT has to be driven into a topological superconducting state by means of a magnetic field. A potential nominee as a superconductor is NbSe₂, a member of the transition metal dichalcogenide (TMDC) family. Only a few years ago, it was demonstrated that even monolayers of this material [205] as well of MoS₂ [187] can stay or become superconducting. They exhibit large spin-orbit interaction (SOI), high critical temperatures and a large mean free path. Due to their 2D nature and Ising superconductivity, these material can stand in-plane field much larger than the Pauli limit. In addition to it, the superfluid density and hence the quantum phase slips (QPSs) rate in 1D superconductors can be tuned by electrostatic gating due

1. Introduction

to decreased area charge density [204, 275].

A landmark in the experimental access to this kind of particles was the work of Mourik et al. in 2012 [145]. They used an InSb nanowire with a normal conducting Au and a superconducting NbTiN contact and fabricated some side gates to define tunnel barriers. This allowed the detection of a bound midgap state starting at 100 mT, which was persistent against the influence of magnetic field and gate voltage. The importance of topological effects can be seen in the award of the Nobel Prize to the physicists Thouless, Haldane and Kosterlitz in 2016 for their pioneering work in areas of topological states of matter and topological phase transitions [212].

In the first part of this work, a new fabrication method for the production of CNT based QDs is developed. We call it *array stamping* since an array of 45 double plateau structures over which CNTs have been grown are stamped on 45 electrode structures prefabricated on another chip in one go. The separation of growth and electrode fabrication allows clean suspended CNT QD devices with high device yield.

In the second part of this work, essential building blocks on the way to a MF detection device were realized according to the in-house theoretical proposal of Marganska et al. [238]. Therein, the emergence of Majorana quasiparticles at the end of a CNT proximitized by 2D NbSe₂ under the influence of a large magnetic field was predicted. We combine 1D CNT growth with mechanically exfoliated 2D van der Waals (vdW) flakes to form a hybrid device. It could be tuned into a topological non-trivial phase by a magnetic field and by tuning the chemical potential μ via electrostatic gating.

In the third part, a 1D nanowire in NbSe₂ flakes was realized using electron beam lithography (EBL) and reactive ion etching (RIE). Since the discoveries of Paradiso et al. [255] phase slip lines (PSLs) in NbSe₂ are well known. The constriction is thought to allow a deliberate control of the site at which PSLs preferentially nucleate.

This thesis is structured as follows. The theoretical background is laid in chapter 2. The basic experimental fabrication and measurement techniques are introduced in chapter 3. Chapter 4 presents the newly developed *array stamping technique* for CNTs. In the following chapter 5, fabrication techniques specific to the assembly of CNT-vdW heterostructures are depicted. The improvements in sample fabrication and measurement results of the CNT-NbSe₂ hybrid devices are recorded in chapter 6. Chapter 7 presents the results on the constrictions patterned in NbSe₂. In the end, chapter 8 summarizes the main results of this thesis. All relevant fabrication details, further developed techniques and other measurement results of additional samples are summarized in appendix A to D.

In this chapter, the basic theoretical background is delineated. We first discuss the different ingredients separately and then combine them to our hybrid devices. Various vdW materials (graphene, hBN, NbSe₂) are introduced in section 2.1. Basic properties of CNTs are envisioned in section 2.2. Thereafter, various transport regimes are reviewed in section 2.3. A detailed overview of MFs in CNTs is given in section 2.4. In section 2.5, we present the theory on resistive states in superconductors.

2.1. Two-dimensional van der Waals materials

Graphite, BN and TMDCs are layered materials with strong in-layer bonds and weak inter-layer vdW interaction. Therefore, they can be thinned down to the monolayer by mechanical or wet-chemical exfolation. On the other hand, these materials can be synthesized over large areas by heating solid starting materials on suitable substrates [139, 149]. The material properties of the three-dimensional (3D) and 2D variants sometimes differ considerably [203].

TMDCs are materials of the type MX₂, where "M" stands for a transition metal (e.g. Ti, Zr, Hf, V, Nb, Ta, Mo, W) and "X" for a calcogen (e.g. S, Se, Te). A layer of the bulk material consists of a sequence X-M-X and the planes of the X-atoms each form a hexagonal structure. TMDCs can be metallic (NbX₂, TaX₂) or semiconducting (MoX₂, WX₂). Their physical properties show a high dependence on the layer number (indirect or direct band gap, value of the critical temperature in superconductors) [149, 191]. In undoped metallic TMDCs the Fermi energy is always in a d-band. Therefore, the electrons flow predominantly in the metal layers. Phase transitions occur in these materials because the density of states (DOS) is quite high at the Fermi level [203].

New functional materials are created when layers of different materials are stacked to form so-called vdW heterostructures. Since metallic monolayers in particular are generally very reactive and corrode in comparison to their 3D counterparts, exfoliation and stacking should take place in an inert atmosphere or in a high vacuum, in the dark and at low temperatures, if possible, to avoid contamination. Unstable materials degrade less or only on long time scales when encapsulated in inert materials. In order to be able to contact the relevant positions electrically, a depth-selective RIE is necessary. Depending on the stacking angle, different crystals with similar lattice constants can show a surface reconstruction (e.g. a Moiré pattern in hBN and graphene) [136, 154, 219, 251]. Heterostructures allow the fabrication of devices with outstanding properties that their individual components do not have [223].

2.1.1. Graphene

A C atom has six electrons. Two of them are strongly bound in the 1s² orbitals as inner electrons, whereas the four others are less strongly bound in the 2s² and 2p² orbitals as visualized in figure 2.1(a). Since the energy difference between the 2s and 2p orbitals is small, the electronic wave functions of the four outer electrons can mix as depicted in figure 2.1(c). A spⁿ hybridization means that the electronic wave functions of a 2s electron and $n \in \{1, 2, 3\}$ $2p_{x,y,z}$ electrons mix resulting in a linear, planar or tetragonal geometry [1, 58].

The 3D C modification graphite consists of 2D graphene layers weakly bound by vdW forces with an interlayer spacing of ~ 0.34 nm. Figures 2.1(b,d) show a graphene sheet where the C atoms are due to the sp² hybridization arranged in a honeycomb structure and strongly covalently bonded with a nearest neighbour distance of $a_{\rm CC} = 1.421$ Å and an in-plane lattice constant $a_0 = a_{\rm CC}\sqrt{3} = 2.462$ Å. Figure 2.1(b) shows the orientation of the two different kind of bonds. There are σ -bonds (overlap of two sp²-orbitals) along the connecting line of neighboring atoms forming the hexagonal network and π -bonds (delocalized electrons of the p_z orbitals). As the binding σ - and the anti-binding σ^* -bands have their smallest energy gap of about 11 eV at the Γ -point, they can in many cases be neglected in band structure calculations whereas the π/π^* -bands contribute to electric transport [1, 95, 109]. Furthermore, the mixing of π and σ orbitals in CNTs due to curvature can be neglected at first approximation [25].

Figure 2.1(d) shows that the graphene unit cell (gray rhombus) contains two C atoms and it is spanned by the two graphene base vectors

$$\vec{a}_1 = a_0 \begin{pmatrix} \frac{\sqrt{3}}{2} \\ \frac{1}{2} \end{pmatrix}$$
 and $\vec{a}_2 = a_0 \begin{pmatrix} \frac{\sqrt{3}}{2} \\ -\frac{1}{2} \end{pmatrix}$. (2.1)

The corresponding reciprocal vectors are given by

$$\vec{b}_1 = \frac{2\pi}{a_0} \begin{pmatrix} \frac{1}{\sqrt{3}} \\ 1 \end{pmatrix}$$
 and $\vec{b}_2 = \frac{2\pi}{a_0} \begin{pmatrix} \frac{1}{\sqrt{3}} \\ -1 \end{pmatrix}$, (2.2)

where $\vec{a}_i \cdot \vec{b}_j = 2\pi \delta_{ij}$. Figure 2.1(d,e) shows a comparison of the graphene real and reciprocal lattice. The latter also shows a hexagonal symmetry but it is rotated for 90° with respect to the real space lattice [58, 95, 109].

The band structure of graphene can be calculated in tight-binding approximation and the dispersion relation then reads

$$E(k_x, k_y) = \pm \gamma_0 \sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_x a_0}{2}\right)\cos\left(\frac{k_y a_0}{2}\right) + 4\cos^2\left(\frac{k_y a_0}{2}\right)}, \qquad (2.3)$$

where $\gamma_0 = 2.5 \text{ eV}$ denotes the overlap integral between nearest neighbors [58, 95]. The graphene dispersion relation is plotted in figure 2.1(f). Note that the bonding/antibonding π/π^* (negative/positive energy) bands touch each other at the inequivalent

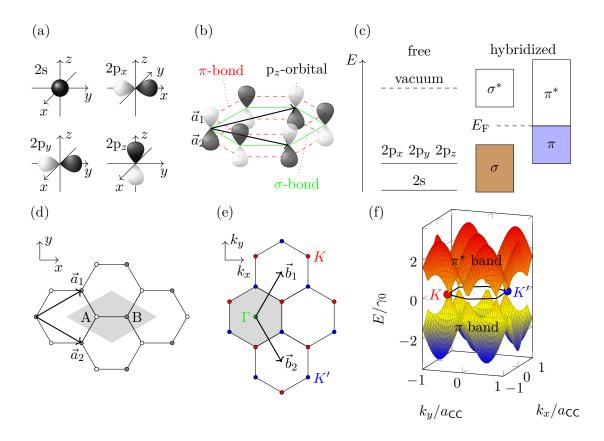


Figure 2.1.: (a) Electronic orbitals of atomic C. In the black (white) drawn orbital lobes, the wave function is negative (positive). (b) σ/π bonds and orientation of p_z orbitals in hexagonal graphene lattice. \vec{a}_1 and \vec{a}_2 denote the basis vectors of real space. (c) Schematic energy diagram atomic (left) and sp² hybridized (right) C. (d) Graphene lattice in the real space. A and B denote the C atoms of the two sublattices. The gray shaded rhombus corresponds to the graphene unit cell. (e) The reciprocal lattice also has a honeycomb structure, which is rotated relative to that of the real space by 90°. \vec{b}_1 and \vec{b}_2 are the reciprocal graphene basis vectors. The hexagon filled in gray corresponds to the first graphene Brillouin zone. (f) Graphene energy dispersion relation of the p_z electrons. The π/π^* conduction/valence bands touch each other at the six K/K' points. Near the Dirac points, the dispersion is linear. Drawn according to [58, 95, 109, 186].

K/K' points (Fermi level) that are energetically degenerated. There the DOS is zero. In the vicinity of the K/K' points, a linear dispersion relation

$$E = \pm \hbar v_{\rm F} \left| \vec{\kappa} \right| \tag{2.4}$$

holds, where $v_{\rm F} \approx 8 \times 10^5 \, \frac{\rm m}{\rm s}$ is the Fermi velocity, $\vec{\kappa}$ is a wave vector near the K/K' points and \hbar is the reduced Planck constant. The plus and minus signs stand for electrons and holes respectively [186]. In undoped graphene and at $T = 0 \,\rm K$ the bonding π -bands are completely filled, the DOS disappears at the Fermi level. Therefore, graphene is also called zero-bandgap semiconductor. The reason for the energetic degeneration of the K/K' points is the symmetry of the hexagonal lattice [91].

Furthermore, it was shown that graphene samples, when encapsulated with hBN, exhibit better transport properties as well as longer lifetime [170, 232].

2.1.2. Hexagonal boron nitride

HBN is very similar to graphite and, like it, consists of 2D layers in which the B and N atoms are arranged alternately in a regular hexagonal structure and joined by strong covalent sp^2 bonds (see figure 2.2(a)) [93, 130, 153]. The material is mechanically and

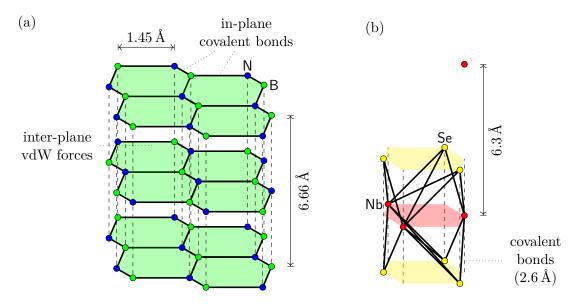


Figure 2.2.: (a) Structure of a sequence of three hBN sheets. (b) Trigonal prismatic structure of a NbSe₂ monolayer. The honeycomb lattice is formed by the Nb and Se sublattices. Drawn according to [12, 163, 190].

chemically stable under ambient conditions and has an atomically smooth surface with neither dangling bonds nor charge traps. It is an ideal insulator due to its bandgap in the order of ~ 6 eV and it resists high electric fields with ~ 0.5 V per crystal layer corresponding to ~ 1.2 $\frac{V}{nm}$ [183]. Therefore, it is excellent as thin dielectric for capacitively

coupled gates [164, 203, 222]. Furthermore, this material has a rather large thermal conductance [162, 163]. It is an excellent substrate for graphene and CNT samples [154]. Transistors with highest mobility can be built from graphene completely encapsulated with hBN [162, 203]. In addition, CNTs are grown by chemical vapor deposition (CVD) on hBN flakes to avoid electrical potential fluctuations and interactions with the underlying substrate [165, 210]. Since the lattice constants of hBN and graphene are nearly identical. the band structure of graphene is not disturbed when encapsulated [118, 203]. Using Raman or photoluminescence measurements, the number of layers of a vdW crystal thinned by mechanical exfoliation can be determined non-invasively [235]. If certain vdW materials, such as NbSe₂, oxidize easily under ambient conditions, a coverage with hBN from top may slow down the oxidation process [225, 243]. But only a complete encapsulation with hBN from above and below can provide complete air tightness. If a flake on a substrate is only protected with hBN from above, this does not provide a complete seal against O_2 possibly due to the roughness of the SiO₂ surface [251]. Note that also an encapsulation with graphene can retain the superconducting properties of NbSe₂ [216]. Also hBN tunnel barriers to CNTs were reported [192].

HBN has a minimum relative permittivity of 4 when combined with a Au topgate [172]. A thus estimated tuning range of ~ 18 meV of the chemical potential is on the one hand much smaller as reported in reference [204], but seems to be sufficient for our aim (see reference [238]), on the other hand.

For this thesis, crystals grown by Kenji Watanabe and Takashi Taniguchi [100] or commercially purchased from HQ graphene are used.

2.1.3. Niobium diselenide

We deal with 2H-NbSe₂ which has a trigonal prismatic phase (2H). We will omit the "2H" in the following. One layer consists of a sequence of Se-Nb-Se sheets. This leads to a trigonal prismatic unit cell, as depicted in figure 2.2(b). The 2 in the above name indicates that there are two metal atoms in the unit cell and H specifies the hexagonal geometry [203, 220]. In the bulk crystal, individual NbSe₂ layers are stacked in an ABAB scheme [7, 150]. NbSe₂ is a hole-metal at room temperature. The strong in-plane covalent bonds are between the d/p orbitals of transition metal/chalcogen atoms, respectively [209, 220, 265].

In contrast to graphene, the electronic spectrum in NbSe₂ is gapped [208]. NbSe₂ is an anisotropic s-wave type II superconductor. In its bulk form, it has a critical temperature of 7.2 K and a superconducting gap of 1.24 meV [17, 150]. The critical temperature decreases with reducing the number of layers. Nevertheless, also the monolayer stays superconducting [12]. However, the exact value depends strongly on the respective sample and the number of defects [190, 205, 221, 244]. When going to fewer layers the superconducting transition broadens due to the enhanced thermal fluctuations in 2D [205].

Since NbSe₂ shows strong spin valley locking (spins forced out-of-plane, opposing alignment in adjacent valleys), it can stand in-plane magnetic fields of at least 30 T [151, 205, 224, 238]. Furthermore, NbSe₂ exhibits charge density waves (CDWs) at ~ 145 K

in the monolayer compared to ~ 33 K in the bulk [64, 156, 216, 239]. Both, CDWs and superconductivity can coexist and compete at low temperatures [64, 203, 229]. CDW order as well as superconductivity can be increased/decreased by raising/reducing the carrier density in 2D NbSe₂ using ionic liquid gating giving rise to a variation of the electron-phonon coupling strength and the DOS. The value of T_c can thus be varied up to ~ 50%. Xi et al. reported that it is possible to tune the chemical potential in bilayer NbSe₂ via ionic liquid gating since the charge carrier density and the associated screening currents are significantly smaller than in the bulk. The charge carrier density could thus be modulated to about 30% [204].

Under ambient conditions, $NbSe_2$ oxidizes, causing crystal defects that impair the superconducting properties [221]. The defects are formed when O_2 interacts with the crystal under the influence of light [11]. To avoid the oxidation of $NbSe_2$, we store it exclusively in a dark container filled with N_2 gas and process it only in N_2 atmosphere. After the exfoliation of $NbSe_2$, it is fully (partially) encapsulated with hBN, which creates an (almost) air-tight protection from O_2 [251].

Due to its geometry, $NbSe_2$ has an out-of-plane mirror symmetry and broken in-plane inversion symmetry [202]. Electrons in opposite K valleys in monolayer TMDCs experience opposite effective Zeeman fields, so-called Ising spin-orbit coupling fields. Electrons are forced to spin in an out-of-plane direction and thus causing Ising superconducting states. The upper critical field is significantly increased. Figure 2.3 illustrates the alignment of spin and magnetic field. As a consequence, the formation of Cooper pairs between

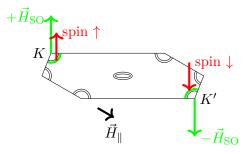


Figure 2.3.: Ising coupling in a monolayer NbSe₂. The Fermi surface for NbSe₂ is shown for the crystal. The spins of electrons located at K and K' are coupled to the out-of-plane spin-orbit field $\pm H_{\rm SO}$. Even large in-plane fields \vec{H}_{\parallel} cannot break this Ising-coupling. The double Fermi surface in the image stands for the two spins. The inner surface at Kis for spin down, the outer for spin up and vice versa in the valley K'. The Se atoms contribute very little to the bands at the Fermi level, so they are usually neglected. Drawn according to [202].

electrons of opposite pockets with opposite spin polarization is favored (Ising pairing) and protects the superconducting state from pair-breaking induced by an in-plane field

 $\dot{H_{\parallel}}$. Therefore, superconductivity survives well above the Chandrasekhar-Clogston limit

$$H_{\parallel}^{\rm lim} = \frac{\Delta_0}{\sqrt{2\mu_{\rm B}}}.\tag{2.5}$$

In principle, this spin-momentum-locking and Ising superconductivity can be lifted for even numbers of layers, where inversion symmetry and spin degeneracy are restored. In practice, coupling between layers is so small that they behave essentially as a stack of monolayers. Therefore, violation of the Chandrasekhar-Clogston limit has been observed up to eight layers and beyond [205]. In type-II superconductors, Cooper pairs are broken by a magnetic field. On the one hand, the magnetic field couples to the momentum of the electrons (orbital effect). On the other hand, the Pauli spin paramagnetic effect can also come to light, whereby the electron spins are aligned in parallel. For the latter, high in-plane magnetic fields are necessary, $\sim 30 \text{ T}$ for NbSe₂ and $\sim 50 \text{ T}$ for gated MoS₂. In 2D superconductors, an in-plane magnetic field should not evoke vortices, thus suppressing the orbital effect [202]. In reference [202], the critical field is up to six times larger than the calculated Pauli limit. This results from the intrinsic spin-orbit coupling (SOC) which yields an effective magnetic field

$$\vec{H}_{\rm SO}(\vec{k}) \propto \vec{k} \times \vec{\varepsilon},$$
(2.6)

where $\vec{\varepsilon}$ is the crystal field. Hence, the spin will be oriented out of plane. The Zeeman field takes opposite directions in opposite corners of the hexagonal Brillouin zone (BZ). The Ising pairing is thus the cooper pair formation between electrons of opposite valleys with opposite spin polarizations. The superconducting state is protected since the Ising pairing prevents the alignment of the spin to in-plane magnetic fields.

The encapsulation of NbSe₂ not only with hBN but also with MoS₂ was reported. The number of layers can be detected via Raman spectroscopy [204]. Usually, as the thickness of superconducting films decreases, their superconductivity is destroyed. This can be caused by either an attenuation of the Coulomb screening or the localization of Cooper pairs at impurity sites. In reference [234], a reduction of the superconducting gap Δ and critical temperature T_c , both $\propto 1/N$, was observed while reducing the number of layers N from 50 down to the monolayer NbSe₂. This is explained by a change in band structure while decreasing the layer number. The monolayer often has its problems with contaminants, defects or oxidation giving rise a large variety in reported values for T_c in the monolayer case. Hence, surface effects become more and more important when reducing the sample thickness.

It has been reported that the growth of mono- and few layer NbSe₂ by means of CVD is possible. But since the resulting films show a critical temperature of $T_c \approx 1 \text{ K}$, it is very likely that the formation of the superconducting phase is suppressed by impurities introduced during the growth process [221]. In contrast to this, the deposition of Si adatoms to a pristine NbSe₂ flake can improve the superconducting characteristics up to a maximum before deteriorating again [265].

For this thesis, NbSe₂ crystals commercially purchased from HQ graphene were used.

2.2. Carbon nanotubes

2.2.1. Geometry and electronic structure of carbon nanotubes

Figure 2.4 shows that one can imagine an ideal single wall carbon nanotube (SWCNT) as a graphene sheet seamlessly rolled up into an (infinitely long) cylindrical shell with a diameter in the nm range and a length of μ m [40, 90]. Since there are theoretically infinite possibilities to roll up a graphene sheet borderless, there are also infinite numbers of CNT geometries. A multi wall carbon nanotube (MWCNT) corresponds to a coaxial

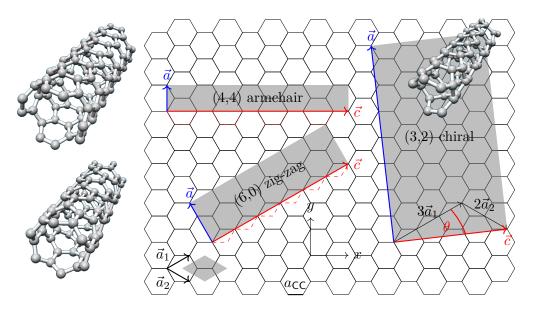


Figure 2.4.: In a graphene layer, the C atoms are arranged hexagonally. The basis vectors are denoted by \vec{a}_1 and \vec{a}_2 . Unit cells are shown as gray rectangles for three different CNTs, which can be thought of as graphene rolled up in different ways. The chiral vector \vec{c} corresponds to the circumference of the nanotube. The vectors $\vec{a} \perp \vec{c}$ correspond to the shortest period in the axial tube direction. The chiral angle θ is the angle between the zig-zag direction and the chiral vector \vec{c} . Drawn according to [95, 109].

assembly of multiple SWCNTs [68, 95]. Their typical diameter ranges from 10 to 20 nm and the intertube distance is ~ 3.4 Å, which is the distance between two graphene layers in graphite [58, 169]. In the following, we will only consider SWCNTs if not mentioned otherwise.

The geometry of a CNT is entirely determined by its *chiral vector*

$$\vec{c} = n\vec{a}_1 + m\vec{a}_2, \tag{2.7}$$

which is a linear combination of the graphene basic vectors \vec{a}_1 and \vec{a}_2 . The two-tuple (n,m) with $n,m \in \mathbb{Z}$ is called *chiral index* [46]. Parameters like the spin-orbit gap or the magnetic flux crucially depend on the structural properties of the CNT [186]. The

diameter of a CNT d_{CNT} can be calculated using equation (2.8).

$$d_{\rm CNT} = \frac{|\vec{c}|}{\pi} = \frac{\sqrt{3}a_{\rm CC}}{\pi}\sqrt{m^2 + mn + n^2}$$
(2.8)

The angle

$$\theta = \tan^{-1} \left(\frac{\sqrt{3}n}{2n+m} \right) \tag{2.9}$$

between the chiral vector and the zig-zag direction is called *chiral angle*. For reasons of symmetry, one can limit it to angles between 0 and 30°. Table 2.1 illustrates the relationship between chiral angle and chiral index [58]. The chiral index can be determined

Table 2.1.: Relationship between chiral index and chiral vector for some special graph grid directions.

direction	zig-zag	armchair	chiral
chiral angle	$\theta = 0^{\circ}$	$\theta = 30^{\circ}$	$0^{\circ} < \theta < 30^{\circ}$
chiral index	(n, 0) or $(0, m)$	(n,n)	(n,m) where $n \neq m$

by Raman spectroscopy [59, 155, 188, 211] or from transport measurements [199]. *Chiral* in this case means that the original and the mirror image of the structure are not identical [40]. The atomic structure of CNTs can be investigated using scanning tunneling microscope (STM) or TEM techniques [90, 95, 186].

The 1D unit cell of a CNT is defined by the vectors \vec{c} and \vec{a} where

$$\vec{a} = \frac{2m+n}{d_{\rm R}}\vec{a}_1 - \frac{2n+m}{d_{\rm R}}.$$
 (2.10)

Here $\vec{a} \perp \vec{c}$ is the shortest vector parallel to the CNT axis which defines the lattice translation in this direction. $d_{\rm R}$ denotes the greatest common of (2m+n) and (2n+m) [40, 109]. The number $N_{\rm C}$ of C atoms in the CNT unit cell is given by twice the number of graphene unit cells inside the CNT unit cell [186], where

$$N_{\mathsf{C}} = 2\mathcal{Q} = 2\frac{|\vec{c} \times \vec{a}|}{|\vec{a}_1 \times \vec{a}_2|} \tag{2.11}$$

holds. Thus there are $N_{\rm C}$ bonding/anti-bonding π/π^* electronic energy bands [40]. Real CNTs however, naturally have a finite length, show defects and interact with their environment [58].

The CNT band structure can be calculated in the simplest form in the so-called *zone* folding approximation. The graphene sheet is rolled up and the electron wave vector in circumferential direction is quantized. This means that only certain values are allowed depending on the chiral index. Whenever the graphene K-point lies on these lines, it is a metallic CNT with a non-zero density of states at the Fermi level. Otherwise, it

is a semiconducting system, where the value of the band gap can vary up to ~ 1 eV. Armchair CNTs (n, n) are always metallic. Other nanotubes (n, m) with n - m = 3jwhere $j \neq 0, j \in \mathbb{Z}$ are semiconducting [58]. If the radius of a CNT is smaller than 1 nm, the σ/π bands rehybridize and change the electronic structure. This can also happen by bending a CNT [58]. The quantization in circumferential direction reads

$$k_{\perp} = \vec{k} \cdot \vec{c} = 2\pi q, \qquad q \in \mathbb{Z}. \tag{2.12}$$

In the axial direction, k_z is continuous if one assumes an infinite CNT. Equation (2.12) defines a discrete number of equidistant lines with a separation of $2d_{\rm CNT}$ which correspond to the allowed modes in the reciprocal space and the 1D subbands along the CNT axis [95]. This is visualized in figure 2.5. When $K_{\rm gr}$ and $\Gamma_{\rm CNT}$ coincide, the corresponding CNT

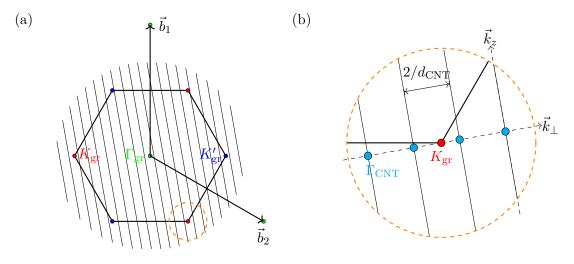


Figure 2.5.: Schematic sketch of the zone folding approximation. (a) First Brillouin zone of graphene with allowed k-lines of a CNT. \vec{b}_1 and \vec{b}_2 are the reciprocal graphene lattice vectors. (b) Enlarged clip of the region of subfigure (a) around the graphene $K_{\rm gr}$ point (marked with the dashed orange circle). \vec{k}_z and \vec{k}_{\perp} are the reciprocal CNT vectors. The cyan circles indicate the CNT $\Gamma_{\rm CNT}$ point. Since $K_{\rm gr}$ and $\Gamma_{\rm CNT}$ are not located on top of each other, the sketched situation corresponds to a semiconducting CNT. Drawn according to [109].

is metallic, otherwise semiconducting. This corresponds to the condition that (n-m) must be a multiple of three.

One can deduce the DOS of a CNT from its energy dispersion [44, 91]. Figure 2.6 shows the energy dispersion relation together with its corresponding density of states for different types of CNTs. In real life, even metallic CNTs show a small bandgap (up to 10 meV) due to strain and curvature. K/K' points move in opposite direction. Only armchair CNTs remain fully metallic. Both nanofabrication and mechanical deformation can cause disorder and thus non-reproducible sample characteristics. For each state in K there is a time-reversed state in K'. Time-independent perturbations like curvature

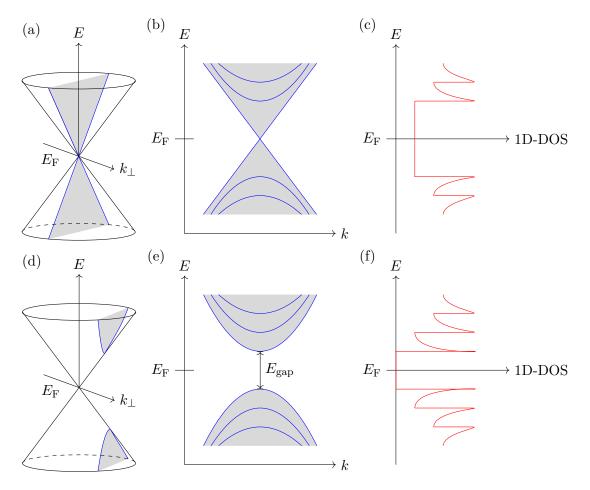


Figure 2.6.: Schematic sketches of the allowed k-values, the energy dispersion relation with its corresponding density of states for a metallic (a,b,c) and a semiconducting (d,e,f) CNT. (a,d) The gray-filled areas inside the cones indicate the allowed k-values. (b,e) Energy dispersion relation. (c,f) Corresponding 1D DOS. Drawn according to [95, 186].

or strain cannot cancel this degeneracy but for example a magnetic field can [186]. Graphene shows a rather weak SOC. But due to the curvature, the z inversion symmetry in CNTs is broken and thus CNTs can show strong SOC with a binding energy in the few meV regime. Figure 2.7 shows that this symmetry breaking results from the fact, that neighboring p_x and p_z are no longer orthogonal to each other [106, 186]. SOC in

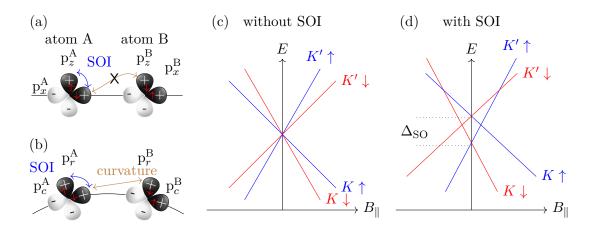


Figure 2.7.: (a) In-plane configuration as in graphene. The red arrows indicate the spin. (b) Curvature enhanced SOC in CNTs. In CNTs, the mirror symmetry is broken compared to graphene. Expected spectra in parallel magnetic field (c) without and (d) with SOC. In the latter case, a gap Δ_{SO} in the spectrum is formed. Drawn according to [186].

CNTs was theoretically predicted already in 2000 [52]. The inherent atomic SOC of a C atom in plane graphene (see blue double arrow in figure 2.7(a,b)) results in a mixing of the $|p_x^A\rangle$ and $|p_z^A\rangle$ orbitals. If now the graphene flake is bent, hopping between adjacent $p_x^{A\uparrow}$ and $p_z^{B\downarrow}$ orbitals (brown double arrow) is no longer forbidden resulting in SOC in the π -bands. Between $|p_r^A\rangle$ and $|p_r^B\rangle$, one receives a direct and a spin-flip term in the effective hopping matrix element. By applying a magnetic field β_{SO} along the CNT axis, one can detect a spin-orbit (SO) splitting of

$$\Delta_{\rm SO} = g_s \mu_{\rm B} \beta_{\rm SO} \tag{2.13}$$

of the two spin states accompanied with a transformation from a four-fold degeneracy (spin and valley) without SOC to a two-fold degeneracy. Orbital and spin magnetic moments of CNTs can be examined in excited-state spectroscopy of the first electron shell of an ultraclean CNT [87, 106, 186]. Figures 2.7(c,d) show the resulting change in the band structure around the Dirac points depending on an externally applied magnetic field \vec{B}_{\parallel} along the axis of the CNT. Note that due to the SOC, even armchair CNTs show a small bandgap at $B_{\parallel} = 0$ [160]. For a more detailed overview of SOC in CNTs see [186].

2.2.2. Superconductivity in carbon nanotubes

A CNT, which is not superconducting per se, can indeed exhibit superconducting properties if it is brought into the vicinity of a superconductor [158]. Morpurgo et al. reported in 1999 [51] that in a SWCNT contacted with Nb/Au in QD configuration, superconducting correlations can be controlled as Andreev reflection using a gate electrode. Andreev reflection occurs when an electron from a normal conductor wants to penetrate into a superconductor and its energy is smaller than the superconducting gap. In this case, there are no available quasiparticle states and a Cooper pair is formed. For reasons of momentum conservation, the original incoming electron is reflected as a hole, as visualized in figure 2.8 [185]. The application of a strong negative gate voltage increases

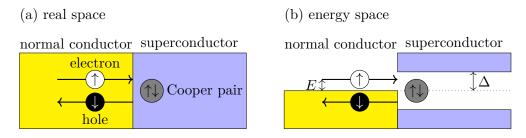


Figure 2.8.: Schematic sketch visualizing Andreev reflection in (a) real and (b) energy space. An electron with an energy $E < \Delta$ smaller than the superconducting gap Δ from a normal conductor enters the superconductor while forming a Cooper pair and is reflected as a hole. Drawn according to [185].

the contact transparency between Nb and CNT, which significantly decreases the sample resistance and the shape of the differential resistance. If no gate voltage is applied, only tunnel conduction is observed. With an increase in temperature, the Andreev dip also disappears [51]. In 2010 individually resolved Andreev bound states (ABSs) in a CNT via transport spectroscopy were reported for the first time. ABSs can be thought of as the electronic analog of resonant states within a Fabry-Perot resonator. A change in the superconducting phase ϕ changes the energy $E_n(\phi)$ of the ABS and results in a supercurrent of $(2e/\hbar)(\partial E_n(\phi)/\partial \phi)$ [126].

In the same year, Kasumov et al. [49, 70] reported induced superconductivity in strained SWCNTs as well as in a bundle of several 100 CNTs. Superconductivity can be induced if the junction resistance is sufficiently small. Temperature and magnetic field dependence of the critical current are described as unusual and attributed to the 1D conductor. The maximum current through a noble metal wire contacted with two superconductors (SNS junction) is

$$I_{\rm max}^{\rm short} = \frac{\pi\Delta}{eR_{\rm N}},\tag{2.14}$$

in the limit of short junction. Here $R_{\rm N}$ denotes the normal resistance of the junction.

On the contrary,

$$I_{\rm max}^{\rm long} = \frac{\alpha E_{\rm c}}{e R_{\rm N}} \tag{2.15}$$

is the limit for long junctions. Therein, $\alpha \approx 10$ is a numerical factor and $E_c = \hbar D/L^2$ expresses the Thouless energy. The authors showed that the maximum current through a CNT can be much higher. Re/Au or Ta/Au contacts were used in these samples. The *IV* characteristics showed levels similar to those of phase slip centers (PSCs), which will be discussed in section 2.5.1. The critical current through a SWCNT falls linearly/concavely with increasing magnetic field/temperature [49, 61].

Similar results were reported by the same group four years later. They reported intrinsic superconductivity in ropes of 40 to 100 SWCNTs (attractive pairing, not repulsive interaction) with *normal* contacts and high temperature resistances ranging from 100 to $1 \times 10^5 \Omega$. Large supercurrents, indicating coherent transport in µm scales were observed. Also proximity effect in individual tubes contacted with superconducting Ta was detected. They also found hysteretic steps in the IV characteristics for $I > I_c$ which was also visible in the differential resistance. The critical current I_c depends linearly on magnetic field. Non-conventional proximity effect and signatures of 1D PSCs are blamed for intrinsic superconductivity [70].

A few years later, induced superconductivity was reported in MWCNTs contacted with Ti/Al/Ti also in QD configuration. The applied gate voltage acting on the diffusion constant increases the critical current by an order of magnitude [102].

Other findings related to superconductivity in CNTs were, among others, reported in references [65, 94, 147].

2.3. Transport regimes

In this section, we discuss some transport regimes, mostly specific to CNTs. A CNT can be seen as a genuinely 1D conductor [37]. Let L denote the typical size of the considered conductor. We have to distinguish three length scales. The Fermi wavelength

$$\lambda_{\rm F} = \frac{2\pi}{k_{\rm F}} = \lambda_{\rm dB} = \frac{h}{mv_{\rm F}} \tag{2.16}$$

corresponds to the de Broglie wavelength $\lambda_{\rm dB}$ of the electrons at the Fermi level. The mean free path $L_{\rm m}$, also called the momentum relaxation length, is the mean path length until an electron is scattered. Third, the phase relaxation length L_{φ} is the distance after which a particle loses its coherence as a wave. During transport only the electrons at the Fermi level contribute [143].

2.3.1. Ballistic transport in carbon nanotubes

Ballistic transport $(L_{\rm m} > L_{\varphi} > L)$ occurs when a defect-free CNT has ideal, highly transparent contacts. Single electron conduction without momentum or phase relaxation takes place and the electron's wavefunction is a solution of the Schrödinger equation.

The transport occurs in the 1D conduction channels of the 1D subbands, which can be described in the Landauer-Büttiker formalism. Scattering occurs only at the edges of the sample. The Drude model cannot be applied. Landauer described ballistic conduction with transmission probabilities and Büttiker used this approach to describe transport in mesoscopic multiterminal devices. The conductance is not infinite even in absence of scattering inside the conductor since there are infinite channels in the reservoirs but only a limited number of conduction channels inside the conductor [34, 39, 138, 218]. Because of the degeneration of spin and valley, a SWCNT ideally contributes $G_0 = 4 \cdot e^2/h = (6.4 \text{ k}\Omega)^{-1}$ to the electrical conduction [95, 96]. In reality, this value can sometimes be significantly reduced by defects within the CNT or non-ideal contacts [71, 143].

2.3.2. Fabry Perot interference in carbon nanotubes

Fabry Perot can appear for extremely transparent contacts in the hole regime where charging effects are suppressed. Here the CNT corresponds to a 1D waveguide. The electronic wavefunction scatters only weakly at the contact. One has to deal with ballistic transport were one has no interaction, charge quantization or Coulomb blockade. In transport, an oscillatory dependence of $dI/dV(V_{SD}, V_G)$ is observed, where the frequency is proportional to the CNT length. In few cases, also a slower modulation on top is detected. From the latter the chiral angle can be extracted [63, 199].

2.3.3. Classical transport

In the regime of classical transport $(L_{\varphi} < L_{\rm m} \ll L)$, an electron can be regarded as a particle because of the frequent occurrence of momentum and phase relaxation. Since the phase should be well defined over a length L, the Schrödinger equation cannot be solved for the whole sample. The total, ohmic resistance is the sum of all microscopic resistance contributions of the pulse relaxations [143].

2.3.4. Diffusive transport and localization in carbon nanotubes

Diffusive transport $(L_{\rm m} \ll L_{\varphi} < L)$ occurs when the distance between the contacts is much larger than the distance scattering events. It is dominated by elastic scattering events which affect $L_{\rm m}$. The wavefunction is localized. The Einstein relation

$$\sigma = e^2 N(E_{\rm F}, B) D(T, B) \tag{2.17}$$

then describes the transport. e represents the elementary charge, N is the density of states and D the diffusion constant. The latter is classically given by

$$D_{\rm class} = \frac{1}{2} v_{\rm F} L_{\rm m}, \qquad (2.18)$$

to which quantum corrections can be added [95]. There are two localization regimes, where $L_{\phi} > L_{\rm m}$ always applies to both. They differ in the localization length $L_{\rm c} = ML_{\rm m}$,

where M stands for the number of line channels. L_c can be understood as the mean spatial extent of quantum mechanical states. In the case of a perfectly periodic lattice, the Bloch states are infinitely extended and $L_c \to \infty$ is valid whereas disorder results in a finite L_c . In the case $L_{\phi} < L_c$, one speaks of the so-called *weak localization*. Known phenomena are the universal conductance fluctuations, the electron-electron interaction (Coulomb screening in lower dimension less effective) and the negative magnetoresistance. In the case $L_{\phi} > L_c$, one speaks of the *strong localization*. This is the effect of a random potential generated by defects. The corresponding wave function is called Anderson localization [143].

2.3.5. Quantum dots and Coulomb blockade in carbon nanotubes

A QD is an approximately 100 nm large conducting island located in a non-conducting environment. A QD can form in a self-assembled metal cluster [103] or in electrically contacted nanowires [76], or be electrostatically formed in a two-dimensional electron gas (2DEG) [128]. A typical sample geometry is shown schematically in figure 2.9. Let

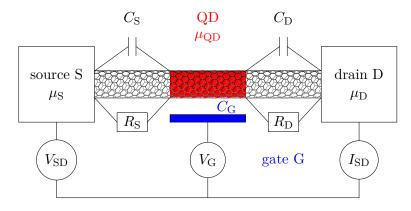


Figure 2.9.: Schematic sketch of a QD electrically coupled to a source (S) and a drain (D) electrode via tunnel junctions. The corresponding tunneling resistances are marked with $R_{\rm S}$ and $R_{\rm D}$, the corresponding capacitances with $C_{\rm S}$ and $C_{\rm D}$. The potential of the QD can be adjusted by a capacitively coupled gate $V_{\rm G}$. For an applied bias voltage between source and drain $V_{\rm SD}$, measure the current $I_{\rm SD}$ through the sample as a function of $V_{\rm G}$. Drawn according to [36, 87].

us assume a metallic capacitor. Only if the charging energy of

$$E_{\rm c} = \frac{e^2}{C_{\Sigma}} \tag{2.19}$$

with $C_{\Sigma} = C_{\rm S} + C_{\rm D} + C_{\rm G}$ (and eventually some additional capacitance $C_{\rm add}$) is paid, the number of electrons inside the QD can be increased by one, against the repulsion of the electrons already inside the QD. Two conditions must be fulfilled for a fixed number of electrons in the QD and thus for Coulomb blockade. First, the thermal energy must be

2.3. Transport regimes

smaller than the charge energy

$$k_{\rm B}T \ll \frac{e^2}{C_{\Sigma}},\tag{2.20}$$

so that the number of electrons cannot vary due to thermal fluctuations. Small structures and mK temperatures make this possible in practice [186]. Second, the tunnel resistances $R_{\rm S}$ and $R_{\rm D}$ must be sufficiently high and couple only weakly to the environment so that the number of electrons for the time scale $\Delta t = R_{\rm S/D}C_{\rm S/D}$ of a representative measurement is well defined. By using the Heisenberg uncertainty relation $\Delta E \Delta t \approx h \stackrel{!}{=} U \Delta t$ one can use equation 2.21

$$R_{\rm S/D} \gg \frac{h}{e^2} = 25.8 \,\mathrm{k\Omega}$$
 (2.21)

as second criterion. Single electron tunneling occurs for $\mu_{\rm QD} = \mu_{\rm S/D}$, see figures 2.10(b,c) [87]. Figure 2.10(a) shows that for a small $V_{\rm SD}$ the QD is in blockade unless $V_{\rm G}$ changes the occupation number from $N \leftrightarrow N + 1$. As a result the conduction $G(V_{\rm SD}, V_{\rm G})$ shows diamond shaped areas with a fourfold periodicity as depicted in figure 2.10(b). It is possible to observe discrete excited state spectrum (red lines) for larger $V_{\rm SD}$ [95]. Here the density of states is no longer constant and the Fermi wavelength $\lambda_{\rm F} \approx 100 \,\mathrm{nm}$ is of the order of the device. The energetic distance $\Delta \varepsilon \gg E_{\rm therm} k_{\rm B} T$ between two discrete states must be greater than the thermal energy. The value of $\Delta \varepsilon$ depends on the dimensionality of the system. Considering the spin degeneration,

$$\Delta \varepsilon_{1\mathrm{D}} = \frac{N}{4} \frac{\hbar^2 \pi^2}{mL^2} \tag{2.22}$$

holds for the 1D case. In the white areas of Coulomb diamonds, no current flow is possible for the respective values of $V_{\rm SD}$ and $V_{\rm G}$ due to Coulomb blockage. Touching the conductive areas at $V_{\rm SD} = 0$ V corresponds to the charge state of the QD where $\mu_{\rm QD}$ is aligned with $\mu_{\rm S}$ and $\mu_{\rm D}$ as visualized in figure 2.10(c). Figure 2.10(a) shows a gate voltage trace at $V_{\rm SD} = 0$ V with Coulomb oscillations. If $V_{\rm G}$ is constant, $V_{\rm SD}$ is increased at a point, an electron is lifted into the conductive region and single electron tunneling (SET) can occur. The bias voltage $V_{\rm SD}$ changes the chemical potentials $\mu_{\rm S}$, $\mu_{\rm D}$ of source and drain contact whereas the gate voltage $V_{\rm G}$ changes the chemical potential of the QD. Extract the slope from the single electron tunneling lines and calculate the gate conversion factor $\bar{\alpha}$. Several single tubes or bundles lead to overlapping coulomb diamonds. Multiplying the width of a Coulomb diamond with $\bar{\alpha}$ gives the addition energy [260]. QDs do not always show a clear four-fold symmetry. K/K' can be mixed at the contact interface or by defects resulting in a lift of degeneracy [66]. Failure of Coulomb diamonds to close completely may result from the nanomechanics of the strained CNT. When a CNT vibrates, the distance between QD and gate changes. Consequently, the gate capacitance changes and so does the current flow through the QD [260].

Regular Coulomb diamonds as well as excited states in a multi walled MoS_2 nanotube at 300 mK and charging energies in the range of 1 meV were observed in 2019 for the first time. Quantum state transitions with a g-factor ≈ 2 predicted from theory are measured

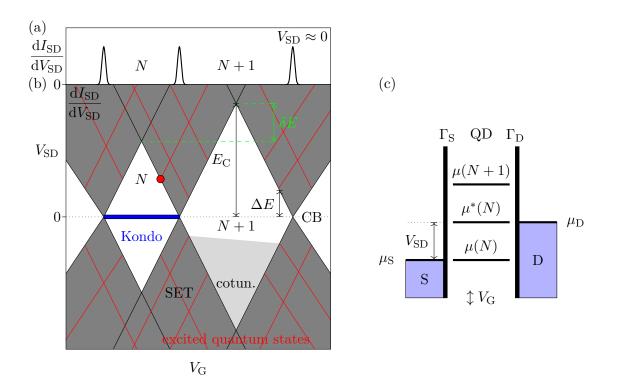


Figure 2.10.: Quantum transport in a QD at finite bias. (a) Coulomb resonances between blocked regions as a function of $V_{\rm G}$ at $V_{\rm SD} \approx 0$. (b) White diamond-shaped regions correspond to Coulomb blockade (CB) inside the QD, the dark gray areas to single electron transistor (SET) where current flow takes place. The red lines visualize the excited quantum states. The light gray area indicates cotunneling. The blue bar indicates a Kondo resonance. ΔE represents the excitation energy. (c) Energy diagram for the red-marked point in subfigure (b). The vertical black lines represent the tunnel barriers of the QD. $\Gamma_{\rm S}$ and $\Gamma_{\rm D}$ denote the tunnel probabilities of source and drain contact. Drawn according to [87, 186].

in the magnetic field perpendicular to the nanotube axis [256].

2.3.6. Kondo effect in carbon nanotubes

The Kondo effect in a QD is a many-body effect and a non-perturbative process. Spin flipping is enhanced at the Kondo temperature $T = T_{\rm K}$ resulting in an increase of the conduction at low temperatures [95]. A local quantum degree of freedom couples to a Fermi sea of delocalized electrons. A CNT QD transforms into a Kondo impurity when weakly coupled to source and drain electrode. In equilibrium, the Kondo effect leads to a resonance peak in the DOS of the QD due to the appearance of a singlet state. The Kondo effect is especially expected for an odd number of electrons in the QD. For an even number of electrons the total spin is zero and hence no Kondo effect should be observed [186, 230]. In contrast, in the general Kondo effect, the resistance of the system increases if the temperature falls below the Kondo temperature $T_{\rm K}$. The initial condition is a spin-degenerate impurity (which replaces the QD), which is occupied by only one electron. This unpaired spin is screened by the mobile electrons of the metal. A virtual transition of an electron from the conduction band into the impurity occurs. This results in an effective antiferromagnetic exchange interaction between surrounding conduction electrons and the impurity [87]. The consequence of a coherent sum of many such transitions is a new state at $E_{\rm F}$ of the metal (Kondo resonance). The bulk offers a large DOS into which electrons can be scattered. Consequently, the scattering cross section increases and thus the resistance rises.

In reference [231], the transverse vibration mode of a suspended CNT is used as a charge detector. The Kondo effect between the QD and its leads was observed. The Kondo effect represents a manifestation of electronic correlations. It is observed in semiconducting CNT QDs as a zero-bias maximum in the differential conductance at even/odd electronic occupation number, resulting from a nearly fourfold spin/valley degeneracy of the single particle energy levels – the so-called SU(4) Kondo. Although the spin is decisive for its formation, it acts on the electronic states. Here the asymmetry concerning the even/odd occupation number is canceled due to the charge confined by a gate. The appearance in the stability diagram is illustrated in figure 2.10(b).

2.3.7. Electric contacts and Schottky Barrier

A Schottky barrier (SB) is formed at the interface between a semiconducting CNT and a metal contact. The work functions of CNT and contact material determine the contact transparency and thus the transport regimes. The transparency can depend on the gate and can be different for electrons and holes in semiconducting CNTs [186].

For the following discussion the Fermi level of a n-type semiconductor should be above that of the metal, as illustrated in figure 2.11(a). If both materials are brought into contact, charge carriers flow from the semiconductor to the boundary layer until both Fermi levels have equalized [122]. In the vicinity of the interface, semiconductor atoms will be ionized. This area exhibits positively charged atoms (depletion zone). Hence,

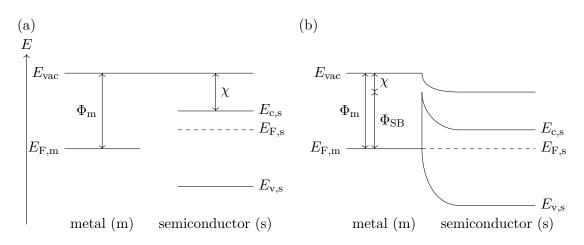


Figure 2.11.: (a) Energy diagram of a metal (left) and a n-type semiconductor (right) when they are not in contact with each other. (b) The two Fermi levels $E_{\rm F,m}$ and $E_{\rm F,s}$ assimilate when both materials are brought into contact and a SB $\Phi_{\rm SB}$ emerges. The subscripts *c* and *v* stand for *conduction* and *valence band*, respectively. Drawn according to [84].

valence and conduction band bend downwards and the SB

$$\Phi_{\rm SB} = \Phi_{\rm m} - \chi \tag{2.23}$$

is formed, as illustrated in figure 2.11(b). Here $\Phi_{\rm m}$ denotes the metal's work function and χ the electron affinity of the semiconductor. Under certain conditions the charge carriers can overcome the SB [53].

For the situation of 1D, CNTs Fermi level pinning only creates a weak tunnel barrier in series with the junction with a spatial extension of ~ 2 nm. Hence, the height of the SB is not affected. Instead, it is mainly dictated by $\Phi_{\rm m}$ [53]. The mircostructure of the contact metal may play a crucial role. It was reported that the Schottky barrier to CNTs can be eliminated when using Pd contacts [69, 108].

2.4. Majorana fermions in carbon nanotubes

A combination of atomic wave functions in many-body physics can be considered as trivial (atomic limit). But if a wave function in a condensed matter system is adiabatically distinct from the atomic limit, it can be considered topologically [217]. In recent years, superconductors have therefore become the focus of interest, as this topological classification is generally applied to numerous quantum many-body states that protect states separated by a gap in their energy bands. In general, the superconducting state of Cooper pairs can be considered trivial. It becomes topological when a certain symmetry is broken. Kitaev was the first to describe topologically non-trivial superconductivity in 1D systems in 2001 [60]. The detection of Majorana zero modes at the edges of the 1D

system indicate the topological phase. The Majorana modes result from a time-reversal symmetry breaking p-wave pairing [127]. MFs are interesting because they are their own anti-particle and they are auspicious candidates for fault-tolerant quantum computing because they obey a non Abelian exchange statistic [217].

In recent years, several material systems based on s-wave superconductors have been proposed that can accommodate MFs [104, 127, 131, 145, 198]. To observe Majorana zero modes, 1D nanowire with large SOC (e.g. InSb, InAs), a s-wave superconductor (e.g. TiNbN, AI) and a magnetic field must fulfill the topological phase condition of Kitaev's 1D spinless p-wave superconductor [124, 125], as illustrated in figure 2.12. Without

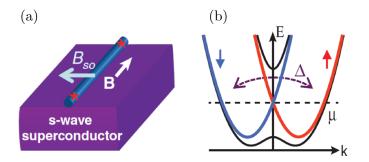


Figure 2.12.: (a) Device for MF detection according to reference [145]. A semiconducting nanowire is placed on top of a s-wave superconductor. A magnetic field \vec{B} is applied parallel to both the wire axis and the superconductor. The SO field \vec{B}_{SO} is oriented perpendicular to the wire axis and parallel to the substrate. The stars indicate the emerging MFs at the wire ends. (b) The two-fold degeneracy at k = 0 is lifted due to the magnetic field \vec{B} . Images taken from [145].

a magnetic field, the band structure is doubly spin degenerated. The different spin bands are marked in red and blue. For no position of the chemical potential μ , the system can be transformed into a spinless state, which is supported by the spectrum only by an even number of paired Fermi points. This is fixed by an external magnetic field applied parallel to the wire axis to create a gap at the intersection of the two spin-orbit bands, allowing the formation of only one such state. Hence, the degeneracy at $\vec{k} = 0$ is canceled. The resulting band structure is indicated by the black lines. The nanowire now becomes spinless if the chemical potential is within the gap. Inside the gap the degeneracy is two-fold (topological superconductor), outside it is fourfold. Cooper pairs can be efficiently introduced into the lower band by proximity effect in the wire between electronic states of different spin and momentum, resulting in the gap Δ . If the topological criterion

$$E_{\rm Z} = g\mu_{\rm B} |B_{\rm Z}| / 2 > \sqrt{\Delta^2 + \mu^2}$$
(2.24)

for the Zeeman splitting E_Z applies, Majorana modes will be created at the ends of the nanowire [131, 140, 145]. Experimentally, Majorana states should show up as zero-bias conduction peaks in transport tunneling experiments. Such zero-bias conduction peaks can also result from Kondo correlations, reflectionless tunneling, weak antilocalization

and Andreev bound states. In the Kondo effect as well as in Andreev bound states, zero bias peaks occur at finite magnetic field, which, however, split with increasing field. The zero peak in weak antilocalization or reflectionless tunnels becomes smaller with increasing magnetic field. MFs can occur naturally as elementary particles or charge-neutral zero-energy quasiparticles in superconductors [145, 152].

We, on the other hand, use a different, theoretical in-house proposal for a sample geometry for the detection of MFs. The sample layout of Marganska et al. [238] is depicted in figure 2.13(a). The scheme is based on the proximation of an ultra-clean

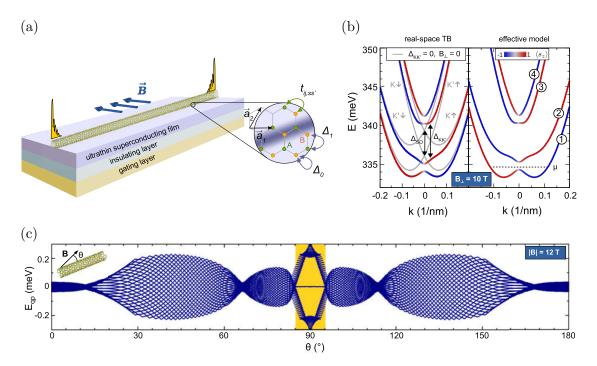


Figure 2.13.: (a) Schematic sample geometry from reference [238]: A CNT lies on a thin superconducting film. The chemical potential of the hybrid system can be controlled by a gate. A magnetic field is applied perpendicular to the CNT and parallel to the substrate. Majorana quasiparticles are observed at the ends of the CNT. (b) Energy bands of a (12,4) CNT near the Γ point in the conduction band. Red/blue mark the spin up/down bands. These diagrams were obtained from real-space tight binding (TB) calculations and an analytical effective model. One observes a gap at k = 0. (c) For $|\vec{B}| = 12$ T the angular range ($\pm 5^{\circ}$) is marked in yellow, for which its deviation still a zero-energy mode is detected. Images modified adopted from [238].

semiconducting CNT by a thin s-wave superconductor. CNTs intrinsically show a large curvature-induced SOC. Due to the SOC, the spin in the CNT is parallel to the CNT axis. This splits the bands by Δ_{SO} , which can exceed 3 meV. Because of the interaction of the CNT with the substrate and the applied magnetic field (perpendicular to the CNT axis and parallel to the superconductor), the subband degeneracies are broken at

2.4. Majorana fermions in carbon nanotubes

k=0 due to valley mixing. The chemical potential μ can be modulated by means of a gate layer. Unlike in reference [157], semiconducting CNTs are treated here because in them the Fermi velocity $v_{\rm F}$ is at least three orders of magnitude smaller than in metallic ones. In semiconducting CNTs, MF can arise at the ends if the CNT is only a few µm long and thus experimentally feasible, whereas a metallic CNT would have to be mm long as in [157]. TB calculations and an effective analytical model revealed that above a critical magnetic field, localized zero-energy states at the ends of the CNT can appear as MFs (see figure 2.13(b)). The detailed calculations start from a microscopic tight binding model of the CNT lattice and then consider the interaction with the substrate. superconducting pairings, external magnetic field and the influence of disorder. Localized Majorana zero-energy states occur above a certain critical magnetic field in real space at the ends of the CNT. Figure 2.13(c) shows the maximum allowed angular deviation $\pm 5^{\circ}$ of the magnetic field from the perpendicular orientation to the CNT axis, below which MFs can still be detected. A magnetic field component parallel to the CNT axis conditions an Aharanov Bohm effect. The different valleys are no longer degenerate and the chiral symmetry is broken. Above a certain angle, no more energy gap is observed.

In contrast to the semiconducting nanowires, CNTs are atomically well-defined and uniform and they represent an almost perfect model of a 1D conductor [58]. Hence, one has a much better control over microscopic properties. CNTs have a typical diameter of $\sim 1 \text{ nm}$. In contrast, a nanowire diameter is in the order of $\sim 10 \text{ nm}$. However, it remains questionable whether it is possible to gate a CNT only a few nm thick into the topological phase [238].

For the experimental realization, single CNTs with a length of 3 to 10 µm are required. One needs to induce superconducting correlations in high magnetic field. Furthermore, the chemical potential μ must be able to be changed so that the topological phase can be reached. Last but not least, it must be possible to orient the magnetic field perpendicular to the CNT axis and parallel to the superconductor [238].

Our solutions for this are as follows. Isolated, sufficiently long and mostly straight CNTs are grown from nominally 1 nm thick Co films. As a thin superconductor, few-layer NbSe₂ is used. This material remains superconducting in-plane magnetic fields up to over 30 T and its chemical potential μ can be changed with a gate [205]. Thin-layer hBN is used as a protective layer and as a dielectric. The chemical potential can be modulated by means of a top gate. The correct orientation of the magnetic field relative to the sample can be ensured by means of an in-situ rotator.

Milz et al. calculated the 3D profile of Majorana bound states in semiconducting CNTs using the atomic tight-binding method [254]. The usage of CNTs for MFs detection were not only proposed in Regensburg but very recently also in reference [269]. Magnetic fields in CNTs usually have to be high due to their low g-factor. Here no Zeeman splitting is needed. They make use of an orbital effect caused by magnetic flux threaded through the CNTs. Curvature-induced SOC of CNTs and a gate breaks the rotational symmetry. Hence, the system goes into a half-metallic state using relatively low fields. They use a non-trivial pairing in NbSe₂ for the topological phase. The other experimental requirements are instead basically the same. A few years back, another mechanism was

proposed by Egger et al. [142]. They calculated the low energy bandstructure of armchair and small bandgap semiconducting CNTs with proximity induced superconducting pairing when a spiral magnetic field creates strong effective SOI from the Zeeman term. This field is much stronger than the curvature induced one and produces a periodic potential along the CNT which breaks automatically the valley degeneracy. Hence, in this proposal the valley mixing parameter $\Delta_{KK'}$ is not essential for forming the Majorana bound states.

2.5. Resistive states in superconductors

In this section 2.5, we will discuss some issues related to superconductivity. In particular, we highlight the topic of phase slip (PS) events in general and their appearance in $NbSe_2$ in particular. Until today, it is not fully understood how resistive zones occur in superconductors and how the dimensionality of the superconductor influences this. $NbSe_2$ is a perfect playground for this [244].

2.5.1. Phase slip centers

The Ginzburg and Landau (GL) theory of superconductivity [5] describes the pairbreaking current as the critical current value at which superconductivity collapses. Below this value, dissipation occurs in superconductors if the current bias is high enough. This can be caused by the movement of Abrikosov vortices by an external magnetic field or by the current through the sample itself. If no vortices are present, dissipation may be due to the occurrence of PSCs as observed in 1D Sn whiskers with diameters of $\sim 1 \,\mu\text{m}$ or microbridges 50 years ago [9, 15]. Current induced phase transition from super to normal conduction due to a finite order parameter were studied. For large currents, voltage steps increasing linearly with current were observed as visualized in figure 2.14 [13, 14]. The

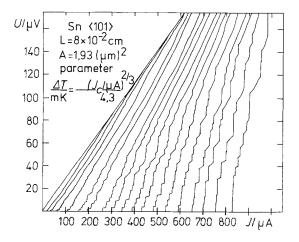


Figure 2.14.: V(I) characteristics of a Sn whisker for fixed temperatures show a staircaselike behavior. These features are related to PSCs. Image taken from [14].

2.5. Resistive states in superconductors

voltage drop along a filament of length L with n equally spaced PSCs is given by

$$V_n = \rho L (J - \bar{J}_{\rm S}) \left[\frac{2n\Lambda}{L} \tanh \frac{L}{2n\Lambda} \right], \qquad (2.25)$$

where $\bar{J}_{\rm S}$ is the time-average supercurrent in the center of the PSC and J is the current density. For Λ see equation (2.40). Equation (2.25) returns a set of straight lines which go through the point $(J = \bar{J}_{\rm S}, V = 0)$. The criterion for nucleating the (n + 1)th PSC is given by

$$J - \frac{J - J_{\rm S}}{\cosh(L/2n\Lambda)} \le J_{\rm c},\tag{2.26}$$

i.e., that the time-averaged supercurrent $J - \bar{J}_n$ shall never exceed the critical current J_c . In equation (2.26), the exponential decay of the normal current on the two sides of the PSC is described with the factor $\cosh(L/2n\Lambda)$. From equation (2.26) one finally receives

$$\frac{J_{\max,n}}{J_{\rm c}} \simeq 1 + 2(1-\beta) \exp\left(-\frac{L}{2n\Lambda}\right),\tag{2.27}$$

where $2(1-\beta) \approx 1$ holds. Hence, PSCs are nucleated in the closest current spacing when $L/2n\Lambda \gg 1$ applies [18].

The resistive state is not present in the classical GL theory and means a coexistence of superconductivity and direct current (DC) electric field. The step shape is less pronounced for longer and dirtier samples. Experiments were typically performed close to T_c because here the relevant currents are low and consequently Joule heating can be reduced. But how can superconductivity coexist with a DC electric field? Since Cooper pairs are charged, they should be accelerated by the electric field and continue to be accelerated until they reach the critical velocity, causing the superconductivity to break down. But this is not the case in the resistive state, because the vector potential \vec{A} and the scalar potential ϕ of the electric field are not sufficient to describe the motion of Cooper pairs in a superconductor. Rather, the gauge invariant potentials

$$\vec{Q} = \vec{A} - \frac{c}{2e} \nabla \chi \tag{2.28}$$

and

$$\Phi = \phi + \frac{1}{2e} \frac{\partial \chi}{\partial t} \tag{2.29}$$

must be used. Note that χ denotes the phase of the order parameter. Via the following

$$\vec{v}_{\rm s} = -\frac{e}{mc}\vec{Q},\tag{2.30}$$

 \vec{Q} is related to the Cooper pair velocity $\vec{v}_{\rm s}$. Finally, by transforming the expression for

the electric field

$$\vec{E} = -\frac{1}{c}\frac{\partial \vec{Q}}{\partial t} - \nabla\Phi, \qquad (2.31)$$

we obtain the following formula for the acceleration of Cooper pairs

$$\frac{\partial \vec{v}_{\rm s}}{\partial t} = \frac{e}{m} \left(\vec{E} + \nabla \Phi \right). \tag{2.32}$$

So that this acceleration does not become infinitely large, \vec{E} must be compensated by $\nabla \Phi$.

Another possibility is not global but only local destruction of superconductivity. In these points, the coherence of the phase is broken and the phase difference changes in such a way that the increase of the electric field is compensated. Such points are called hot spot (HS) and have a slightly higher temperature. They are based on Joule heating and depend on the thermal contact between the sample and the environment [21].

Now, if Joule heating is sufficiently small, then the resistive state is degenerated into distinct points, the so-called PSCs. As explained above, the electric field \vec{E} conditions an acceleration of Cooper pairs. Since Φ is non-decreasing along the channel, this acceleration is associated with the growth of the phase difference between two different points in the superconducting channel according to equation (2.33)

$$\delta\phi + \frac{1}{2e}\frac{\partial}{\partial t}\delta\chi \simeq 0, \qquad (2.33)$$

where $\delta \chi$ is the order parameter's phase difference between two distinct points. Figure 2.15 shows the real and imaginary parts of the complex-valued order parameter $\psi = \psi_1 + i\psi_2$ along the *x*-axis (sample axis). Since in the uniform state, the amount $\Delta = \sqrt{\psi_1^2 + \psi_2^2} =$

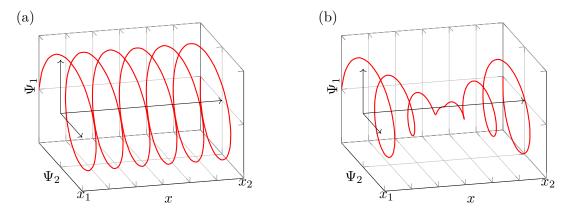


Figure 2.15.: (a) Helix of the complex order parameter Ψ as a function of Ψ_1 , Ψ_2 and x. (b) During a PS event the helix can loose one of its loops when its radius takes the value zero at a certain point. Drawn according to [21].

const. holds, all turns of the helix have the same radius. As time passes, the phase difference $\delta \chi$ increases and the windings of the helix become denser. A regressum ad

infinitum is not possible, as described above, because $\delta \chi$ determines the Cooper pair velocity

$$v_{\rm s} \propto \frac{\delta \chi}{m(x_2 - x_1)}.$$
 (2.34)

However, this cannot become arbitrarily large, since otherwise the superconductivity would collapse again. For this not to happen, the helix must loose at least one of its windings, which is achieved by making the radius of the helix zero at a point between x_1 and x_2 . Exactly such points, where the order parameter vanishes and the phase jumps by multiples of 2π , are called PSCs. To maintain superconductivity within the channel, the PS process must repeat periodically in time. The relationship between the mean time t_0 between two such events and the associated mean voltage V between points x_1 and x_2 is given by equation (2.34). After time averaging, after discarding one winding, which corresponds to a phase slip of 2π , one obtains the usual Josephson relation

$$2eV = \frac{2\pi}{t_0}.$$
 (2.35)

Two mechanisms for the formation of a PSC are possible. One can be the formation of thermodynamic fluctuations in the system, which is proportional to $\propto \exp(-\delta \mathcal{F}/T)$. $\delta \mathcal{F}$ denotes the free energy barrier between two uniform states before and after the phase slip. This process is more likely close to T_c [8]. At temperatures lower than the critical one, the process must be imagined differently. The formation of PSCs is most likely to occur at the weak points of the superconducting channel, such as structural defects, because there the order parameter is suppressed by external reasons. On the other hand, if the sample is homogeneous and sufficiently long, PSCs should emerge periodically in time and space. A visualization is given in figure 2.16. We consider the space-time $\{x; ct\}$.

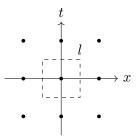


Figure 2.16.: Space-time $\{x; ct\}$. PSCs are indicated with filled black circles. At these points, the phase of the order parameter jumps by 2π when a closed line is traversed. The dashed line *l* encloses the unit cell of the PSC structure in space-time $\{x; ct\}$. Drawn according to [21].

black filled circles regularly spaced in time and space represent PSCs. In these points, the magnitude of the order parameter $\Delta = 0$ is zero. The process sketched in figure 2.15 is equivalent to when the phase of the order parameter changes by a multiple of 2π as one walks around a PSC in figure 2.16 along a closed line *l*. Consequently, PSCs can be

2. Theoretical background

seen as vortex-like topological singularities in space-time $\{x; ct\}$.

For this, a quantization rule for the electric field in space-time $\{x; ct\}$, analogous to the magnetic flux quantization in normal space, can be derived. One receives a generalized Josephson relation

$$\int_{S_0} E \mathrm{d}s = \phi_0 n. \tag{2.36}$$

The experimentally accessible time-averaged electric field is then

$$\langle E \rangle = \frac{\phi_0 n}{c t_0 L},\tag{2.37}$$

where $\phi_0 = \pi c/l$ and $n \in \mathbb{Z}$. t_0 and L denote the time and space period of the PSC structure and S_0 is its unit cell area [21]. According to the model developed by Skocpol, Beasly and Tinkham (SBT), the superconducting order parameter oscillates between its maximum value and zero inside a PSC and a finite voltage and thus dissipation occurs [21]. I_c can in some point be lower in a disordered, non-homogeneous film. In such places, PSCs will be generated preferentially. The emerging electric field accelerates the supercurrent above the critical velocity $v_{\rm c}$. The order parameter collapses and all current flows as normal current. Superconductivity reappears as soon as the velocity is below $v_{\rm c}$ and the cycle will start again. The phase difference slips by 2π each time Δ goes to zero in the middle of a PSC. A PSC has a spatial extension of $\sim 2\xi$ since this quantity governs the spatial variation of Δ . This is visualized in figure 2.17(a). There, quasi-particles, which correspond to the normal current, are periodically formed. They diffuse outwards up to the quasi-particle relaxation length Λ with an exponential decrease. The supercurrent time-averaged over the Josephson cycle has some non-zero DC value $\bar{I}_{\rm s} \approx I_{\rm c}/2$ as illustrated in figure 2.17(b). The rest of the current $(I - \bar{I}_{\rm s})$ must be carried as normal current [81].

The total voltage across a single PSC is given by

$$V = \frac{2\Lambda\rho}{A} \left(I - \frac{I_{\rm c}}{2} \right), \tag{2.38}$$

where ρ is the normal state resistivity and A is the cross-sectional area. Since this is essentially the same as the weak links described in Josephson junctions (JJs), it can be assigned a phase oscillation frequency $\nu = 2eV/\hbar$ [81].

There can be one or more such PSC breakdown zones. They are referred to as currentinduced PSCs and must be distinguished from thermally activated PS events. If the current is significantly higher than I_c , then the PSC becomes a normal conducting HS due to Joule heating. Its corresponding nucleation current shall be denoted with I_h . For a long time, it had been assumed that PSCs can only be observed close to the transition temperature. This has now been experimentally disproved [107, 112, 166]. The IV-characteristic shows a jump at I_c , which is followed by a rising ramp as

$$V(I) = R_{\rm u}(I - I_{\rm S}),$$
 (2.39)

2.5. Resistive states in superconductors

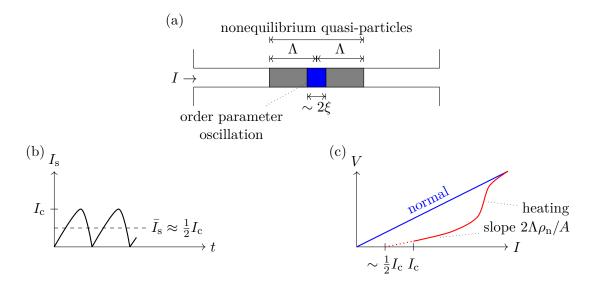


Figure 2.17.: (a) Schematic sketch of a PSC in a 1D superconductor. The order parameter oscillates in a region of extension ~ 2ξ . The relaxation of non-equilibrium quasi-particles takes place over the range of Λ . (b) Oscillations of the supercurrent in the core. The mean value is ~ $I_c/2$. (c) Schematic *IV* characteristic of a strip hosting one PSC. Drawn according to [81].

where $R_{\rm u}$ denotes the differential resistance, which results from the generation of quasiparticles at every gap closing and the diffusion to the two ends of the PSC zone with a spacial extension of ξ (coherence length) over a distinctive length of

$$\Lambda = \sqrt{\frac{v_{\rm F} l_{\rm e} \tau_{\rm R}}{3}},\tag{2.40}$$

which is typically in the µm-range. In equation (2.40), $v_{\rm F}$ denotes the Fermi velocity, $l_{\rm e}$ the electronic mean free path and $\tau_{\rm R}$ the transverse relaxation time. Both, $R_{\rm u}$ and $I_{\rm S}$, can be considered independent of the current I [15]. A characteristic of current-induced PSCs is that they have a finite nucleation time in the range of ns and they are time independent of their voltage, whereas the flow of vortices, for example, starts instantaneously. HS instead grow linearly with voltage when driven with a constant current [107]. It was assumed that the transverse dimensions of a sample for observing PSCs should be smaller than the London penetration depth λ and the coherence length ξ [107]. Nevertheless, PSCs have also been observed in 1D systems that do not meet this criterion [107, 112, 166].

A little later, PSCs were also detected in their analog form of PSLs within 2D systems [31]. PSLs show IV characteristics that are very similar to those of PSCs. However, the respective physical mechanism behind them is different. PSLs could only be observed in high quality thin films with special care for roughness of the edges and close to T_c [74,

2. Theoretical background

107, 255]. The oscillation of the order parameter does not have to be uniform but there may be propagating waves that carry the singularities of the order parameter across the sample, also called kinematic vortices. It is also possible that two singularities propagate in opposite directions (kinematic vortex-antivortex pair) [111]. To make the observation of PSLs possible, the formation of Abrikosov vortices must be prohibited by suitable energy barriers at the edges. Furthermore, Joule heat must be efficiently dissipated so that the IV characteristic is not smeared. The presence of PSLs instead of Abrikosov vortices in thin films can be seen in the transport properties in the vertical magnetic field. Numerical simulations based on the time-dependent GL equations [110] have shown, the experiment observes a rapid washing-out of the PSLs up to fields as low as 10 % of $B_{c2,NbSe_2} \approx 3 T$ [255].

2.5.2. Thermally activated phase slips

The energy of a Josephson junction is given by

$$U(\phi) = -E_{\rm J}\cos\phi \tag{2.41}$$

when the phase difference between the two superconducting reservoirs is equal to ϕ and $E_{\rm J}$ corresponds to the Josephson energy. A supercurrent

$$I_{\phi} = \frac{2e}{\hbar} \frac{\partial U}{\partial \phi} \stackrel{(2.41)}{=} \frac{2e}{\hbar} E_{\rm J} \sin \phi \tag{2.42}$$

will be obtained if $\phi \neq 0$. Equation (2.43) contains the Ambegaokar-Baratoff formula

$$E_{\rm J} = \frac{\hbar\Delta}{4e^2 R_T} \tanh\left(\frac{\Delta}{2k_{\rm B}T}\right),\tag{2.43}$$

which holds for a tunnel junction between two Bardeen-Cooper-Schrieffer (BCS) superconducting reservoirs with energy gap Δ . Herein R_T is the normal resistance just above T_c . An external current source I can build up a charge difference

$$\frac{\mathrm{d}q}{\mathrm{d}t} = I - I_{\phi} \tag{2.44}$$

giving rise to a voltage difference

$$V = \frac{q}{C},\tag{2.45}$$

where C is the junction capacitance [134].

When the diameter $d \ll \xi(T)$ of a wire with length L is much smaller than the coherence length, variations of Ψ along the diameter can generally be neglected. $\Psi = \Psi(x)$ is then only a function of the position x along the wire for all times. A vortex degenerates to a single point with $\Psi(x) = 0$ whereas a PS represents an isolated point in time and space where Ψ passes through zero and the phase difference along the wire changes by $\pm 2\pi$. Close to T_c , the free energy barrier ΔF^{\pm} , which must be overcome to produce phase

2.5. Resistive states in superconductors

slip, can be estimated by means of the GL free energy functional given (in cgs units) in equation (2.46).

$$F = \int \mathrm{d}^3 \vec{r} \left[-\frac{\alpha}{2} |\Psi|^2 + \frac{\beta}{4} |\Psi|^4 + \frac{\gamma}{2} \left| \left(\nabla - \frac{2ie}{\hbar c} \vec{A} \right) \Psi \right|^2 \right]$$
(2.46)

Here $\alpha, \beta, \gamma > 0$ for $T < T_c$ hold. \vec{A} denotes the electromagnetic vector potential. When the wire is connected to an external current source I, one has to add the expression

$$-\frac{\hbar}{2e}I\Delta\phi\tag{2.47}$$

to equation (2.46). Therein $\Delta \phi$ is the phase difference between the wire ends. For $k = 2\pi n/L \ll \xi$, one receives

$$\Delta F^{\pm} = \Delta F_0 \mp \frac{\hbar I}{2e} \equiv K_0 A \xi f_0 \mp \frac{\hbar I}{2e}$$
(2.48)

for +/- forward/backward phase slips. A is the cross section of the wire and $K_0 = 8\sqrt{2}/3$, $f_0 = \alpha^2/\beta$ hold. One can deduce the pre-factor of the thermal-excited transition rate η in equation (2.49)

$$\eta \propto \exp\left(\frac{-\Delta F}{k_{\rm B}T}\right)$$
 (2.49)

to be

$$\Omega(T) = \frac{0.156}{\tau_{\rm GL}} \frac{L}{\xi} \sqrt{\frac{\Delta F_0}{k_{\rm B}T}}$$
(2.50)

with $1/\tau_{\rm GL} \equiv 8k_{\rm B}(T_{\rm c}-T)/\pi\hbar$. The corresponding contribution to the resistance is given by

$$R = \frac{\pi\hbar^2}{e^2 k_{\rm B}T} \Omega e^{-\Delta F_0/(k_{\rm B}T)}.$$
(2.51)

For a film with thickness $d \ll \xi$, the free energy barrier for nucleation of a vortex can be calculated according to

$$\Delta F \approx \pi K d \log \left(\frac{2eK}{j\hbar\xi}\right). \tag{2.52}$$

Here j represents the external current density and $K = \gamma \alpha / \beta$ holds [134].

2.5.3. Phase slip lines in niobium diselenide

Now, thin 2D superconducting films of thickness d are considered, whose width w is larger than the effective magnetic penetration depth $\lambda_{\text{eff}} = \lambda^2/d$. Herein the formation and flow of Abrikosov vortices in type-II superconductors will lead to dissipation. An external magnetic field can enter the superconductor through the normal conducting zones that pass through it. The normal conducting zones move at a constant speed. They balance the Lorentz force of the superconducting current as well as the viscous force.

2. Theoretical background

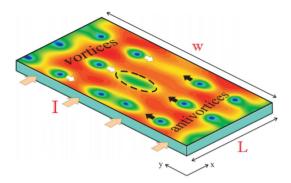


Figure 2.18.: When a DC current I is applied to a 2D superconducting film, vortexantivortex pairs form at the corners. These move towards each other and extinguish in the middle. Graphic taken from [166].

These vortices are considered as quasi-particles with a characteristic size λ_{eff} . Since their size simply exceeds the width of a 1D superconducting strip, as discussed previously, they cannot arise in it [81, 158].

Let us now have a closer look at the regime where the width of the superconducting channel $\xi < w < \lambda_{\text{eff}}$ lies between the coherence length and the effective penetration depth. Since $\xi \ll w$ can hold, 2D dynamics of the order parameter and the current take place. In contrast, w is too small for the formation of Abrikosov vortices within the filament. Abrikosov vortices move with a much slower velocity compared to the kinematic vortices. The formation of the latter is predicted by numerical simulations of time-dependent GL equations. Kinematic vortices are zeros of the superconducting order parameter. They move as vortex and antivortex pairs from the edges of a 2D filament towards each other and annihilate in the middle. This process is visualized in figure 2.18. Depending on the parameters and the geometry of the channel, they will move with an arbitrary velocity [166]. A PSL can be viewed as a series of counter propagating vortex-antivortex pairs having an infinite velocity [26]. This does not imply that the order parameter oscillation must strictly be uniform along the PSL [74]. These superconducting strips show distinct steps in the IV characteristics, very similar to PSCs. Berdiyorov et al. [110] investigated the interplay of Abrikosov vortices with PSLs in strips with a width larger than the coherence length ξ . Abrikosov vortices, triggered by a magnetic field, penetrate the sample in chains in narrow samples or in a triangular lattices for samples having larger dimensions. The whole vortex lattice shifts due to the Lorentz force when a current is applied. Given a current sufficiently large, Abrikosov vortices enter and pass through inducing a tiny voltage jump thus causing dissipation. Instantaneously, the vortex lattice is rearranged and rows of vortices are formed. With further increasing current PSLs (as vortex channels) appear inside the sample. Hence, PSLs and Abrikosov vortices coexist. However, if one wants to observe PSLs experimentally, the formation of Abrikosov vortices should be avoided [110].

A few years ago, our research group started with the transport characterization of

2.5. Resistive states in superconductors

few-layer NbSe₂. The first results of two- and four-terminal measurements were reported in reference [255]. In this work, few-layer NbSe₂ was dry-stamp-transferred onto Ti/Au contacts that had been fabricated in advance. A protection layer of hBN against oxidation on top plays the role of an efficient heat sink since the *IV* characteristic could be smeared otherwise. Investigated were the low temperature transport properties of few-layer NbSe₂ in the clean 2D regime ($l > \xi_{GL} > d$) at high current bias values. The edge roughness is in the order of 1 nm and thus smaller than it could be when formed with EBL. Thus the energy barrier at the edges is sufficiently high to prevent Abrikosov vortices from forming. Consequently, PSLs should dominate the transport for currents far below the pair breaking current [255]. Figure 2.19 presents the experimental results. Figure 2.19(d) shows the differential conductance measured between contacts 1 and 5 as a function of both temperature and current. At low temperatures, one observes several dips while increasing the current. The evolution of one of these dips with increasing temperature is exemplified by a dashed black line and follows the phenomenological dependence

$$\frac{\Delta(T)}{\Delta(0)} = \tanh\left(1.74\sqrt{\frac{T_{\rm c}}{T}} - 1\right),\tag{2.53}$$

as a correction to the BCS theory. The steps in conductance are attributed to the sequential nucleation of PSLs near the contact interface at voltage bias of the order of many times Δ_{NbSe_2} . Also characteristic of PSLs is that already at a perpendicular magnetic field of 300 mT, i.e. only ~ 10 % of the critical field $H_{c2} \approx 3 \text{ T}$ [177], the dip structure gets completely washed out. They developed a model for the qualitative understanding of the high bias behavior $(I > 12 \,\mu\text{A})$. Figure 2.19(b) shows a schematic drawing of the area around contact 5. They state that the overlapping Au area, which is highlighted with a black dashed line, has to be at least partially proximitized, since a low transparency contact would lead to a much lower subgap conductance. On the contrary, the critical current in this area is lower than in the rest of the crystal. An increase of the current will hence turn this area normal first, corresponding to the first step in the conductance plot. The position x = 0 corresponds to the normal conductor-superconductor interface. If this region becomes normal conducting, then there is a pure normal current exclusively. The charge imbalance equilibration length Λ_q is the characteristic length scale over which the normal current is transformed back into a supercurrent by means of inelastic scattering, described by the nominator in equation (2.54). For this situation, one can deduce a time-averaged supercurrent density

$$\langle J_{\rm s}(x) \rangle \propto \frac{1 - \exp\left(-x/\Lambda_q\right)}{w + 2h + \pi x},$$
(2.54)

where x denotes the distance from the contact, h the length of the overlap region and w the width of the contact. The expression of equation (2.54) is plotted in figure 2.19(c). The denominator takes into account the widening of the cross sectional area. This is schematically represented as a red line in figure 2.19(b). At a distance of $x = \Lambda_q$ from the contact, the maximum superconducting current density is reached for the first time

2. Theoretical background

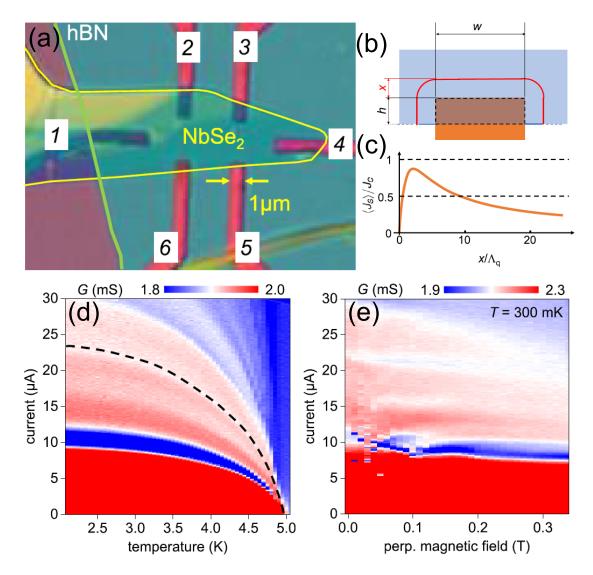


Figure 2.19.: (a) Optical image of the sample. A few-layer $NbSe_2$ flake is stamptransferred onto pre-patterned Au contacts, labeled from 1 to 6. The device is covered with a hBN flake. The time-averaged model of the critical current density around contact 5 is presented in subfigures (b) and (c). The sample shows the characteristic converging of PSLs with increasing temperature (d) and suppression with perpendicular magnetic field (e). Taken from [255].

2.5. Resistive states in superconductors

and a first PSL is nucleated. As soon as the critical current density is exceeded again, a new PSL is generated. The nucleation of PSLs occurs mainly near the contact on a length scale of $L = w + 2h + \pi x$, since $\langle J_s(x) \rangle$ decreases strongly with distance x. The model in reference [15] for PSs in homogeneous wires can be applied to a system of ninteracting PSLs confined to a length L giving a differential resistance of

$$R_{\rm PSL}^{(n)} = R_0 \frac{2\Lambda_q n}{L} \tanh\left(\frac{L}{2\Lambda_q n}\right).$$
(2.55)

In this equation (2.55), $R_0 = \rho L/A$ is the low temperature resistance in the normal state and $R_0 = \rho/(d\pi) = R_{\Box}/\pi$ holds otherwise. R_{\Box} is the sheet resistance and is 66 Ω for a trilayer of NbSe₂ [18]. In extended flakes, the nucleation of a single PSLs can be caused by the mechanical stress of an underlying trench. The novelty of these measurements was that PSLs were observed well below the critical temperature [255].

2.5.4. (Quantum) phase slips in hybrid materials

Nanowires made from CNTs sputtered with MoGe (diameter 10 to 22 nm, length 0.1 to 1 µm) show an increasing broad resistive transition while the wire diameter becomes smaller. This effect is related to thermally activated PSs close to T_c and QPSs at lower temperatures [62]. In the case of QPSs, the question is how narrow a superconducting wire can become until it gets completely resistive due to an overwhelming flow of PSs [74]. A constriction is patterned in a MoGe film and shows with decreasing temperature two different resistive transitions. One is a Berezinskii–Kosterlitz–Thouless (BKT) related one, the other is a crossover which corresponds to the freezing of thermally activated PSs localized inside the constriction. The width of the constriction is of the order of the coherence length of ~ 25 nm. The constriction behaves independent of the banks. The PS rate increases when the width gets smaller since this correspond to smaller interactions with the banks [77]. In MoGe film structures paired QPSs were reported. They are parity conserving and change the winding number by 4π [176]. QPSs and number-phase duality was observed in disordered TiN nanostrips [261].

Now that we have armed ourselves with the most important theoretical background knowledge in this chapter 2, we will look at some important experimental techniques in the following chapter 3.

3. General experimental techniques

This chapter 3 will give a short overview of the various experimental techniques that were applied in this thesis in order to be able to fabricate and characterize our devices via transport measurements at room temperature as well as at low temperatures. In section 3.1, several CNT synthesis techniques are introduced as well as the main standard growth models of CNTs. The basic operation of the low temperature generation mechanisms used for the transport measurements are described in section 3.2. The measurement techniques are presented in section 3.3.

3.1. Carbon nanotube synthesis

In this section, the growth of CNTs by arc discharge, laser ablation and CVD are described. The latter technique is applied in the context of this thesis. In addition, growth models of CNTs are discussed in subsection 3.1.4.

3.1.1. Growth of carbon nanotubes via arc discharge

This growth method yields high quality SWCNTs and MWCNTs (typical diameter 5 to 30 nm and length $\sim 10 \,\mu\text{m}$) by vaporizing C atoms through a He plasma. A high current is passed from a C anode (with e.g. Co catalyst for SWCNTs) to a cathode. Growth is followed by purification with O₂ plasma [23, 35, 58, 89, 95]. A schematic growth setup is shown in figure 3.1(a).

3.1.2. Growth of carbon nanotubes via laser ablation

An intense laser pulse is applied to a C target with catalyst particles in a 1200 °C hot furnace. C atoms are removed by ablation. The flow of an inert gas through the quartz tube during the growth process allows the grown CNTs to be collected at the colder end of the tube [58, 95, 178]. Figure 3.1(b) shows schematically the structure of a laser ablation growth furnace. Note that for the growth of MWCNTs, neither the arc discharge nor the laser ablation method requires a catalyst, whereas for the growth of SWCNTs nanoparticles of transition metals such as Fe, Ni or Co are required. Often two of these elements are also used to improve the growth result [40, 58].

3.1.3. Growth of carbon nanotubes via chemical vapor deposition

CVD is a commonly used experimental technique for CNT synthesis. In this process, metal particles catalyse the thermal decomposition of a hydrocarbon feedstock and

3. General experimental techniques

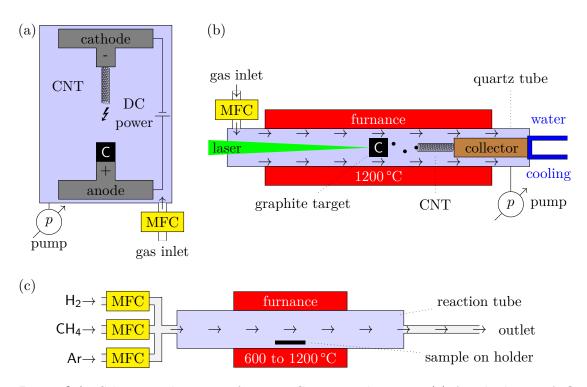


Figure 3.1.: Schematic diagrams of various CNT growth setups. (a) Arc discharge: A C anode is located in a reactor filled with plasma. An arc discharge causes CNTs to grow on the cathode. (b) Laser ablation: A C target is placed in a heated plasma tube. C is detached by means of intense laser pulses. CNTs grow on the water-cooled collector. (c) A CVD setup used in our group. A substrate with catalyst particles is located in a quartz tube inside a furnace. The flow of the process gases is controlled by mass flow controllers (MFCs). We use CH_4 , H_2 and Ar as process gases. Drawn according to [89, 123, 178, 197].

enable the growth of CNTs. The advantages of CVD compared to laser ablation and arc discharge methods are the low setup costs, high yield, upward scalability, the ability to use hydrocarbon in solid, liquid and gaseous state. High purity of CNTs, a wide choice of substrates and better control of process parameters make this growth method attractive. However, the CNTs have a poorer crystallinity [73, 123].

Figure 3.1(c) shows a schematic sketch of the CVD setup used in our group. In our CVD process, a $Si++/SiO_2$ substrate with catalyst particles (catalyst solution or thin Co films) is placed into a quartz tube located in a furnace. From one opening of the quartz tube, the process gases can flow in and, at the other end, they can escape into the exhaust. The gas flow rates are controlled by means of MFCs. In addition to CH_4 as C raw material, we could also use acetylene for the growth of MWCNTs. Furthermore, ethylene, acetylene, benzene, xylene, cyclohexane and fullerene were reported in literature [58, 123] as alternative C feedstock. The furnace can typically reach temperatures between 600

3.1. Carbon nanotube synthesis

and 1200 °C needed for the thermal decomposition of the hydrocarbon feedstock into the catalyst and the subsequent CNT growth. While temperatures between 600 and 900 °C favor the growth of MWCNTs, SWCNTs grow at higher temperatures between 900 and 1200 °C [123]. In general, higher temperatures seem to increase yield, length and quality of the CNTs [68]. The reactor volume is kept oxygen-free by evacuation or by a flow of an inert gas, such as Ar, during heating and cooling [123]. An H₂ atmosphere stabilizes the structure by terminating an open covalent bond through an H-atom. Furthermore, H₂ reduces the catalyst surface [54]. Nanoparticles (on an AI support material) or thin films of transition metals such as Fe, Co, Ni or their compounds are widely used as catalysts [58, 168]. C can be easily dissolved in these elements at sufficiently high temperatures. The elements have a high melting point, a high carbon diffusion rate and a low equilibrium vapor pressure. Cu, Au, Ag, Pt and Pd are also used as catalysts. All these substances can also be used in the other growth processes. Note that the melting point of the particles or films decreases dramatically with decreasing particle size or film thickness [27, 43, 123].

Also inorganic materials such as MoS_2 , BN, WS_2 and V_2O_5 can form nanotubular structures. They can be grown by chemical vapor transport (CVT). A fine powder of the starting material is applied to the hottest point of an evacuated quartz tube together with Br_2 or I_2 as transport aid. A temperature gradient of 20 to 50 °C is maintained at one end of the tube. After about two weeks, inorganic nanotubes will be formed at the colder end. Due to the two-week growth period, it is difficult to scale up and optimize this method [30, 32, 55, 58].

3.1.4. Growth models

Even after thirty years of research, the exact growth process of CNTs is still controversial. Two generally accepted growth mechanisms are shown in figure 3.2 [23, 24, 123]. Hydrocarbon (C_xH_y) is split exothermically into H₂ and C by contact with a hot catalyst

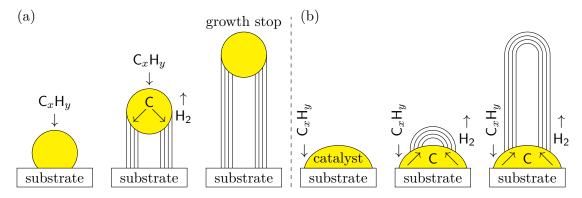


Figure 3.2.: Schematic sketches of two different generally accepted growth mechanisms for CNTs. In (a) the catalyst nanoparticle is lifted (tip-growth) whereas in (b) the CNT grows out of the particle (base-growth). Drawn according to [16, 123].

particle. H_2 migrates into the vent whereas carbon is stored in the metal. Once the

3. General experimental techniques

maximum solubility of carbon in the metal is reached, C leaks out and crystallizes endothermically as CNTs. The temperature gradient of both processes maintains growth. Figures 3.2(a) and (b) show the situation when the adhesion between catalyst and substrate is weak or strong, respectively. In the first case, we speak of the so-called *tip-growth*, in which the catalyst particle is lifted off the substrate. The growth process continues until the surface of the catalyst particle is completely covered with carbon. The second case is called *base-growth*. In this case, the dome-shaped end is formed first before the actual CNT is formed. In both situations, C migrates both through the metal and on its surface to build the CNTs [58, 123]. It is still under debate if the CNTs grow capped or not [40].

If the size of the nanoparticles or the roughness of the catalyst film is in the range of $\sim 1 \text{ nm}/\sim 10 \text{ nm}$, SWCNTs/MWCNTs will grow preferably. The substrates used, such as graphite, Si, SiO₂ and SiC, can also influence growth results [58, 123].

Since the same catalysts are used in all three growth processes presented above, it is highly probable that the same growth process for SWCNTs is used for different C starting materials. The fact that SWCNTs never grow without catalysts but MWCNTs do, may indicate that two different growth processes are underway for the two species [58].

As already explained in chapter 2, many properties of the CNTs depend strongly on their respective chirality. For a particular experiment, it would therefore be desirable to use CNTs of a defined chirality. In recent years, several techniques have been developed for this purpose but none have been able to establish themselves. One method uses complex hydrocarbon precursor molecules that form an initial cap of a CNT of a given chirality under annealing. The actual nanotube then grows by epitaxial elongation through the incorporation of C atoms [171]. Another method uses a special catalyst mixture of W and Co. Its melting point is so high, even for thin films, that the catalyst retains its crystalline structure at CVD temperatures and from this, CNTs of defined chirality can be grown. Yet another method is based on the cutting of a given CNT [174, 193].

3.2. Cooling techniques

This section briefly discusses the cooling systems used in this thesis for performing low-temperature transport measurements. For almost all cooling techniques that reach temperatures below 10 K, use, at least as a pre-cooling stage, the cooling power released during the evaporation of liquid 4 He.

The physics department of the University of Regensburg has its own ⁴He liquefaction plant. Liquid N_2 , which is used in outer heat shields in certain setups, is delivered already liquefied. The transport of the cryogenic liquids from the output to the measurement setup is done by means of dewar vessels [101, 148] with a capacity of 100 L and 160 L, respectively. The transfer of the liquids to the measurement setups is carried out by means of transfer rods and overpressure inside the dewar vessels. On the one hand, evaporated ⁴He is collected by means of return lines and liquefied again. On the other hand, liquid N₂ evaporates into the environment.

3.2. Cooling techniques

3.2.1. ⁴He dip stick with additional ⁴He 1K-pot

A typical setup for transport measurements at 4.2 K in a ⁴He bath is shown in figure 3.3(a). Pumping out the evaporated ⁴He makes the temperature range between

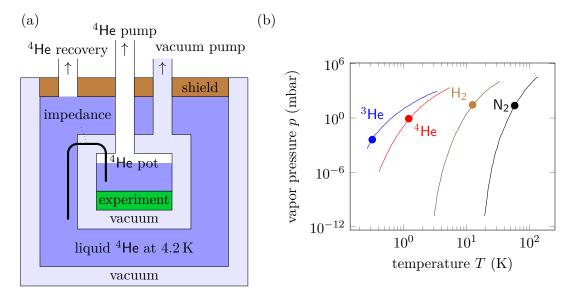


Figure 3.3.: (a) Schematic drawing of a ⁴He cryostat with which one can reach temperatures of liquid He which is 4.2 K at normal pressure. Temperatures in the lower 1 K range can be achieved with an additional ⁴He 1 K-pot. (b) Vapor pressure curve of some cryogenic materials. The bullets in the T(p) diagram indicate the in practice lowest achievable temperatures. Drawn according to [85, 101].

1.3 and 4.2 K accessible. The vapor pressure curves of some cryogenic materials are shown in figure 3.3(b). In our system, this is realized by a so-called 1 K-pot. Through a flow impedance, a small amount of liquid He is continuously flushed through a small volume inside the cryostat vacuum. Pumping the gas phase of this volume is more efficient than pumping the large He bath. This is shown schematically in figure 3.3(a). Such a setup can be operated both in an He transport vessel or in a separate dewar. In the latter case, liquid He can be refilled and the experiment can thus be operated longer. Heating of the samples up to ~ 20 K is done by means of a heating element. Our setup reaches a base temperature of 1.3 K. It is used for fast characterizations or for samples with relatively high critical temperatures in the Kelvin range. The separate dewar is equipped with a superconducting coil that can be used to generate magnetic fields up to 12 T. Radio frequency (RF) filtration is provided by room temperature π filters. The samples can be mounted so that the magnetic field points either in-plane or out-of-plane.

3.2.2. ³He system

To achieve temperatures down to 300 mK, the ³He isotope is used, which has a much higher vapor pressure than ⁴He at the same temperature (see figure 3.3(b)). Since ³He is

3. General experimental techniques

very expensive to purchase, it is used only in relatively small quantities and in closed systems. It is liquefied by bringing a ³He pot inside a ⁴He system with 1K-pot into contact with a ~ 1.3 K cold surface. Provided the gas pressure is high enough, the gas will condense. Subsequent pumping lowers the temperature from 1.3 K to 300 mK. The surrounding ⁴He bath required for this cooling technique additionally serves to shield heat entering from the outside and it is used as a heat sink for the cabling. In our case, a cold adsorption pump built into the cryostat was used for the ³He cycle. When the large surface of a charcoal is held at low temperatures above the ³He bath temperature, this pumps the ³He vapor and the liquid ³He remains cold. When the ³He pot is empty, the ³He stored in the charcoal can be released by heating. In practice, this limits the measurement time at 300 mK to about 10 h [101].

3.2.3. ³He/⁴He dilution refrigerator

The previously described cooling techniques make use of the heat of evaporation of the individual He isotopes. The core cooling process of a ${}^{3}\text{He}/{}^{4}\text{He}$ dilution cryostat, in contrast, relies on the heat of mixing of the two He isotopes. One can thus continuously obtain temperatures in the mK range. The relative ³He concentration in a ${}^{3}\text{He}/{}^{4}\text{He}$ mixture will be denoted as x in the following. Let us consider the phase diagram of the He mixture in figure 3.4(c). The transition temperature of pure 4 He is 2.177 K. The Fermi liquid ³He does not become superconducting in the considered temperature range. The socalled "2-phase region" is not accessible for a He mixture for the appropriate temperatures and concentrations. If a mixture with x > 6.6% is cooled below a temperature of 870 mK, a^{3} He rich (top) and a depleted (bottom) phase are formed (see figure 3.4(a)). However, in the ${}^{3}\text{He}$ poor phase, even for the lowest temperatures, at least a concentration of 6.6 % of 3 He atoms is present. The actual cooling process is based on the phase transition of ³He atoms of the ³He rich phase into the dilute phase (endothermic cooling). The cooling capacity is equal to the heat of mixing of the two isotopes. The cooling power of the earlier described cryostats $Q \propto \exp(-1/T)$ decreases exponentially with decreasing T. In dilution cooling, the two specific heats of the He isotopes are of importance for the enthalpy of mixing of the two quantum fluids. Since both specific heats are proportional to T, a quadratic dependence of the cooling power $\dot{Q} \propto T^2$ on the temperature is obtained for the cooling process.

Figure 3.4(a) shows schematically the technical realization of dilution cooling. ³He gas comes from outside the cryostat through a pump and is first precooled from room temperature down to 4.2 K through a ⁴He bath. Afterwards, it is condensed in a second step at ~ 1.5 K. All the cables and tubes are also thermally anchored at this temperature level. The main flow impedance provides the necessary pressure for the incoming ³He to actually condense. The now liquid ³He flows through a heat exchanger, which is thermally connected to the still. The underlying second flow impedance prevents the ³He from re-evaporating. Through several heat exchangers, the ³He is sufficiently cooled and enters the ³He rich phase in the mixing chamber. From the dilute phase, a wider tube passes through the heat exchanger, which in turn is used to precool the incoming ³He. The still is pumped and the ³He gas is returned to the circuit. Thus a continuous

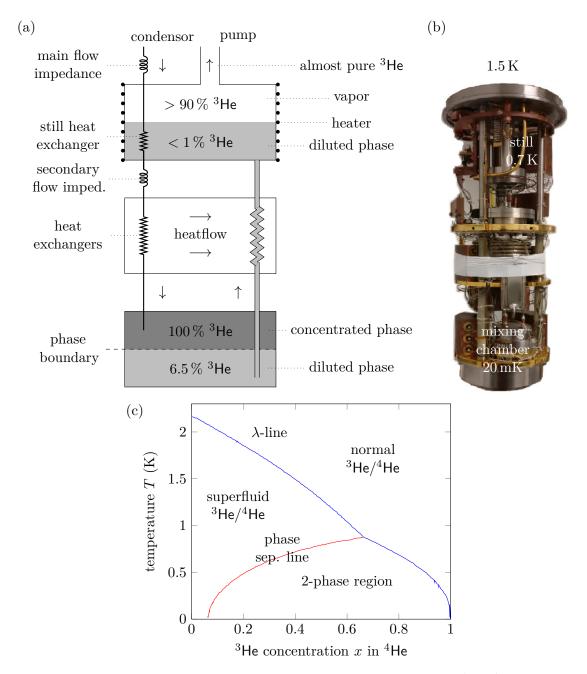


Figure 3.4.: (a) Schematic representation of the cooling mechanism in a ${}^{3}\text{He}/{}^{4}\text{He}$ dilution cryostat. (b) Optical photo of the system we use. (c) Phase diagram of a mixture of liquid ${}^{3}\text{He}$ and ${}^{4}\text{He}$ under saturated vapor pressure. The λ -line of ${}^{4}\text{He}$ separates its normal-fluid and the superfluid regions. Drawn according to [85, 101, 260]. Photo taken from [260].

3. General experimental techniques

cooling circuit is possible [101, 148].

Within the scope of this work, a ${}^{3}\text{He}/{}^{4}\text{He}$ dilution refrigerator from CryoConcept was used providing a base temperature of 20 mK. The 1.5 K temperature level is realized by a Joule-Thomson stage. In addition to the ${}^{4}\text{He}$ bath, an outer bath of liquid N₂ is additionally used to minimize thermal loads. The cryostat is equipped with both room temperature RF π -filters and low temperature copper-powder filters. The magnetic field, up to 15 T, is provided by a superconducting coil. By mounting the specimen appropriately, the magnetic field can be oriented in- or out-of-plane to it. The mixture is cleaned in a N₂ trap outside the dewar at room temperature [143, 260].

3.3. Transport measurement techniques

This section briefly introduces the transport measurement techniques used in this thesis. The setups used for a quick sample characterization at room temperature are discussed in subsection 3.3.1. In the following subsection 3.3.2, we present the low temperature measurement circuits.

3.3.1. Room temperature transport characterization

After sample preparation is completed, the contact resistances of two leads each are determined at a probe station at room temperature. The two-point measurement setup used for this purpose is shown schematically in figure 3.5(a). The DC bias voltage $V_{\rm SD}$ is provided by a Yokogawa 7651. The current through the device is amplified by a current-voltage amplifier (Ithaco 1211 Current Preamplifier) and converted into a voltage which is read by a multimeter (Agilent HP 3458A). If necessary, the gate voltage $V_{\rm G}$ is provided by a Yokogawa GS200 and connected to the Si++ substrate below the SiO₂ layer in order to electrostatically modulate the carrier density of the sample. Since the bias voltage drops mainly at the contacts, primarily tunnel phenomena can be observed. A high contact resistance can be intrinsic or result from a contamination of the contact surfaces as well as from the granularity of the contacts. For the observation of intrinsic properties, samples with lowest possible contact resistances have to be used. The contact resistance can be improved, for example, by heating the metal contacts [58, 143].

When a sample has provided reasonable results at the tip measurement station, it is glued into a 20 pin LCC chip carrier with polymethyl methacrylate (PMMA) or Ag conductive paste. Bond wires are used to electrically connect the pins to the leads. In order to contact the doped Si to a specific pin, the pin can be connected to the bottom of the carrier via a drop of Ag conductive paste. Alternatively, the overlying SiO_2 can be scraped off with a diamond scriber. A bonding wire is then placed on this spot from an empty pin. Ideally, promising samples should be mounted in a cryogenic setup very promptly after bonding. If this is not possible, the samples should be stored in the dark, preferably in a cool place, in vacuum and grounded.

3.3. Transport measurement techniques

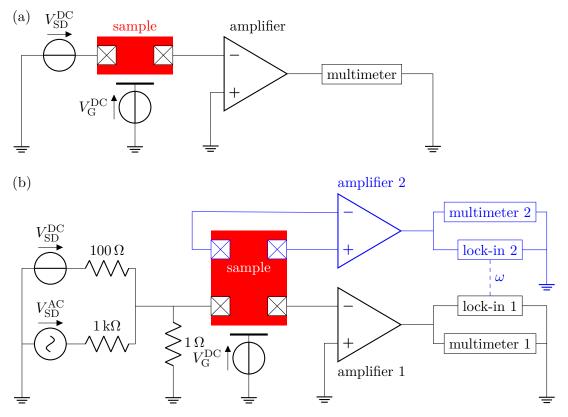


Figure 3.5.: (a) Measurement setup for a quick two-terminal sample characterization at room temperature. (b) Setup for transport measurements at low temperatures. The components drawn in black show the configuration for a two-point measurement. This can be extended to a four-point measurement as required with the components drawn in blue.

3.3.2. Low temperature transport characterization

The measurement setups used at low temperatures are schematically drawn in figure 3.5(b). In it, all relevant components necessary for two-point measurements are drawn in black. We performed two-terminal measurements using a combined voltage excitation of an alternating current (AC) signal provided by a *Stanford Lock-in amplifier SR830* (27.77 Hz) mixed with a DC signal from a *Yokogawa 7651* DC voltage source with voltage division factors of 1000 and 100, respectively. The current is converted back into a voltage signal and amplified by a *Femto Ampere Current Amplifier DDPCA-300*. The AC component is detected with the same lock-in amplifier, whereas the DC part is measured with a *Keysight 3458A Digital Multimeter*. Additional gates are each biased with another *Yokogawa 7651*. This setup can be extended to four-point measurement with the components shown in blue in figure 3.5(b). The voltage drop is amplified by means of a *Femto Voltage Amplifier DLPVA-100*. Its DC component is measured with an *Agilent HP 34410A multimeter*. The AC component is detected with a second lock-in amplifier coupled to the

3. General experimental techniques

first one with respect to its frequency. If not stated otherwise, all contacts not involved in measurement are kept floating.

All relevant measuring devices are connected to each other and to the measuring computer by means of general purpose interface bus (GPIB) cables. Driver suites Lab::Measurement and Lab::Moose [257] written in *Perl* were used for automated control of the measurements. The data analysis was performed using *Igor Pro*, *OriginLab*, *QtiPlot* and *Microsoft Excel*.

In this chapter 3, we have learned the main adjusting screws for the growth of CNTs. In addition, the basic operation of the cryogenic equipment used in this thesis was explained in detail. Furthermore, the techniques for the transport measurements were presented.

With this knowledge introduced, as well as the theoretical background in chapter 2, it is now possible to understand the fabrication method of *array stamping of CNTs* and the associated measurement results in the following chapter 4.

4. Array stamping of carbon nanotubes

In this chapter 4, an alternative approach to the fabrication of devices based on CNT-QDs in the low disorder regime is presented. The fabrication method consists of growing CNTs on a transparent SiO_2 chip and stamping them on an array of tens of devices with prepatterned leads. The growth chip and the electrode chip are designed in such a way that during the stamping process the CNTs do not touch any substrate and stay suspended on the electrodes. The parallel transfer of tens of CNTs highly increases the average number of usable devices per chip. The resulting CNT-based devices are characterized via transport measurements at different temperatures down to the mK-regime. The separation of growth chip from the electrode chip allows one in principle to freely choose the material for the electrodes, opening the way for the implementation of CNT-based devices with superconducting or ferromagnetic leads.

This work was initially pioneered by Korbinian Mühlberger [201] and Julian Heger [214], two former master students of our group. However, it was only within the framework of this doctoral thesis that this procedure was brought to reliable function.

Section 4.1 will give a basic introduction to the various CNT-QD fabrication methods and will point out the advantages of stamp transfer over conventional techniques. In the next section 4.2, the sample processing as well as the stamp transfer process will be presented. The results of the transport measurements are discussed in section 4.3.

4.1. Why stamping of carbon nanotubes?

Many fields of physics drive interest in clean CNT devices. This ranges from technological transistor application and eventually the carbon nanotube microprocessor [250], coherent quantum devices and the application as qubits [99] all the way to nanomechanics [113] and the fundamental physics of electron-electron interaction [47].

There are two different conventional techniques for the fabrication of CNT-QD devices. The first one is a top-down approach as illustrated in figure 4.1(a). CNTs are grown on a flat substrate and are afterwards located using scanning electron microscope (SEM) or atomic force microscope (AFM) imaging. Subsequently, the electrodes are designed on a suitable CNT by means of standard nanofabrication. This method is straightforward, allows application of all materials available for nanolithography and was used for the fabrication of the early devices [37, 57]. However, CNTs will interact with the substrate [41] and in particular with surface charges of the amorphous SiO₂. While this can be avoided by underetching the active device regions [97], a second disadvantage remains: contamination via C deposition during EBL and resist residues. Both, random potentials and residues cause disorder in the CNT and thus make the observation of fine

4. Array stamping of carbon nanotubes

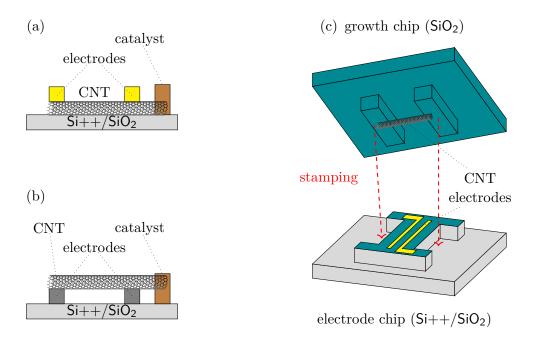


Figure 4.1.: Conventional CNT-QD device fabrication: (a) Top-down approach. (b) Overgrowth technique. (c) Basic idea of our stamping approach: A transparent SiO_2 stamp (two pillars with a CNT grown across) is glued on a glass plate and is mounted upside down in a mask aligner used for optical lithography (OL). With the help of the latter, the alignment to the electrode chip is performed. The depicted structure on the growth and electrode chip is fabricated 45 times per sample.

structures in transport measurements impossible [58, 79, 165].

The development of the so-called overgrowth method represented a significant improvement in sample preparation with respect to low disorder [83]. The electrode structure is manufactured first. Subsequently, CNTs are grown in situ on top of the metallic structures from closely placed catalyst points as visualized in figure 4.1(b). Furthermore, CNTs remain suspended above the substrate surface. However, in this case the choice of electrode materials is severely limited since the metallic thin films have to survive the high-temperature CVD growth process, i. e., standing gas temperatures between 600 and 1200 °C for 10 to 30 min [123]. So far, successful experiments are limited to W/Pt, Re or MoRe alloys [75, 115, 194]. As a result, clean Coulomb blockade transport spectroscopy [253] as well as high quality factor mechanical resonators and strong interaction between vibrational motion and single electron tunneling were reported [116, 165, 199, 246].

Recently, further techniques have been developed, where electrode fabrication and CNT growth are done on two different chips. The CNTs are transferred to the electrodes before measurement. In this way, one overcomes all the above mentioned disadvantages of the standard methods and one can in principle design superconducting and ferromagnetic contacts on CNTs. As long as the growth and electrode chip geometries match, there are no restrictions for the chip design and various implementations of stamping are thinkable. The success of a stamping process is often in situ characterized by transport measurements, sometimes even at low temperatures. The techniques broadly fall into two classes – either a controlled deposition of single CNTs [129, 146, 161, 173, 181, 228] or bulk transfer of CNTs into multiple devices [86, 182].

Here, we use the latter strategy. Our sample layout is sketched in figures 4.1(c) and 4.4(b). We parallelize the transfer of CNTs from growth chip to electrode chip by stamping an entire array of 45 CNT-QD-devices at once. We thus maximize the yield of devices available on a single chip for transport measurements. In the overgrowth method or stamp transfer technique, an imaging method for the CNTs is not necessarily required because it can be electrically verified that one or more CNTs have grown or transferred over the electrode structure [260]. This stamping approach is consequently not deterministic. A prediction on which devices and in which position of the long electrodes the CNTs have been transferred is impossible.

4.2. Sample fabrication and stamping procedure

4.2.1. Growth chip fabrication

Since SiO₂ is transparent and chemically and physically stable under CVD conditions, it is used as a growth (and stamp) chip raw material. Figure 4.2 sketches the fabrication steps for the growth chip. On an $8 \text{ mm} \times 8 \text{ mm}$ SiO₂ piece, we define via OL a mask

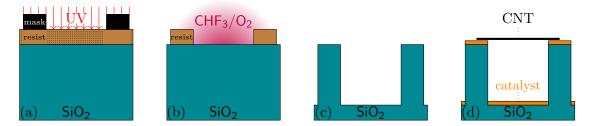


Figure 4.2.: Schematic visualization of the production of the SiO_2 growth chip. (a) An etch mask for the 45 double plateaus is defined on an SiO_2 piece covered with optical resist using OL. (b) In a RIE process, the SiO_2 is anisotropically etched using CHF_3/O_2 as process gases. (c) After removing the optical resist, the plateaus are about 6 µm high. (d) The CNT growth catalyst dispersion is applied globally to the entire chip surface for subsequent growth of CNTs from one plateau to the next in the CVD furnace.

on a triple optical resist (thickness ~ $21 \,\mu$ m, see panel (a)) for an anisotropic RIE process as visualized in figure 4.2(b). For the RIE process, CHF₃/O₂ with flow rates of $50 \,\text{sccm}/6 \,\text{sccm}$ at a pressure of $55 \,\text{mTorr}$ and a power of $150 \,\text{W}$ are used. Typically, to etch SiO₂ 6 μ m deep, a total etch time of 5 h is necessary, interrupted every 30 min by 10 min of pumping out the chamber in order to keep the etching rate controllable and to

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completely remove the etched material. This results in an array of 45 double plateaus of height 6 µm (single plateau width 80 µm, single plateau length 200 µm, distance between the two plateaus 20 µm). In the master's theses preceding this project [201, 214], this geometry was identified as the most promising one. The plateaus on the growth chip should be $\sim 2 \mu m$ higher than their corresponding counterpart of the electrode chips where the prepatterned contacts will be fabricated on. This will prevent the electrode structures from damage. After removal of the resist layer (see panel (c)), we globally drop-cast our catalyst suspension for CNT growth via CVD on the SiO₂ growth chip (see panel (d)). Here, a final lift-off is not performed. The solution is intentionally applied to the entire chip. CNTs are grown via CVD at 1040 °C for 20 min. CH₄ is used as C feed stock (flow 10 sccm) and H₂ as carrier gas (flow 20 sccm). The interior of the reaction tube is kept O₂-free during heating and cooling by an argon flow of 1500 sccm [98, 123]. For fabrication details see appendix B.

4.2.2. Electrode chip fabrication

Figure 4.3 schematically shows the fabrication steps for the electrode chip. On a $4 \text{ mm} \times 4 \text{ mm} \text{Si}_{++}/\text{SiO}_2$ chip with a dry thermal oxide thickness of 500 nm, we define by OL a mask for an anisotropic RIE process. CHF_3/O_2 (50 sccm/10 sccm, 55 mTorr, 150 W) and CHF₃/SF₆ (3 sccm/5 sccm, 25 mTorr, 40 W) are used as process gases for etching SiO_2 and Si, respectively. This results in an array of 45 mesa structures, i.e., dumbbell-shaped plateaus of height 2.5 µm (protrusion width 15 µm, protrusion length $245 \,\mu\text{m}$). To avoid accidental electrical shortcuts between CNTs and the etched substrate. we deposit 500 nm of amorphous SiO_2 via PECVD. For the same purpose, we deposit after the lift-off 20 nm of insulating Al_2O_3 via ALD. It turned out that such a leakage current was a significant challenge for this project. Unfortunately, this effect only became visible at low temperatures. As a last step, we fabricate two long electrodes from 20 nm Ti and 100 nm Pt via EBL and metal deposition on top of the ridge (lead width 500 nm, distance between leads 750 nm). The bond pads on each side have a size of $100 \,\mu\text{m} \times 100 \,\mu\text{m}$. The height of the electrode materials is chosen in such a way that a transferred CNT remains suspended and does not touch the SiO_2 surface. Si++ is used as a global backgate down to mK temperatures. For fabrication details see appendix B.

4.2.3. Carbon nanotube stamp transfer procedure

Figure 4.4 schematically illustrates the CNT stamp transfer process. The growth chip is glued face-down on a glass plate with PMMA and mounted similar to an optical mask in a Karl Suss mask-aligner usually used for OL. The electrode chip is placed face-up in the position of a regular chip just below the growth chip. Growth and electrode chip are aligned relative to each other in several iterations using the micrometer screws (x, y, z, ϕ) of the movable plate of the mask aligner. Alignment here means that the ridge of the protrusion chip is located between the double plateaus of the growth chip for all 45 structures. Then the growth chip is lowered in z-direction onto the electrode chip. Since the height of the double plateaus on the growth chip is about 4 µm larger than

4.2. Sample fabrication and stamping procedure

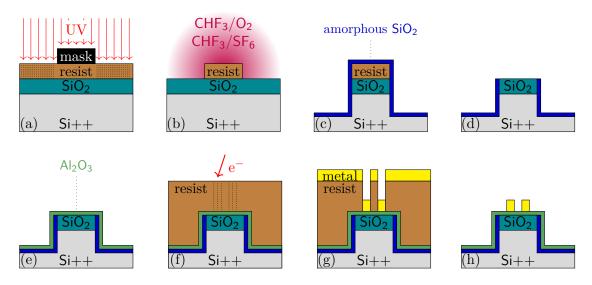


Figure 4.3.: Schematic visualization of the production of the electrode chip. (a) Using optical lithography, a resist deposited on an $Si++/SiO_2$ chip defines an etch mask. (b) In a RIE process, the approximately 2.5 µm high 45 protrusion structures are anisotropically etched out using CHF₃/O₂ and CHF₃/SF₆ as process gases for etching SiO₂ and Si, respectively. (c) To prevent a stamp-transferred long CNT that may extend down the sides of the protrusion from short-circuiting with the Si++ gate later, a layer of amorphous SiO₂ is deposited on the entire chip in a plasma-enhanced chemical vapor deposition (PECVD) setup. (d) Chip after performing the subsequent lift-off. (e) To avoid a short circuit between a CNT with Si++, an additional layer of insulating Al₂O₃ was deposited using atomic layer deposition (ALD) in later samples. (f,g) The electrode structure (20 nm Ti, 100 nm Pd) is defined by EBL and thermal and electron beam evaporation. (h) Finished electrode chip after performing the lift-off.

the electrode ridge, CNTs first touch the electrodes. When rainbow colored interference patterns are seen, both chips touch. Thereupon the growth chip is lifted up again. Transferred CNTs stick to the electrodes via vdW forces and are ripped off the growth chip. An electrode height of 120 nm assures that the successfully transferred CNTs are suspended above the SiO₂ layer between the leads. For details see appendix B.

4.2.4. Stamping results

For statistics, stamped CNTs were located on the electrodes using an SEM. The images in figure 4.5 show typical CNT (highlighted in red) stamp transfer results from the growth to the electrode chip. Figures 4.5(a) to (c) show early results. More than 0.1 mL catalyst solution was added to the growth chips and was hardly blown dry with N₂. Also, the clumped nanoparticles in this solution were crushed only for insufficient time (< 30 min) in an ultrasonic bath. As a result, large clusters of these nanoparticles (height up to $2 \,\mu$ m) were unintentionally deposited on the electrodes, causing either a short circuit of 4. Array stamping of carbon nanotubes

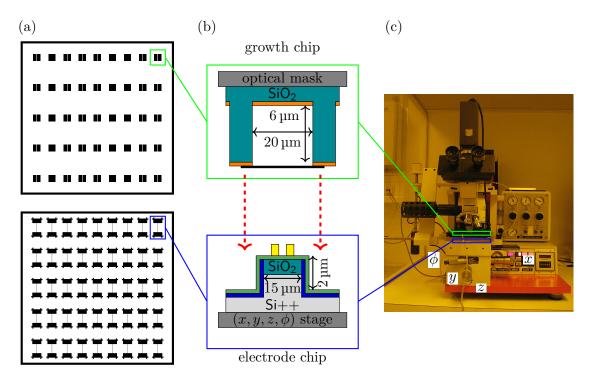


Figure 4.4.: Simultaneous stamp transfer of CNTs in an array of 45 electrode structures. (a) View from top of growth (top) and electrode (bottom) chip. (b) Visualization of the stamping process in side view. (c) The stamping process is performed with a maskaligner normally used for OL. For this purpose, the growth chip is glued onto a blank glass plate with PMMA and mounted upside down as an "optical mask". The electrode chip is located at the site of a regular sample and is held in position using an aspirating vacuum. Its position can be changed with the x, y, z, ϕ adjustment screws. Through multiple iteration, the 45 structures on the two chips can be precisely aligned with each other. CNTs are deposited on the electrodes as soon as the two chips make contact with each other and a rainbow colored interference pattern is observed in the optical microscope.

the two leads or even their destruction. Because of the large amount of catalyst material, the yield of growth and transfer of CNTs are significantly increased (more than ten stamp transferred CNTs per electrode structure) [68]. Failure to align the two chips with sufficient precision relative to each other during stamping can destroy entire sections on them. Therefore, in the initial stamping experiments, at most two of the 45 structures exhibited a reasonably successful transfer of multiple CNTs.

To optimize this method, the catalyst solution amount was iteratively reduced to approximately 0.05 mL per growth chip. Subsequently, the chips were blown dry considerably with N₂. Also, the precision of the alignment has been increased. After all the optimization steps, CNTs are successfully transferred on about 50 % of the structures in this stamping process. On average, 2 to 3 CNTs are transferred onto one contact structure. SEM images of improved stamping results are shown in figures 4.5(d) to (f).

4.2. Sample fabrication and stamping procedure

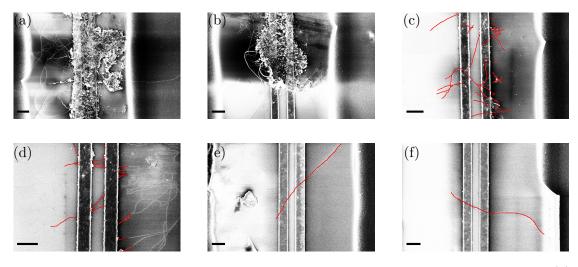


Figure 4.5.: SEM images of the electrode structures after successful transfer of CNTs. (a) to (c) show early results. Large catalyst particles short-circuit or even destroy the leads. Often a large number of CNTs has been transferred. (d) to (f): by reducing the amount of catalyst and by sweetening the alignment during the stamping process, significantly less catalyst material and CNTs are transferred. The black bar in the lower left of each image corresponds to the length of $1 \mu m$. Note that in (e,f) the single transferred CNTs lie completely on the plateau ridge.

For details see appendix B.

4.2.5. Reduction of the contact resistance by annealing in argon atmosphere

Subsequently, the devices are placed into an oven in inert Ar atmosphere at a flow of 1500 sccm for 10 min at 400 °C. This annealing process can occasionally reduce the contact resistances by one order of magnitude. For details see appendix B.4.2.

4.2.6. Reuse of growth and electrode chip

The production of growth and electrode chips, even if some are fabricated in parallel, takes a lot of time. In addition, lack of precision during stamp transfer can completely destroy the structure of individual chips. Therefore, it is only right and proper if intact chips can be reused. The following methods have been developed for this purpose.

After a stamping process, the chips must be inspected under an optical microscope for obvious damage. The growth chips are immersed into a 1.5 molar NaOH base at 40 °C for 2 h. The caustic base etches the SiO_2 surface and thus leads to lift-off of the catalyst particles. The stamped CNTs on the electrode chips on the other hand can be removed in an O_2 plasma treatment, which also burns away other organic residues such as amorphous C from the transfer process. For details see appendix B.5.

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4.3. Transport characteristics

For a room temperature pre-characterization of our devices, we apply a bias voltage of $V_{\rm SD} = 3 \,\mathrm{mV}$ and measure the conductance while sweeping the gate voltage $V_{\rm G}$ from -5 to 5 V as shown in figure 4.6(a). Our devices typically exhibit a resistance of ~ 50 k\Omega

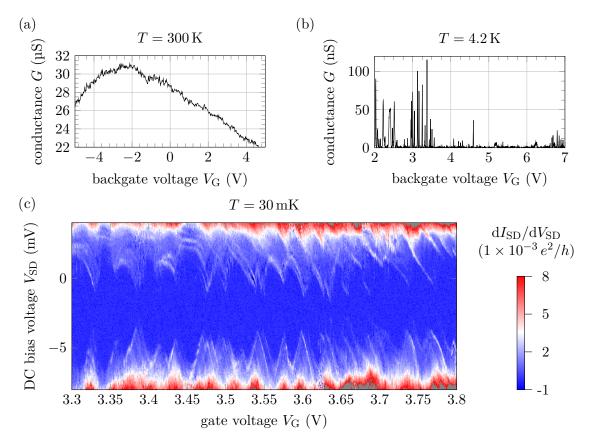


Figure 4.6.: Transport characteristics of sample CB1145 at different temperatures. DC conductance G as a function of gate voltage $V_{\rm G}$ at (a) room temperature and (b) 4.2 K. At room temperature, the conductance varies between 22 and 31 µS as a function of gate voltage. Coulomb oscillations can be observed at 4.2 K. (c) Stability diagram of the same CNT measured at 30 mK: Differential conductance $dI_{\rm SD}/dV_{\rm SD}$ as a function of both, gate $V_{\rm G}$ and DC bias voltage $V_{\rm SD}$.

up to several M Ω varying up to 30 % with the backgate voltage. For a specific device (device CB1145), we repeat this measurement at 4.2 K where we observed Coulomb oscillations as depicted in figure 4.6(b). Figure 4.6(c) shows the differential conductance of a CNT-QD-device as a function of gate and bias voltage measured at 30 mK. We observe overlapping Coulomb diamonds indicating that several CNTs were stamped on this device. By a posteriori SEM imaging, we counted three stamped CNTs on this particular device. The asymmetric shape of the upper conductance peaks stems from

mechanical vibrations of our system. We extract a charging energy of 8 meV.

In this chapter 4, we presented a successfully developed alternative approach for stamping an entire array of CNTs onto prepatterned electrode structures. In the future, we plan to reduce the number of CNTs stamped per device and stamp CNTs on superconducting and ferromagnetic leads. Furthermore, the metallic leads can also be used to amplify the Raman signal of the CNTs. These can also be characterized optically. In total, the stamping process was carried out more than fifteen times.

Now that we have considered pure 1D systems, we will look at 1D-2D hybrid systems in the following three chapters.

5. Fabrication of van der Waals-carbon nanotube hybridstructures

In this chapter 5, some techniques specifically needed for the fabrication of (CNT-) vdW heterostructures are presented. First, the fabrication of reference markers on $Si++/SiO_2$ chips is presented in section 5.1. Then, sections 5.2 through 5.5 highlight all the important details for exfoliation and stamping of vdW crystals. Concepts of encapsulation with hBN are introduced in section 5.6. Section 5.7 summarizes the optimization of CNT growth from Co catalyst films. This chapter is finally completed by the presentation of edge contacts to NbSe₂ and CNTs in section 5.8.

5.1. Chip with basic markers

In a first fabrication step we fabricate an array of reference markers (10 nm Pt on 15 nm ReMo via electron beam evaporation/sputtering), i. e., crosses having a spacing of 50 µm both, in x and y-direction and labeled with numbers on a $4.5 \text{ mm} \times 4.5 \text{ mm}$ Si++/SiO₂ chip (see figure 5.1). These marker serve as reference for subsequent fabrication of catalyst dots, localization of CNTs after CVD growth using a SEM as well as for the hot pick-up transfer of CNT. If the target substrate, onto which the individual components are transferred, does not need to withstand CVD temperatures, 5 nm Ti and 20 nm Au are commonly used as marker materials. At the beginning of this thesis, these marker chips were patterned individually via EBL, and later by OL in an industrial mask aligner on a whole wafer, which resulted in significant time savings.

In a second step, if needed, catalyst dots (nominal diameter ~ 4 µm) are fabricated in the center of four adjacent crosses. As will be discussed further in section 5.7, both the standard catalyst and preferentially thin Co films are used. As it turned out, the geometry described in this way is very advantageous for our project. First, the CNTs grown from the catalyst dots have a sufficient distance to the markers so that the CNTs can be easily picked up or vdW materials can be stamped onto them without the markers getting in the way or inadvertently causing a short. Second, the markers are sufficiently close to each other so that the position of the CNTs can be easily located with a necessary scale bar in the SEM. Furthermore, even at a distance of 50 µm, the stamp and pick-up processes can be performed with sufficient precision when followed live on a television (TV) screen via an optical camera. For fabrication details see appendix C.

5. Fabrication of van der Waals-carbon nanotube hybridstructures

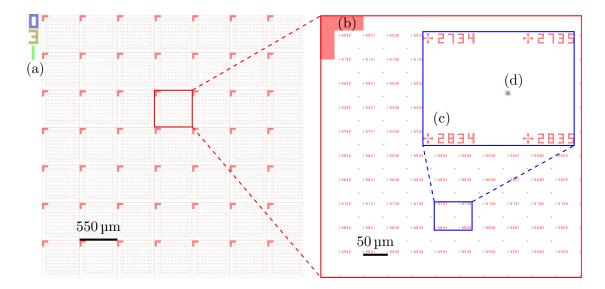


Figure 5.1.: The left half shows the complete patterns for a chip with basic markers (chip size $4.5 \text{ mm} \times 4.5 \text{ mm}$). (a) Name of the sample in the upper-left corner. (b) Angle for alignment and guideline for the eye. (c) Cross with coordinate point, labeling in matrix form. (d) Star-shaped catalyst dot. The corresponding dimensions are indicated.

5.2. Mechanical exfoliation and transfer onto PDMS or SiO₂

Basics for exfoliation have not changed since the graphene breakthrough of Novoselov and Geim in 2004 [80]. Individual layers of a vdW crystal can be isolated with the aid of scotch tape. The fabrication steps described below are shown schematically in figure 5.2. They are identical for graphite, hBN and NbSe₂. In the case of NbSe₂, however, these steps are carried out to avoid oxidation in N_2 atmosphere. Our few mm thick bulk vdW crystals are stored on stripes of white tape (scotch tape) placed on glass slides in N_2 atmosphere. For efficient thinning of bulk crystal down to the few-layer regime, we use the commercially available Blue Nitto-tape SPV 224P. The latter will be called simply blue tape from now on. By bringing the blue tape and the bulk crystal into contact and retracting again, we can pull off several macroscopic portions of the bulk crystal onto the blue tape. This produces the so-called 0th crystal generation. In order to further thin down the crystals, we repeatedly (3-5 times) cleave the crystals using fresh blue tape every time. This results in the subsequent 1st to 5th generations. Which generation is the most promising one, depends on the crystal itself and on the user's experience. Typically, we observe the best results with the 2nd or 3rd generations. The cleaved crystals are then placed on a thin rectangular ($\sim 8 \,\mathrm{mm} \times 8 \,\mathrm{mm}$) layer of viscoelastic PDMS, which in turn is placed on a glass slide. Commercially available gel film from Gel-Pak is used as the PDMS layer. Alternatively, the crystals on the blue tape can also be transferred to a $Si + +/SiO_2$ substrate, depending on which stamping method is to be used later on.

5.3. Stamping setup with glove box

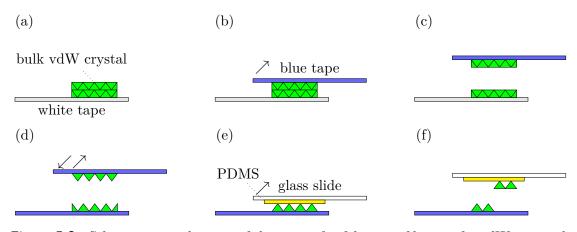


Figure 5.2.: Schematic visualization of the steps of exfoliation of layers of a vdW material from a bulk crystal and their subsequent transfer to a polydimethylsiloxane (PDMS) layer (or a $Si++/SiO_2$ substrate). (a) The bulk crystal sticks to a white tape for storage purposes. (b) A blue tape is carefully applied to the bulk crystal and then quickly peeled off. (c) Some layers of the vdW material remain attached to the blue tape. (d) The layers can be further reduced in height several times by using additional blue tapes. Usually, this step is applied two to four times. (e) A thin PDMS layer was applied to a glass slide. The desired blue tape with the flakes is brought into contact with the PDMS. (f) Some flakes remain on the PDMS layer. In the following, suitable few-layer vdW crystals can now be searched on it with the help of an optical microscope. Drawn according to [167].

Lastly, we search under the optical microscope for flakes suiting our purposes with respect to size, thickness, homogeneity and other surrounding flakes. The contrast allows the approximate thickness of the flakes to be estimated [132]. For details see appendix C.1.

5.3. Stamping setup with glove box

A photograph of the stamping setup used in this thesis is shown in figure 5.3 and it is similar to [167]. This setup is used both for dry stamping and for the hot pick-up technique. If NbSe₂ crystals are used, the glove box is constantly flooded with N₂ so that the O₂ concentration is significantly below 100 ppm [177]. Inside the box, there is a hot plate that can be used to bake the target substrate as well as the flakes on the PDMS to avoid humidity inside the samples as much as possible. Using an optical microscope with magnification levels of $2\times$, $10\times$, $20\times$, $50\times$ and $100\times$, we search for suitable flakes on PDMS or SiO₂ and capture optical images with the connected digital camera. The optical images are stored on the connected computer and serve as a reference for further fabrication steps. The target substrate ($4.5 \text{ mm} \times 4.5 \text{ mm} \text{ Si} ++/\text{SiO}_2$ chip, array of alignment marker with a lateral spacing of 50 µm) is placed on the computer-controlled x, y, z, ϕ -piezo stage before the stamping process begins. Its position is controlled by the computer via a LabVIEW program. The position of the slide is traversed with an

- digital cameras === \mathbb{N}_2 \mathbb{TV} screen optical microscope ---- zoom lens x, y, z, ϕ translational stage \mathbb{R}_2 \mathbb{R}_2
- 5. Fabrication of van der Waals-carbon nanotube hybridstructures

Figure 5.3.: Photo of our stamping setup.

 x, y, z, ϕ -translation stage and monitored on a TV-screen via a second digital camera equipped with a zoom lens. This further allows to observe the stamping process live. For more specific details see appendix C.

5.4. Dry stamping technique

Previous 2D crystal placement techniques were based on wet chemistry and sacrificial polymer layers. Castellanos-Gomez et al. presented an all-dry transfer method [167] which we adopted for our purposes.

The term *dry stamping* will delineate the stamping process as described in the following and as visualized in figure 5.4. A glass slide with a layer of PDMS on it, after 2D crystals have been transferred onto it, is examined under the optical microscope for suitable flakes (size depends on the project but typically a few μm^2 , homogeneity, smallest possible thickness). It is mounted face-down into a micro-manipulator stage and positioned just above the target substrate. The target substrate is usually a Si ++/SiO₂ reference marker substrate. This substrate is cleaned before in a plasma ashing process and is placed on

5.5. Hot pick-up stamping technique

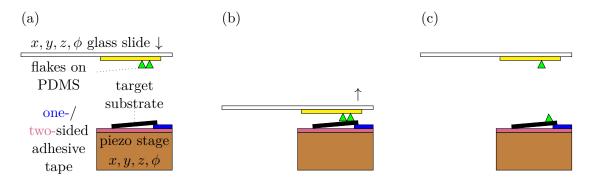


Figure 5.4.: Schematic sketch of the dry stamping process. (a) The glass slide with PDMS layer and the selected vdW flake is clamped upside down in a x, y, z, ϕ -micromanipulator. The target substrate is fixed by a single-sided adhesive tape (adhesive surface facing down) edged onto a double-sided adhesive tape. This is located on a x, y, z, ϕ -piezo stage. Iteratively, the flake and the desired location on the target substrate are aligned. This process can be monitored live on a TV screen via a digital camera with zoom lens. (b) Due to the upstand, the PDMS layer comes into contact with the upper part of the substrate first. This allows the meniscus to slide over the desired flake in a targeted manner. Afterwards, the glass slide is guided upwards again. (c) The desired flake was successfully transferred to the target substrate. Drawn according to [167].

edge on a double-sided adhesive tape on top of the piezo stage. The upturning is made possible by a single-sided adhesive tape. The resulting tilt of the substrate allows better control over the direction of meniscus propagation during the stamping process. The target substrate is placed onto the piezo stack. The latter is used for rough adjustments only. For the actual stamping process, the glass slide is moved down towards the target substrate and the flake to be stamped is aligned using the screws of the translational stage. The substrate and PDMS layer are then carefully brought into contact so that the meniscus can slide over the desired flake in a controlled manner. Once the whole flake has made good contact with the substrate, the moving direction of the meniscus is reversed by retracting the glass slide. When the whole flake sticks, the PDMS is retracted completely. With this technique, one can obtain a sub-um stamp precision. One can use this technique to subsequently stamp multiple flakes on top of each other but since the PDMS comes into contact with previous stamped flakes, the chance of failure or damage increases with each successive stamped flake. Finally, the chip that was stamped on is heated again to 150 °C in forming gas (H_2/N_2) atmosphere to relieve stress and allow gases trapped in the stack to escape [210]. For details see appendix C.2.1.

5.5. Hot pick-up stamping technique

In our group, another stamping method, which we will call *hot pick-up technique* in the following, is used. It is inspired by [162, 175, 189] and allows a sequential picking up of

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several flakes one after the other and their subsequent transfer to a target substrate. This technique is schematically shown in figure 5.5. The stack of flakes sticks together by vdW forces. The contact areas between the flakes remain free of polymers and the number of bubbles can be minimized. In our approach, we apply this transfer method also to CNTs. Flakes of the desired material must first be transferred to a Si/SiO_2 substrate as described in section 5.2. CNTs can be picked up from a separate growth substrate.

A lens-shaped PDMS stamp is covered with a thin PC film. The PDMS lens is fabricated by placing single drops of PDMS base material mixed with a curing agent onto a glass slide and baking for 10 min on a hot plate set to 150 °C. The PC film is fabricated by sandwiching a handful of drops of 5 % PC/chloroform by weight solution between two glass slides. When all the air between the glass slides is expelled, the top glass slide smoothly and quickly removed and an even and thin film of PC/chloroform solution remains on the bottom slide. Placing the slide on a hotplate set to 150 °C for 5 min drives off the solvent. The so produced PC film can be stored in ambient conditions until use. The PC film is transferred onto the PDMS lens using a common scotch tape. First, a hole is punched in the scotch tape with an office puncher. Second, using the scotch tape the PC film is lifted from the glass slide in such a way that it spans over the hole without cracks. The scotch tape with the PC film is fixed onto the PDMS lens by applying more scotch tape.

Temperature control during the procedure is provided using a self-made chip holder made of Cu. It is placed in top of the piezo stack and it is connected to a DC powered heating resistor and a thermometer. When the pick-up or target substrate (Si $++/SiO_2$, reference marker with spacing of 50 µm) is placed on the Cu block, it is held in position by a vacuum pump via a tube-like opening located underneath. We load the glass slide with the PC layer face-down into the micromanipulator stage and position the tip of the PDMS lens above the flake/CNT to be picked up. Before starting the actual pick-up process, the temperature of the Cu sample holder must have a temperature below 50 °C. Failure to do so may cause the PC layer to sag prematurely.

The PC layer is brought into contact with the pick-up substrate about 100 μ m away from the relevant flake or CNT so that they just touch. The Cu block is then heated to 120 °C. The temperature increase softens the PC and it bends down. Once the 120 °C is reached, the flake or CNT will adhere to the PC. The glass slide with lens is then carefully lifted upwards and the heater is switched off. If necessary, with one flake already picked up, several more flakes of each smaller size can be picked up in succession. In order for the stack to be deposited on the target substrate, essentially the previously described steps are repeated with the difference that the Cu block is heated to 180 °C. This completely melts the PC from the PDMS lens. The PC is detached in a chloroform bath. If a CNT was transferred, it is advisable to verify the success of the transfer in the AFM. In this context, the diameter of the CNT or the thickness of the stamped flakes can also be estimated. Furthermore, since CNTs cannot be seen in the optical microscope, their position must be determined as accurately as possible relative to prominent scratches in the PC layer or PDMS lens. With our method, a precession for the hot pick-up of about 5 µm can be obtained.

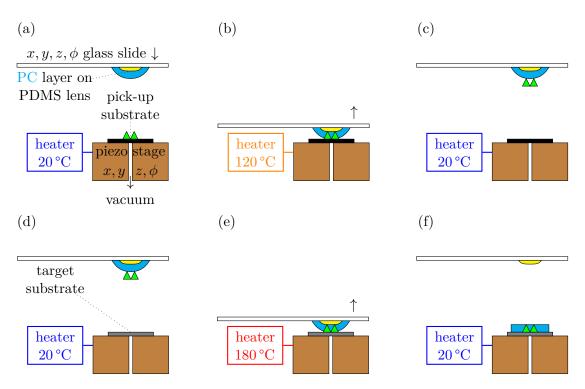


Figure 5.5.: Schematic sketch of the hot pick-up stamping technique. (a) vdW crystals were transferred onto a pick-up substrate. The substrate is held in position on a x, y, z, ϕ -piezo stage, the top end of which is made of Cu, by a suction vacuum. A thin polycarbonate (PC) layer is deposited on a PDMS lens on a glass slide. This structure is mounted upside down in a x, y, z, ϕ -micromanipulator. (b) The glass slide is brought into contact with the pick-up substrate. The Cu block is heated to about 120 °C with a power supply. The temperature is measured with a connected thermometer. (c) Once the 120 °C is reached, the flakes adhere to the PC layer. The glass slide is pulled away upwards again and the heater is switched off. Steps (a) to (c) can now be repeated several times. With the flakes already picked up, further (smaller) flakes can be collected. (d) The final flake stack is brought into contact with the target substrate and (e) now heated to 180 °C. (f) This melts the PC layer with the flakes onto the target substrate and releases it from the PDMS lens. The PC layer is detached by immersing the substrate in chloroform. Drawn according to [162, 175].

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Finally, the chip that was stamped on is heated again to $150 \,^{\circ}\text{C}$ in forming gas (H_2/N_2) atmosphere to relieve stress and allow gases trapped in the stack to escape [144].

In the literature [184, 210] and in our experience, it is almost impossible to pick up a CNT with a hBN flake because the vdW forces between the two are too small. Alternatives reported were the growth of CNTs onto hBN as well as their direct stamp transfer onto hBN [210]. For details see appendix C.2.2.

5.6. Encapsulation of van der Waals materials and carbon nanotubes with hexagonal boron nitride

In the following, *half encapsulation* will describe the situation where a 2D flake or a CNT are encapsulated with a hBN flake only from the top. In contrast, the term *full* encapsulation denotes the situation where the desired materials are encapsulated from both top and bottom with two hBN flakes. In principle, both types of encapsulation can be performed using both stamping methods. As already explained in detail in section 2.1.2, encapsulation with hBN serves to protect the enclosed material.

5.7. Optimization of carbon nanotube growth from cobalt catalyst dots

Up to now, our standard catalyst solution for CNT growth contains $FeNO_3$, MoO_2 and $AlsO_3$ nanoparticles solved in methanol (see appendix A.2.1) [42]. For the optimization of CNT growth via CVD, only the catalysts and the growth quartz tube were varied. All other process parameters were kept constant as described in appendix A.2.3. We use CH_4 (flow 10 sccm) as C feedstock and H_2 (flow 20 sccm) and Ar (flow 1500 sccm) as carrier gases. The growth temperature is set to 20 min.

The SEM images in figures 5.6(g) and (h) show the growth results from catalyst dots for different growth temperatures of 850 °C and 900 °C, respectively [43]. We observe a random growth of several CNTs out from one catalyst dot which often cross each other or grow backwards into the catalyst dot. Higher temperatures increase yield and CNT length. Rarely do CNTs grow longer than a few 10 μ m. Furthermore, we often faced changing growth properties concerning yield and length. Two quartz tubes were used for growth, one of which showed significant C deposits. Mostly this tube showed better results.

The main requirements on CNT growth for CNT-2D vdW hybrid devices are a CNT length of $\sim 10 \,\mu\text{m}$ or even longer in a rather straight growth direction with high reproducibility. Furthermore, the CNTs should be well separated from each other. Nearly none of these requirements can be fulfilled with our standard catalyst.

Hence, we started to use a few nm thin films of Co as a catalyst. In order to optimize the growth parameters, we fabricate an array of catalyst dots (diameter 4 µm, spacing 50 µm) on Si++/SiO₂ substrates via EBL. Co is deposited via electron beam evaporation with a rather slow evaporation rate of $0.1 \frac{\text{\AA}}{\text{e}}$.

5.7. Optimization of carbon nanotube growth from cobalt catalyst dots

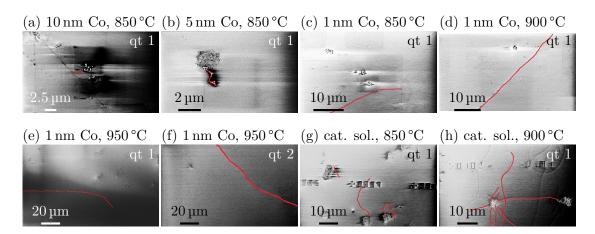


Figure 5.6.: SEM images of typical CNT (highlighted in red) growth results for different catalysts, growth temperatures and quartz tubes. The other CVD parameters were not varied. (a) to (c): By reducing the thickness of the **Co** film from 10 to 1 nm, the yield and length of grown CNTs at a growth temperature of 850 °C. For a film thickness of 20 nm, no growth was observed at all. (c) to (e): Now, if the **Co** thickness is left at 1 nm, the yield and length of CNTs will increase with increasing temperature. (e) and (f): The success of the growth is independent of the quartz tube (qt) used. Within qt 1, in contrast to qt 2, a clear **C** deposition is visible, which may be crucial for the growth success of CNTs from the standard catalyst. (g) and (h): For comparison, growth results using the standard catalyst for two growth temperatures: the number of CNTs per catalyst point is significantly increased. However, these CNTs are significantly shorter and cross each other like spaghetti. "Cat. sol" stands for "catalyst solution".

Table 5.1 illustrates the influence of Co film thickness and growth temperature on yield and length of CNT growth from Co catalyst dots. Figures 5.6(a) to (f) show representative

Table 5.1.: Parameters for CNT growth from Co catalyst dots. The most promisingresults are provided by a Co film thickness of 1 nm and a growth temperature of 950 °C.Temperature (°C)850850850850850850850900950

Temperature $(^{\circ}C)$	850	850	850	850	900	950
Nominal Co-thickness (nm)	20	10	5	1	1	1
Yield (CNTs/dot)	-	1/300	1/200	1/100	1/100	1/100
Typical length (µm)	-	2	2	10	>10	≫10

corresponding SEM images. CNTs are highlighted in red. We used the inlense mode (surface sensitive), a 30 µm aperture and an acceleration of 2 kV.

At first, we kept the growth temperature constant at 850 °C and decreased the Co film thickness from 20 nm down to 1 nm. For 20 nm, we could not observe any growth of CNTs at all. For 10 nm and 5 nm we observe in average one CNT per 300 and 200 catalyst dots respectively. The typical length of a such grown CNT is $\sim 2 \,\mu\text{m}$. Figure 5.6(c) shows that the situation improves by reducing the film thickness down to 1 nm. Here we

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observe one CNT per 100 catalyst dots with a typical length of 10 µm. The CNT length increases > $10 \,\mu\text{m} \gg 10 \,\mu\text{m}$ while increasing the growth temperature to $900 \,^{\circ}\text{C}/950 \,^{\circ}\text{C}$ as visible in figures 5.6(e) and (f).

Overall, the growth direction is rather straight. The individual CNTs are indeed well separated from each other. These growth properties are highly reproducible and are independent on the quartz tube used for the CVD process. Since Co films are at most a few nm high, it is very unlikely that an AFM tip will be demolished during scanning. This was regularly the case with the standard catalyst, which was up to $2 \,\mu$ m high. Furthermore, pure Co is cheap to purchase compared to the other catalyst components and does not age over a period of years. CNTs grow even from Co, even if the growth was performed months after the films were applied. With the standard catalyst, to be successful, the CVD process had to be completed immediately after deposition.

For imaging, SEM was given preference over AFM because a complete $4.5 \text{ mm} \times 4.5 \text{ mm}$ chip had to be scanned in each case. The exposure time was kept as short as possible. After imaging, the growth chips are stored in darkness and vacuum at approximately 1×10^{-2} mbar until the stamping process.

As reported in [123], Co provides a lower yield than Fe based catalyst and the growth rate increases with increasing temperature [68]. According to [58], the use of an Al_2O_3 support material (as present in the standard catalyst) increases the yield of CNTs drastically because of its large surface area and pore volume.

5.8. Graphite and edge contacts to hexagonal boron nitride covered carbon nanotubes and niobium diselenide

The encapsulation of 2D vdW materials with hBN to prevent oxidation also has one significant drawback: using standard EBL and metalization techniques, direct electrical contacts cannot be manufactured to the relevant structures.

First, graphite flakes still protruding from the hBN were stamped on NbSe₂ and CNTs before being covered with hBN. Metallic contacts are then deposited onto the protruding graphite flakes using EBL and thermal evaporation (1 nm Cr, 100 nm Au). One receives reliable contacts to NbSe₂ and CNT [154] when compared to direct metal contacts. However, with each additional graphite flake required to be applied by dry stamping, the chance of already stamped structures being unintentionally demolished also increases. Likewise, slipping of individual flakes can unintentionally short-circuit certain sections. Consequently, the sample geometry is strongly dependent on the shapes of the available flakes and the accuracy of the stamping process.

Since 1D edge contacts to fully encapsulated 2D vdW materials such as graphene or MoS_2 highly increase the sample properties [162, 252], we applied this technique also to $NbSe_2$. In 2018, when we first tried this, to the best of our knowledge, nothing has been reported about this in the literature. Further inspired by [184, 210], we successfully implemented this concept for contacting encapsulated 1D CNTs with zerodimensional (0D) edge contacts. The basic idea of this contacting method is illustrated in figure 5.7 and works as follows. The 2D flake or the 1D CNT is encapsulated from above

5.8. Graphite and edge contacts

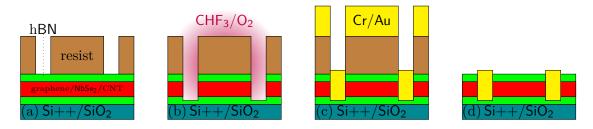


Figure 5.7.: Schematic representation of the edge contact fabrication. (a) With this method, graphene (graphite), NbSe₂ and CNTs can be contacted equally in one process. The materials to be contacted are encapsulated (at least from above) with hBN on a $Si++/SiO_2$ chip. By means of EBL, a PMMA layer is patterned as etch mask for the contacts. (b) In a RIE process, the materials to be contacted are etched through. (c) Immediately after etching, the resulting trenches are filled with metal (1 nm Cr/100 nm Au). (d) Finished device after lift-off.

(and possibly also from below) by hBN flakes. In a PMMA layer, EBL is used to define a mask for an anisotropic RIE process. Here hBN serves as a protection layer. Directly afterwards, contact metal (1 nm Cr/100 nm Au) is then deposited into the etched trenches. The fabrication process is identical for 1D and 2D materials and can be performed at the same time on the same chip. The previously required graphite contacts are consequently no longer necessary. We can thus reduce number of required stamping steps and minimize contamination at interfaces. The contacts can be designed one order of magnitude more precisely. The main advantages are higher yield and quality, especially for the NbSe₂ contacts. Although NbSe₂ easily photo oxidizes under ambient conditions, we were able to achieve a relatively low contact resistance of $1 \frac{\text{mS}}{\text{µm}}$ for the edge contacts in the vast majority of cases. In the case of CNTs, more than half of the fabricated edge contacts work and the contact resistance is in the order of few k Ω to M Ω [248, 274].

In reference [162], 1D contacts to a 2D material in contrast to conventional surface contacts were reported for the first time. By this, one achieves a separation of layer arrangement and metalization of contacts. Theory calculations showed that edge contacts exhibit a smaller bonding distance with larger orbital overlap in contrast to surface contacts and lead thus to a lower contact resistance [162]. In contrast to [262], we do not need an additional Ar ion cleaning before metal deposition. In reference [195], also Al_2O_3 was reported as protection layer. As stated in [184], hBN-encapsulated CNTs can carry larger current densities due to the high thermal conductivity of hBN and a low thermal conductivity between CNT and hBN. 1D contacts to a semiconducting MoS_2 were among others reported in references [226, 245, 252, 264].

It is important for us to know the thickness of the upper hBN layer and possibly the thicknesses of the NbSe₂ and graphite flakes by means of AFM or optical contrast before fabricating the contacts. This is because the etching time is based on this. Our standard etching parameters are CHF_3/O_2 as process gases with flow rates of 40 sccm/6 sccm at a pressure of 35 mTorr and a power of 35 W. A similar recipe was reported in [210]. In

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a previous Regensburg work [247], an etch rate of $\sim 0.8 \frac{\text{nm}}{\text{s}}$ in hBN was determined for these values. We quickly got the impression that this recipe etches significantly less deeply. Thus we investigated the etching rates in our RIE system for NbSe₂, hBN and graphite as part of Maximilian Ufer's bachelor thesis [263].

The desired flakes were exfoliated and stamped onto a Si $++/SiO_2$ chip under ambient conditions. An EBL patterned PMMA layer serves as an etching mask. The thickness of the flakes before and after the RIE process are determined via AFM. We keep all RIE parameters as indicated above constant and vary only the etching time t_{etch} between 3 s and 60 s. Figure 5.8 depicts the etching depth of these materials as a function of the etching time. By extracting the slope of the linear fits to our measurement data,

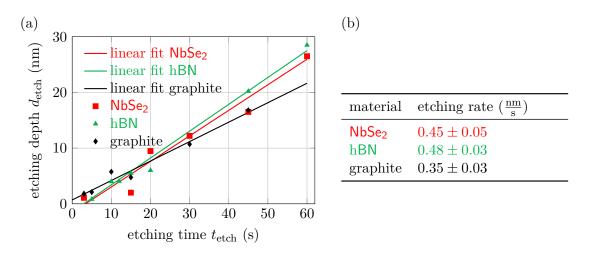


Figure 5.8.: (a) Etching depth of NbSe₂ (red squares), hBN (green triangles) and graphite (black diamonds) as a function of etching time in our RIE system. All other RIE parameters were instead kept constant. As process gases we used CHF₃/O₂ with a flow rate of 40 sccm/6 sccm, a chamber pressure of 35 mTorr and a power of 35 W. We estimate the etching rates by extracting the slope of the linear fits (straight lines) of our measurement data. (b) Experimentally determined etching depths. The fabrication and measurements necessary for this data were performed under my guidance by Maximilian Ufer [263]. The etching rate of SiO₂ was determined later as ~ 0.1 $\frac{\text{nm}}{\text{s}}$.

we determine the etch rates of NbSe₂ to $(0.45 \pm 0.05)\frac{nm}{s}$, of hBN to $(0.48 \pm 0.03)\frac{nm}{s}$ and of graphite to $(0.35 \pm 0.03)\frac{nm}{s}$. We see that the etching rates of these materials are indeed comparable. At a later time point, the etch rate in SiO₂ was determined as $(0.10 \pm 0.03)\frac{nm}{s}$.

We have now assembled all the important craft skills required to fabricate (CNT-) TMDC (hybrid-) devices. Concrete sample geometries and measurement results will now be highlighted in the following two chapters 6 and 7.

This chapter 6 describes the fabrication and measurement results of CNT-NbSe₂ hybrid devices. The overall goal of this thesis is to fabricate and measure a device for the detection of MFs in a CNT, proximitized by superconducting NbSe₂. We follow the idea of Marganska et al. [238], as presented in section 2.4. Already the single partial steps on this way give interesting results, which are now explained in more detail.

In section 6.1, the main milestones towards such a device are presented. Thereafter, a specific sample is used as an example to highlight the results of the early generations of such devices in section 6.2. In these samples, the relevant components were still provided with graphite contacts and the stability diagrams showed a charging pattern typical for a chain of QDs and no clear signatures related to superconductivity. Section 6.3 discusses the results of a sample whose contact resistance was very low. In a bundle of only a few CNTs, a supercurrent could be detected as well as signs of both PSCs and PSLs. The individual transport features have characteristic behavior with respect to temperature and magnetic field.

6.1. Brief overview of the development of specimen fabrication

Initially, it was not trivially clear whether electrical contact between a CNT and a NbSe₂ flake could be realized at all. Therefore, this project began by dry-stamping two graphite flakes onto a CNT grown with the catalyst solution in ambient conditions. This is obvious since graphite, unlike NbSe₂, does not oxidize and is made of the same basic building material as a CNT, namely graphene. The graphite flakes were then provided with metal contacts. The results can be found in appendix D.2. The length of the CNT portion between the graphite flakes was about 10 µm (sample 055). The contact resistance at room temperature was $250 \text{ k}\Omega$ and the conductance of the sample showed a dependence on the gate voltage. At about 100 K, the graphite contacts repeatedly froze out [213].

After this first, encouraging proof of principle, it was clear that for the projects going forward, the type of CNT growth based on the catalyst solution was not target-oriented. Long, well-separated and as straight as possible CNTs could be obtained by using thin Co films as catalyst, as described in section 5.7, after optimization of film thickness and growth temperature. In appendix D.3, sample 052 represents the first device for which both multiple graphites and, for the first time, a NbSe₂ flake were deposited onto a CNT grown from thin Co films using dry-stamping under ambient conditions. The working contacts showed a $5.5 \text{ M}\Omega$ high contact resistance of NbSe₂ over an approximately 25 µm

long CNT portion to a graphite flake as well as a gate voltage dependence. This sample could not be examined immediately after fabrication at low temperatures and showed no electrical conduction after five weeks of storage in a dark vacuum box [213].

Sample 103 (see appendix D.4) was the first MF detection device that could be studied at low temperatures. The length of the CNT portion between NbSe₂ and graphite flake could be reduced to about 2 µm by refining the stamping process. The contact resistance of ~ 50 k Ω at room temperature deteriorated by three orders of magnitude by cooling to 2.2 K. The stability diagram showed a Coulomb charging pattern typical of chains of QDs. No evidence of superconductivity could be detected. The NbSe₂ flake probably partially oxidized during the dry-stamping process [227].

6.2. Early Majorana fermion detection device (sample 128)

Sample 128 belongs to the next generation of MF detection devices. Its schematic fabrication process is visualized in figure 6.1 and an optical image is shown in figure 6.2(a). A NbSe₂ flake is applied to a CNT grown from thin Co films by dry stamping. The

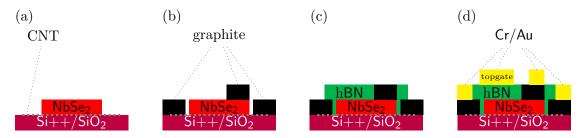


Figure 6.1.: Schematic fabrication process of early 1D-2D hybrid structures. (a) A few layered NbSe₂ flake is stamped on a CNT grown on a $Si++/SiO_2$ substrate by dry stamping. (b) Using the same technique, graphite flakes are then applied to both ends of the CNT and to the NbSe₂. (c) Subsequently, the NbSe₂ flake and the area of the CNT between its two graphite contacts are covered with a hBN flake, thus protecting it from oxidation and degradation to the greatest extent possible. (d) In the final step, EBL and thermal evaporation are used to fabricate the three contacts and optionally a top gate.

layout of sample 128 had slightly changed from the previous generation (sample 103, see appendix D.4) in that, in accordance with the suggestion in reference [238], only a 4 µm wide NbSe₂ flake was used. Additionally, two graphite contacts were placed on both the left and right ends of the CNT adjacent to the NbSe₂ flake. The relevant part of the device is protected against oxidation by a thin hBN flake from above. The exfoliation as well as the dry stamping process were carried out by Brecht Simon [242]. The precision in the orientation of the flakes during stamping was performed very accurately with a precision of 1 to 2 µm, in contrast to previous samples. Also new at this time was that heating the sample in forming gas atmosphere for 10 min at 150 °C minimized the risk of flakes being thrown off during spinning of the PMMA resist. Moreover, the stress of the 2D vdW flakes relaxes due to the heat treatment. The metal leads (1 nm Cr/100 nm Au) for the graphite flakes and the topgate finger above CNT and NbSe₂ are created in a subsequent nanofabrication step. Note that the lower CNT graphite contact 1 did not work. From this sample on, the EBL step not only used the interferometric laser stage to design the contacts. Instead, their sub-µm alignment precision is ensured by using the so-called *windows of alignment*. A bilayer NbSe₂ crystal, which is so thin that its electron density and chemical potential can be tuned by the topgate, was chosen. Such tunability is crucial to enter the topological phase of the proximitized CNT.

The first transport characterization is presented in figure 6.2(b) to (d). Panel 6.2(b)shows the conductance G_{23} between the contacts 2 and 3 (graphite-NbSe₂-CNT-graphite) as a function of Si++ backgate voltage at room temperature (red) and 4.2 K (blue). The value of the conductance decreases only by a factor of 3 after reaching liquid He temperatures. The conductance is more pronounced on the hole side and shows a distinct backgate voltage dependence as well as a gap not symmetric with respect to $V_{\rm G} = 0$ V. The stability diagram in panel 6.2(c) depicts the differential conductance as a function of both bias voltage $V_{\rm SD}$ and backgate voltage $V_{\rm G}$ at $T = 2.2 \,\rm K$ in absence of magnetic field. The range of the gate voltage was chosen so that well-defined current flow is measurable for moderate bias voltage. As in sample 103 (see appendix D.4), no single diamonds but a very complex structure is observed as in the case of a QD chain [38, 95. 114]. Its origin can be related to disorder introduced by the SiO_2 substrate. Water or nanofabrication residues may be also responsible for this [259]. Panel 6.2(d) shows the DC current between the same contacts for a wider range of bias voltage at $V_{\rm G} = -4.9755 \, {\rm V}$ at $T = 2.2 \,\mathrm{K}$ in absence of magnetic field. By performing a linear fit for $|V_{\mathrm{Bias}}| > 5 \,\mathrm{mV}$, we extract a CNT-NbSe₂ contact resistance of $180 \,\mathrm{k\Omega}$. We attribute this reduction of resistance by two orders of magnitude to the refined sample fabrication techniques. As we will see in the next section 6.3, this value can be even decreased further by making use of edge contacts to both CNT, NbSe₂ and graphite.

Stability diagrams are displayed in figure 6.3 for different temperatures and perpendicular magnetic fields (perpendicular to the $NbSe_2$ plane). The diagrams in the the upper/lower row were recorded at $4.2 \,\mathrm{K}/300 \,\mathrm{mK}$. In the left/right column the magnetic field was 0 T/5 T. The value of 5 T was chosen to be safely larger than the critical perpendicular field of NbSe₂, which in the few layer regime is about 2 to 3 T [224]. The ranges for gate and bias voltage as well as the linear colorbar in panel 6.3(b), which encodes the value of the differential conductance, is the same for all four stability diagrams. In the considered range of gate voltage, the familiar Coulomb charging pattern is seen in panel 6.3(a) at $4.2 \,\mathrm{K}$. This appearance changes only insignificantly when a perpendicular magnetic field of 5 T is applied, see panel 6.3(b). A marked difference is seen when the sample is cooled to $300 \,\mathrm{mK}$ in the absence of a magnetic field, see panel 6.3(c). Here one sees a conduction gap whose energy roughly matches the superconducting gap $\Delta_{\mathsf{NbSe}_2} \approx 1 \,\mathrm{meV}$ of NbSe_2 [224]. The latter is indicated by the horizontal black dashed lines. However, this gap does not close at low temperatures again when the magnetic field is applied, see panel 6.3(d). So one cannot speak of clear signs of superconducting proximity effect. The occurrence of the gap at low temperatures is probably due to defects. The stack of different materials can cause complex behavior. In addition, the

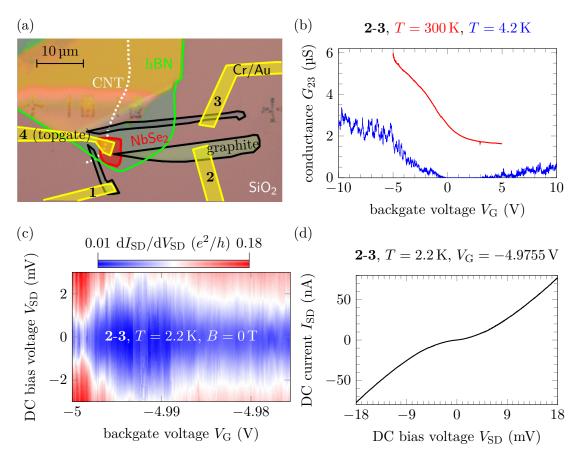


Figure 6.2.: Sample 128 (second Majorana fermion detection device at low temperatures, with topgate). (a) The optical image shows a NbSe₂ flake (outlined in red) stamped on a CNT (highlighted with dotted white line). The two ends of the CNT and NbSe₂ are contacted with graphite flakes. The metal contacts (1 nm Cr/100 nm Au) and the top gate are only indicated here with a yellow outline and numbered from 1 to 4. Contact 1 did not work. The relevant part of the sample is covered with hBN (outlined in green). (b) The conductance is higher on the hole side and only drops by a factor of three during cooling. (c) The stability diagram at the hole side shows a complicated diamond structure typical for a series of several QDs. (d) *IV* charactersitic at T = 2.2 K and $V_{\rm G} = -4.9755 \text{ V}$. By a fit in the linear domain ($|V_{\rm SD}| > 5 \text{ mV}$), the resistance of the system can be determined to $\sim 180 \text{ k}\Omega$.

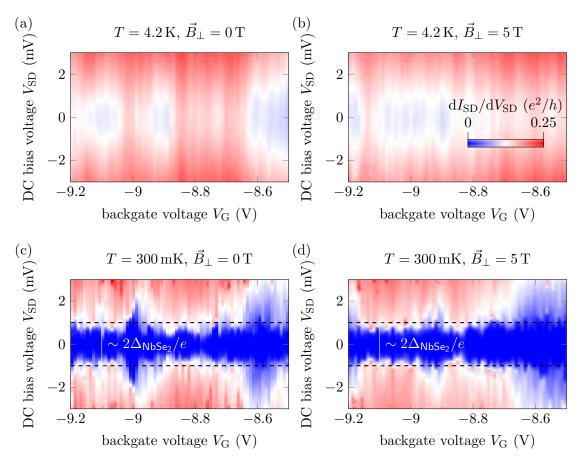


Figure 6.3.: Magnetic field and temperature dependence of the differential conductance of sample 128. The ranges of $V_{\rm G}$ and $V_{\rm SD}$, as well as the linear color scale for the differential conductance in subfigure (b), are the same for all four stability diagrams. Contacts 2 and 3 were used for source and drain. (a) At 4.2 K, one observes a washed-out charging pattern characteristic of coupled QDs. (b) Applying a magnetic field at the same temperature has only a very moderate effect on the overall appreance. (c) At 300 mK, a conduction gap of the width of about the superconducting gap of NbSe₂ (~ 1 meV [238]) can be seen. (d) This gap does not close when applying a perpendicular magnetic field.

length of the CNT over which the transport behavior is measured, is still relatively long at about 4 µm and a decay into a series of multiple uncorrelated QDs is likely.

As mentioned earlier, the ability to gate the hybrid system into the topological phase is essential for our long-term project. Hence, we brought our topgate to action and investigated the dielectric breakdown of hBN, see figure 6.4. For this purpose, the sample

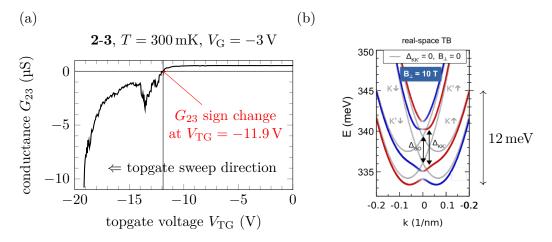


Figure 6.4.: Determination of the hBN breakdown field in sample 128. (a) Determination of the electrical breakdown field of hBN at 300 mK. A bias voltage $V_{\rm SD} = 10 \,\mathrm{mV}$ is applied between contacts 2 and 3. The global gate voltage on the doped Si substrate is set to $V_{\rm G} = -3 \,\mathrm{V}$ such that a (positive) conductance of about 0.5 µS can be detected through the Majorana device. The topgates voltage is swept in negative direction starting from zero. At $V_{\rm TG} = -11.9 \,\mathrm{V}$ a sign change in conductance and hence the hBN breakdown is observed. (b) From the value of the breakdown voltage as well as the estimated hBN thickness, the 2D carrier modulation can be estimated into an energy value of ~ 12 meV. This value is compared with the energy diagram from reference [238]. Figure taken from reference [238].

was first cooled to 300 mK without magnetic field. At a gate voltage of $V_{\rm G} = -3$ V, the bias voltage between contacts 2 and 3 was chosen such that $G_{23} \approx +0.25 \,\mu\text{S}$ (positive) a clear current flow through the device was discernible. Subsequently, the topgate voltage (at contact 4) was slowly moved in the negative direction starting at 0 V until the hBN layer breaks through and this will be visible as a sign change in the conductance G_{23} . Panel 6.4(a) shows the conductance G_{23} as a function of the topgate voltage $V_{\rm TG}$. At $V_{\rm TG} = -11.9$ V, the hBN flake breaks through which is visible as negative leakage conductance. By AFM measurements, the hBN flake thickness was determined as ~ 15 nm. Consequently, the dielectric strength is about 0.8 $\frac{\text{V}}{\text{nm}}$. This value has also been reported in literature [135, 200]. From this value, one may expect a change in carrier density $\Delta n_{2\text{D}} = \frac{\varepsilon_0 \varepsilon_{\text{r}}}{e} E^{\varepsilon_{\text{r}}=4} 1.8 \times 10^{13} \frac{1}{\text{cm}^2}$ according to reference [204]. Hence, the possible change of chemical potential $\Delta \mu \approx 12$ meV should be large enough to tune a MF detection device into the topological phase, see panel 6.4(b).

6.3. Supercurrent and phase slips in a ballistic bundle of carbon nanotubes (sample Majorana 5)

In this section 6.3, we present a CNT-NbSe₂ hybrid device following the approach of [238]. We show that the NbSe₂-CNT contact transparency can be drastically improved by making use of edge contacts to both CNT, NbSe₂ and graphite as described in section 5.8. In contrast to earlier samples (see section 6.2, appendix D.4), we were able to detect a considerable superconducting current through a bundle of few CNTs contacted with few-layer NbSe₂ over a distance of about $2 \,\mu$ m, which is just not below the flake. Since this supercurrent exhibits a large in-plane critical magnetic field, it is very probable that the Cooper pairs inside the CNT are protected by Ising superconductivity [205, 224]. The nucleation of PSCs (resistance steps) mediates the breakdown of superconductivity caused by current in the 1D superconducting system. Results are published in reference [266].

6.3.1. Sample fabrication

Figures 6.5(a) to (d) show the schematic sample fabrication process and panel (e) depicts an optical image of the finished device *Majorana 5*. As an innovation in sample fabrication. a graphite flake (height $\sim 40 \,\mathrm{nm}$) was applied to a substrate for the first time by dry stamping, hoping for better current carrying abilities, avoidance of charge traps on the SiO_2 surface and disorder emerging from contaminants next to the CNT as reported in references [170, 184, 241, 252]. Hence, this configuration enables ballistic transport. The graphite flake can act as a gate, as presented in references [175, 273]. Afterwards, the lower hBN flake (height $\sim 35 \,\mathrm{nm}$) was dry stamp transferred onto the graphite flake and serves as a dielectric for the graphite gate. Together with the upper hBN, it fully encapsulates the relevant sample part and assures the best possible air tightness [251]. Long CNTs were grown on an additional marker substrate using thin Co films as catalyst. It is in general difficult to locate CNTs grown on hBN or on a macroscopic substrate. Optical microscopy cannot do it at all because of its resolution and AFM takes a lot of time. The best compromise in terms of time required to obtain sufficiently meaningful images is the SEM technique. The quality of the images depends significantly on the electron detector mode, the acceleration voltage and the aperture used [165, 210]. That is why the CNT in our case was stamp-transferred via the hot pick-up technique on top of the lower hBN flake. The success of the transfer and the absence of impurities were confirmed via AFM measurements, see figure 6.8. Up to this point, all transfers were performed under ambient conditions. In contrast to reference [162], our CNT could not be picked-up with NbSe₂ or hBN. Therefore, as a finish, NbSe₂ (thickness $\leq 3 \text{ nm}$) and the upper hBN (thickness $\sim 5 \,\mathrm{nA}$) were applied using the hot pick-up technique in N₂ atmosphere. The sample was annealed for 2 h at a temperature of 150 °C and a pressure of 10 mbar in forming gas atmosphere after all transfer processes had been performed.

Subsequently, edge contacts (1 nm Cr, 100 nm Au) were added to both ends of CNT, as well as to NbSe₂ and graphite in one step using EBL, RIE (CHF_3/O_2) and thermal evaporation as described in section 5.8. The main part of the sample preparation was

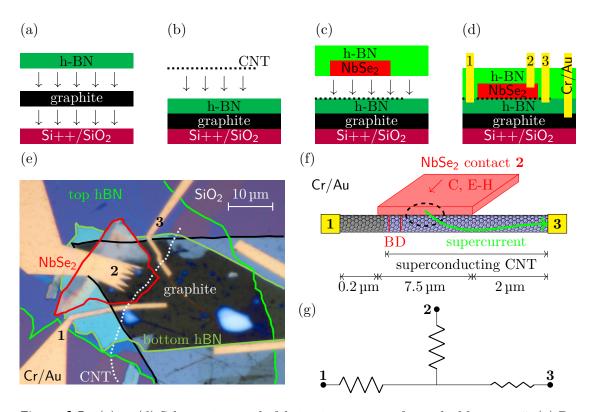


Figure 6.5.: (a) to (d) Schematic sample fabrication process of sample *Majorana* 5. (a) By dry-stamping, a graphite layer (black) and the lower hBN (dark green) are deposited successively on a $Si++/SiO_2$ substrate. (b) The application of CNT (dotted black line) to the lower hBN by hot pick-up method. The success of the transfer is evaluated with a AFM measurement. (c) The hot pick-up method is then used to add another few-layer NbSe₂ flake (red), previously picked up with the top hBN (green), to the existing stack. (d) In one step, both CNT, NbSe₂ and graphite flakes are equipped with edge contacts (1 nm Cr/100 nm Au). For this purpose, EBL, RIE and thermal evaporation are used. (e) Optical image of the finished device. (f) Schematic side view. The device has two 0D Cr/Au edge contacts to the CNT (designated as contact 1 and 3). Contact 2 is formed by NbSe₂ flake (red). The corresponding lenghts of the three CNT portions are indicated. The normal/superconducting CNT portions (left, right) are highlighted in gray/light blue. In a certain segment, the contact transparency between $NbSe_2$ and CNT is lower (dashed black ellipse) and analogously corresponds to the point contact experiment in reference [255]. B and D represent the resistance peaks associated with PSCs. They are to be found somewhere between contact 1 and 2. For the observation of the resistance peaks C and E-H associated with PSLs, contact 2 must be involved in transport measurements. (g) Electrical scheme of the measured device. The resistance associated with contact 3 is much lower than that of the other two contacts and is in good approximation negligible.

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performed by Lorenz Bauriedl as part of his master's thesis [267]. In contrast to our recipe, the authors in reference [162] used SF_6 gas to etch through the vdW hetero structure. The main advantages of this procedure are that the actual device remains resist-free, is fully encapsulated and is screened of SiO₂ charge traps.

As one can see from figures 6.5(e,f), our device has three terminals. Contact 1 and 3 are the two Cr/Au edge contacts to the CNT. Contact 2 is formed by the NbSe₂ flake. The length of the CNT covered with NbSe₂ is 7.5 µm. Between contacts 1 and 2 and 2 and 3, the lengths of CNT not covered with NbSe₂ and extending to the edge contacts are $0.2 \,\mu\text{m}$ and $2 \,\mu\text{m}$, respectively.

Then, at the probe station, the pairwise contact resistances were determined as explained in section 3.3.1. By applying a bias voltage of $V_{\rm SD} = 3 \,\mathrm{mV}$, the room temperature contact resistances $R_{12}^{\rm RT} = 3 \,\mathrm{k\Omega}$, $R_{13}^{\rm RT} = 6 \,\mathrm{k\Omega}$ and $R_{23}^{\rm RT} = 7 \,\mathrm{k\Omega}$ were determined. None of the contact configurations exhibited pronounced gate voltage dependence. No leakage current was observed between the three contacts to either Si++ or the graphite gate. This further implies that our determination of etch rates from section 5.8 was sufficiently accurate to avoid etching too deeply and thus contacting the graphite flake with Au.

6.3.2. Stability transport characterization

The low temperature transport measurements were performed in a dilution refrigerator with filtered DC transport lines and a base temperature of 30 mK, see section 3.2.3. For different temperatures, magnetic fields, and gate voltages, the differential conductance $G = dI_{SD}/dV_{SD}$ is measured between all three possible pairs of contacts (1-2, 1-3, 2-3) as described in section 3.3.2.

Figure 6.6 displays stability diagrams for contacts 1-3 (a), 1-2 (b) and 2-3 (c), respectively at a temperature of 30 mK and in abscence of magnetic field. As already

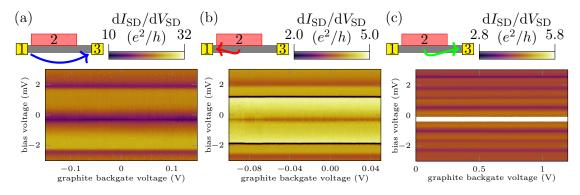


Figure 6.6.: The stability diagrams for all three contact configurations at T = 30 mK and B = 0 T show no dependence on the gate voltage V_{GG} applied to the graphite flake. No Coulomb charging pattern is observed compared to previous samples but instead various minima in the differential conductance as a function of bias voltage are visible. For panel (c) the color range is chosen such that one can see the side peaks.

anticipated in the introduction to this chapter, unlike previous generations, no obvious

sign of Coulomb blockade or disorder for any contact pair is evident in this sample. Instead, several minima in the differential conductance are observed for all contact configurations when the bias voltage is swept. One possible explanation for the independence of the conductance on the gate voltage might be that the CNT is *squeezed* inside the vdW stack and hence is *doped*.

To get a better understanding of the origin of these features, figure 6.7 now plots the differential resistance $R_{ij} = dV_{SD}/I_{SD}$ (between contacts *i* and *j*) in panel (a) as a function of voltage bias and in (b) as a function of current bias. The differential resistance for contacts 1-2 is coded in red, 1-3 in blue and 2-3 in green. These measurements were

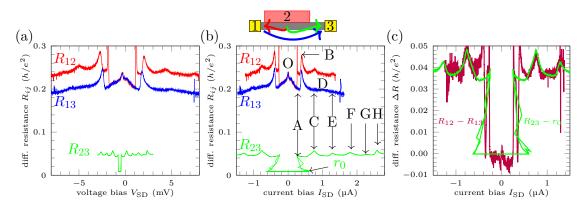


Figure 6.7.: Two-terminal differential resistance R_{ij} between contacts 1-2 (R_{12} , red), 1-3 (R_{13} , blue) and 2-3 (R_{23} , green) plotted as a function of (a) voltage bias and (b) current bias at a graphite gate voltage of $V_{\mathbf{GG}} = 0$ V, T = 30 mK, and B = 0 T. Characteristic peaks in the differential resistance are labeled with letters from A to H and with O. The distinct features of the different traces are only aligned on top of each other when plotted as a function of current bias. (c) According to this plot $R_{12} - R_{13} = R_{23} - r_0$ holds, where r_0 is the residual resistance of R_{23} at low bias ($I_{\mathrm{SD}} < 600$ nA).

also performed at 30 mK and without applying neither a magnetic field nor any gate voltage.

All measurement curves have in common that they show plateaus in the resistance, which are parted from each other by peaks. The various features of the different traces, labeled with A-H and O, are aligned on top of each other only when plotted as a function of current bias. This clearly indicates that the resistive features are triggered by current. As the superconducting gap of bulk NbSe₂ is $\sim 1 \text{ meV}$ [224] and since the features occur at larger energy scales, one may not blame Andreev tunneling or reflection as spectroscopic characteristics varying the resistance for measurements between contacts 1-2 and 1-3.

Let us now take a closer look at the resistance maxima of the different traces in panel 6.7(b). By accurately contrasting the three resistivity measurements, the contributions coming from different areas of the sample can be determined. In the resistance measurement between contacts 1-3 (blue, through the CNT), the two maxima labeled B and D can be seen. We will identify these as PSCs within the CNT (somewhere between

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contact 1 and 2) throughout this section. If we then look at contacts 1-2 (red, left end of CNT to NbSe₂), peaks B and D are present, as well as additional peaks C, E-H. These new features, which we will attribute to PSLs emerging in NbSe₂, are then also present between contacts 2-3 (green, NbSe₂ to right CNT portion) but not features B and D. This is schematically indicated in figure 6.5(f). Note that the minimum current needed to trigger these PSLs is about 780 nA and is hence much smaller as the currents reported in reference [255] ($\geq 10 \,\mu$ A). The contact area between CNT and NbSe₂ is thus probably narrow, as indicated with the dashed black ellipse in figure 6.5(f). The resistance maximum at zero bias, denoted by O, which is visible between contacts 1-2 and 1-3, will be discussed in section 6.3.3. The resistance curves, we measured, are very similar to those of JJs based on short CNTs. They are associated with PS events [49, 70, 78]. A series of several maxima in the differential conductance, appearing very similar to our findings, were reported in a NbSe₂-graphene junction [270]. As long as the bias is sufficiently high, the resistance between contacts 1-2 and 1-3 is about $0.2 h/e^2$, which is only slightly below the $0.25 h/e^2$ resistance minimum of a perfectly conducting single SWCNT. Between contacts 2-3, however, the resistance is significantly lower with a value of $0.05 h/e^2$ and thus deviates downward by a factor 5. One can interpret this value as contact resistance between the few-mode CNT and multi-mode NbSe₂ being the only resistive contribution to the otherwise ideal ballistic conducting nanowire. Yet again, the resistance value $r_0 = R_{23}(I_{\rm SD} < 600 \,\mathrm{nA})$ of this contact pair is significantly smaller for currents $I_{\rm SD} < 600 \,\mathrm{nA}$. In this range, a conductance of $\sim 120 \,e^2/h = 30 \cdot 4 \,e^2/h = 225 \,\Omega$ is detected. This superconducting jump will be labeled as feature A.

Figure 6.8(a) shows an AFM scan at the sample periphery after the stamping process was finished. The successfully transferred CNT (white line) is further highlighted with white arrows. Moreover, the lower and upper hBN (bordered with a dark/light green dashed line) as well as the graphite flake (dashed black border) are discernible. The small orange bar in the lower left region of the AFM image indicates the position on the SiO_2 surface where the topography trace in panel 6.8(b) was taken from. There we can estimate a CNT diameter of (1.2 ± 0.5) nm. Although the error bar may be relatively large, the CNT diameter value is typical of our CVD growth (1-2 nm). Moreover, especially because of the conductance being greater than $4e^2/h$ at high bias, it cannot be completely ruled out that a bundle of few CNTs was inadvertently transferred. Nevertheless, it can be ruled out with fairly high certainty that it is a bundle of many CNTs. The conductance value of $\sim 18 e^2/h$ at high bias would require a CNT bundle many nm thick. Otherwise, considering that in a two-terminal measurement, we still have to subtract all lead resistances (~ 80Ω for the cables to the sample, ~ 100Ω for the Au-NbSe₂ contact resistance corresponding to previous experiments), the conductance between contacts 2-3 will be correspondingly even higher. Hence, we attribute this large conductance between contacts 2-3 to a supercurrent within the CNT. The resistance r_0 probably stems entirely from the Cr/Au edge contact and the cryostat cables. The superconductivity in the CNT must probably extend directly to the Au edge contact, since any normally conducting section in the CNT there, however small, would limit the maximum conductance to $4e^2/h$ per single CNT. Note that there is no scattering in the CNT portion between

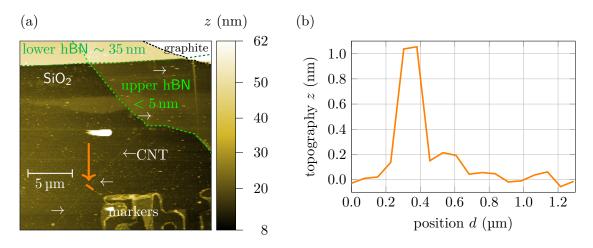


Figure 6.8.: CNT diameter estimation using an AFM topography map. (a) The AFM image of the CNT transferred to the graphite and the lower hBN (highlighted with white arrows) was taken after the final stamping process and before contact electrode fabrication. The lower hBN is at most 5 nm high, and the lower one is about 35 nm. (b) Topography z along the position marked with the orange bar (and additionally highlighted with the orange arrow) in subfigure (a) to estimate the CNT diameter. This measurement is carried out in a place where the CNT is not covered by other vdW materials. The diameter can be determined as (1.2 ± 0.5) nm. From this measurement, we can exclude a thick bundle of several CNTs.

contact 2 and 3.

Figure 6.7(c) displays both the difference $R_{12} - R_{13}$ and $R_{23} - r_0$ as a function of current bias. This means that $R_{12} \approx R_{13} + R_{23}$ holds. As illustrated in the schematic electronic circuit in figure 6.5(g), the resistance associated with contact 3 is thus in good approximation negligible in our three-terminal device. It is further evident that all the characteristics in R_{23} are also present in the difference $R_{12} - R_{13}$.

As already stated, the supercurrent between contacts 2 and 3 is flowing through a $\sim 2 \,\mu\text{m} \log \text{CNT}$ portion which is not in direct contact with NbSe₂. This supercurrent can be extrinsic or intrinsic. The first scenario is probably the most obvious one. NbSe₂ introduces superconducting correlations inside the nearby lying CNT section by proximity effect. The second scenario is less intuitive and was reported for arrays of a huge number or a large bundles of CNTs [49, 70, 147]. However, we can exclude the case of *many* CNTs in our case. In order to distinguish between the two cases of extrinsic and intrinsic superconductivity, we will take a closer look at the dependence of the differential conductance on different magnetic field directions in the following section 6.3.3.

6.3.3. Magnetic field dependence

Figure 6.9 displays the differential conductance G as a function of current bias $I_{\rm SD}$ and perpendicular/parallel magnetic field B_{\perp}/B_{\parallel} in panels (a) to (c)/(d) to (f). All these

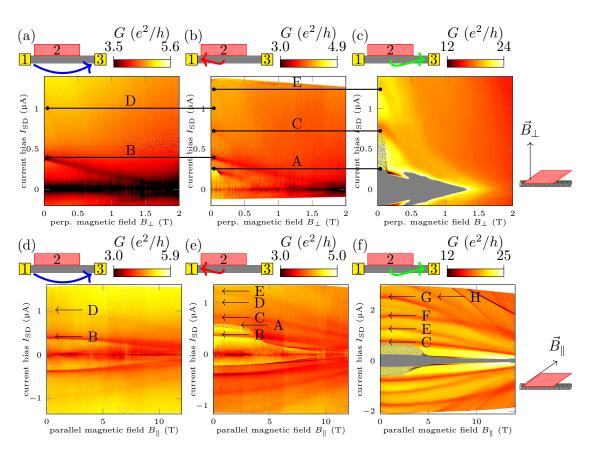


Figure 6.9.: Differential conductance G as a function of current bias $I_{\rm SD}$ and perpendicular/parallel magnetic field B_{\perp}/B_{\parallel} in panels (a) to (c)/(d) to (f) for all pairs of contacts. The field direction relative to CNT and NbSe₂ is indicated on the right of each line. The contact configuration is shown schematically for each plot above the upper left corner. The plots in the lower line were measured in a second cooldown which was necessary to rotate the sample. The measurements were performed at T = 70 mK and for a graphite gate voltage of $V_{\rm GG} = 0$ V.

measurements were performed at a temperature of 70 mK and a graphite gate voltage of $V_{\rm GG} = 0$ V. The measurements in parallel field were performed in an additional cool-down made necessary for sample rotation. As illustrated in the two sketches on the right side of figure 6.9, *perpendicular* indicates a field orientation perpendicular to the NbSe₂ plane (and to the CNT axis), whereas *parallel* means in the NbSe₂ plane (and perpendicular to the CNT axis).

In the previous section 6.3.2, we identified features B and D as PSCs inside the CNT and features C and E to H as PSLs in NbSe₂. PSCs and PSLs show quite a different behavior on a perpendicular magnetic field. The current triggering the latter usually shows only a weak dependence (downward curvature) on the magnetic field and the PSLs features are washed out completely for field below 1 T [110, 111, 255]. The trigger current for PSCs, on the other hand, drops almost linearly with increasing field and PSCs features are visible for field values close to the critical field of NbSe₂. The smearing is due to the entrance of Abrikosov vortices [49, 70]. And this is what we exactly see in perpendicular magnetic field in figures 6.9(a) to (c). Note that the prominent feature B indeed falls linearly with field and crosses the zero current line at around 2 T. This kind of behavior was also reported for JJ based on short CNTs [49, 70, 78]. Feature D is in contrast no longer discernible for fields larger than 0.5 T but also decreases linearly with perpendicular magnetic field.

The behavior in parallel magnetic field is strikingly different, see figures 6.9(d) to (f). The rather high parallel fields up to 14 T do not wash out the PS features but only suppress the trigger current for PSL nucleation only very moderately. The reason for this is that this particular field orientation does not allow vortices to enter the 2D Ising superconductor NbSe₂. Please note further that the magnetic field is always oriented perpendicular to the CNT axis for both field directions. The fact that the field orientation has a significant effect on the appearance of the conductance color map thus argues that the superconductivity, we observe within the CNT, is extrinsic, i. e., induced by the proximity effect.

When measuring the conductance between terminal 1-2 and 1-3, a relatively broad zero bias resistance peak O is observed. We attribute the emergence of this feature to a potential barrier of finite width and height somewhere close to contact 1. Such a zero-bias anomaly has been observed also in short CNT-JJs [70]. Since it endures up to magnetic field values much larger than the critical field value, it is not related to superconductivity.

6.3.4. Temperature dependence

Figure 6.10 presents the temperature and current bias dependence of the differential conductance $G_{ij}(I)$ of the three contact configurations. These measurements were taken in absence of magnetic field and for a graphite gate voltage of $V_{\rm GG} = 0$ V.

Panel 6.10(b) displays a color plot of the differential conductance in dependence of current bias and temperature and panel (a) shows selected traces for the same contact configuration. Their appearance is very similar to that reported in references [49, 70]. The two dashed lines in panel 6.10(b) highlight the evolution of the trigger current $I_{c,A}(T)$ and $I_{c,B}(T)$ of features A and B with temperature. For these two features, one

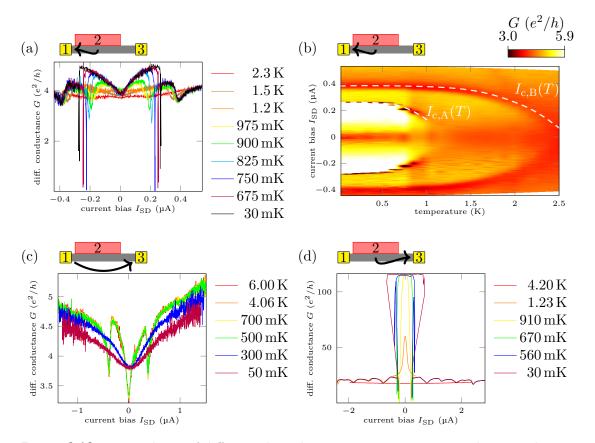


Figure 6.10.: Dependence of differential conductance on temperature and current bias in absence of magnetic field between contacts 1 and 2 (a,b), 1 and 3 (c), and 2 and 3 (d), respectively.

can extrapolate critical temperatures of 1.5 K and 2.6 K, respectively. Feature A can be interpreted as the junction between CNT and NbSe₂. Equation (6.1)

$$I_{\rm c} \simeq \mathcal{T} N \frac{e\Delta^*}{\hbar} \tag{6.1}$$

holds for a junction in a 1D conductor with N channels and four-fold degeneracy and transparency \mathcal{T} . Using $T_{c,B} = 2.6 \text{ K}$, $I_{c,A} = 600 \text{ nA}$ and $\Delta^* = 1.764k_BT_{c,B}$, one receives $\mathcal{T}N = 6.2$. From figure 6.7(c) one can deduce a minimum normal conductance $G_{23}(I > 600 \text{ nA}) = 1/0.043 h/e^2 = 5.8 \cdot 4 e^2/h$, corresponding to a value of $\mathcal{T}N = 5.8$. Hence, the measured critical current $I_{c,A}$ matches that one expected for a junction in a 1D conductor in rather good approximation.

Panel 6.10(c) shows the dependence of the differential conductance on current bias measured between contacts 1-3 for selected temperatures. The minima in the differential conductance seem to be independent of current up to at least 700 mK and they disappear at latest 4.06 K. Since the temperature range between 800 mK and 4.2 K is difficult to access in a dilution refrigerator, only these few measurement data are available for this contact configuration.

Figure 6.10(d) demonstrates that the high differential conductance of ~ 120 e^2/h for $I_{\rm SD} < 600 \,\mathrm{nA}$ has a pronounced temperature dependence. The maximum conductance is maintained up to a temperature of 910 mK, even if the width of this maximum becomes smaller and at 560 mK two side maxima become visible. In contrast, the minima for $I_{\rm SD} > 600 \,\mathrm{nA}$ are independent for temperatures up to more than 1 K. At 4.2 K, these dips also disappear completely.

To conclude this section, we have demonstrated evidence for a macroscopic lateral proximitization in ballistic CNT-NbSe₂ vdW heterostructure. In this scheme, we observed a large supercurrent and current-bias-triggered PS features measured in a nominally normal CNT segment $2 \,\mu\text{m}$ away from the NbSe₂ parent superconductor.

In the next chapter 7, we will consider pure $NbSe_2$ samples without CNTs from which 1D channels were formed by a RIE process.

7. Constriction in niobium diselenide

Although the superconductor NbSe₂ is intensively characterized optically and via transport measurements using current methods with few or even only one layer as 2D clean devices, NbSe₂ has mostly been studied only as a single exfoliated flake. The thickness of these devices can be substantially thinner than the mean free path or the GL coherence length ξ [177]. This pure 2D character combined with the presence of large SOC enables Ising superconductivity [205, 224]. Hence, NbSe₂ is the ideal playground to examine the emergence of PS events. Paradiso et al. could show that the nucleation position of PSLs in plain NbSe₂ films is hard to predict and crucially depends on the individual sample layout due to edge effects or other *weak points* inside the crystal [255]. By patterning a constriction in NbSe₂ with a width of ~ 100 nm, one receives a cross section of ~ 1000 nm². Hence, the free energy barrier, which must be overcome to create a normal conducting region inside the superconducting 1D channel, will be sufficiently small [21]. By doing so, we hope to better control the position of the PS and better understand the associated dissipation [203, 255].

In section 7.1, the fabrication steps necessary to produce a constriction in NbSe₂ are explained. The temperature and perpendicular magnetic field dependence of the four-terminal measurements on the constriction of sample *Majorana 20* are then presented in sections 7.2 and 7.3, respectively. The transport properties of upper and lower bank are discussed in section 7.4.

7.1. Sample fabrication procedure for constrictions in niobium diselenide

Figure 7.1 shows the schematic sample fabrication process and an optical image of the finished device *Majorana 20*. Initially, this sample was intended to be processed as a MF detection device, as presented in chapter 6. However, because the CNT, once successfully deposited, was unintentionally removed by subsequent fabrication steps, a constriction was formed in the NbSe₂ flake.

First, a bottom hBN flake (thickness 25 nm) was deposited on a Si++/SiO₂ substrate by dry-stamping. Second, using the hot pick-up method, a NbSe₂ (thickness < 3 nm, bi or trilayer)/upper hBN (thickness ~ 8 nm) vdW stack was transferred onto the lower hBN flake (removing the previously successfully stamped CNT). Four edge contacts were then attached to the fully encapsulated NbSe₂ flake using EBL, RIE and thermal evaporation (1 nmCr/100 nmAu). Their functionality was then successfully tested at the probe station. In a further EBL/RIE step, the constriction (width 250 nm, lenght 4 µm, aspect ratio 1 : 16) is finally shaped. In literature, a coherence length $\xi \simeq 8$ nm

7. Constriction in niobium diselenide

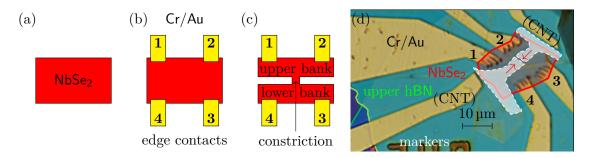


Figure 7.1.: Sample Majorana 20 (first constriction in NbSe₂). (a) to (c) Schematic sample fabrication process from top. (a) First, an as homogeneous as possible 2D NbSe₂ flake fully (half) encapsulated with hBN is transferred onto a Si++/SiO₂ subtrate. Only NbSe₂ is shown. (b) In a second step, four edge contacts are manufactured using EBL, RIE and thermal evaporation (1 nmCr/100 nmAu). (c) After the integrity of the contacts has been verified on the probe station, the constriction is formed in a third step by means of EBL and RIE. (d) The optical image shows a constriction (width 250 nm, lenght 4 µm, aspect ratio 1 : 16) patterend in a few layer NbSe₂ flake. The four edge contacts are numbered from 1 to 4. The NbSe₂ flake is outlined in red. The white area was etched out by the RIE process. The two red arrows point to the constriction. The two contacts labeled *(CNT)* should have contacted the CNT that is no longer present. The room temperature two-terminal contact resistance values can be found in table 7.1.

and a London penetration depth $\lambda = 75 \,\mathrm{nm}$ was reported for NbSe₂ [92] giving rise to an effective penetration depth and hence an Abrikosov vortex size of $\lambda_{\rm eff}^{\rm bi} = 4.5 \,\mu\mathrm{m}$ and $\lambda_{\rm eff}^{\rm tri} = 3 \,\mu\mathrm{m}$. Here $\lambda_{\rm eff} = \lambda^2/d$ holds, with d denoting the crystal thickness. The geometry of the NbSe₂ constriction after the RIE process is sufficiently small to prevent the entrance of Abrikosov vortices. This is due to the fact that we have to deal with the intermediate regime $\xi \ll w \ll \lambda_{\rm eff}$ assuring a uniform current density. Furthermore, PSLs can be observed without interfering with Abrikosov vortices.

Table 7.1 shows the pairwise contact resistances of the finished device at room temperature before and after constriction etching. It can be seen that the resistance values

the sample *Majorana 20* before and after etching the constriction at room temperature. Due to the RIE process, the values deteriorate only very moderately. 1-2 1-3 1-4 2-3 2-4 3-4

Table 7.1.: Comparison of the two-terminal resistances of all possible pairwise contacts of

pins	1-2	1-3	1-4	2-3	2-4	3-4
R (k Ω) before constriction etching	0.64	1.47	1.50	1.21	1.28	0.73
$R~(\mathbf{k}\Omega)$ after constriction etching	0.83	3.85	3.57	3.00	3.00	2.17

are in the range of several 100Ω to a few k Ω and changed only slightly during the RIE treatment.

The nanofabrication was performed by Lorenz Bauriedl within his master's thesis [267].

7.2. Temperature dependence of the differential resistance measured across the constriction

The low temperature transport measurements, the results of which are presented in the following sections, were performed in a 1 K stick (see section 3.2.1). The measurement setup is described in section 3.3.2. Table 7.2 summarizes the names of the four different contact configurations (ccs) used in the cryogenic transport measurements on sample *Majorana 20*. Between ccA and ccB, the difference is that the roles of the contacts

Table 7.2.: Assignment of names for four contact configurations used in the low-temperature measurements. The contact numbers were assigned in figure 7.1(d). "I" labels the contacts between which the current through the device was measured whereas "V" labels the contacts between which the voltage drop was measured.

name	contact 1	contact 2	contact 3	contact 4
ccA	V	I (source)	I (drain)	V
ccB	I (drain)	V	V	I (source)
ccC	I (drain)	I (source)	_	_
ccD	_	_	I (drain)	I (source)

for current and voltage drop measurement across the constriction for a four-terminal measurement are reversed. Since no discernible difference is noticeable between the two, only the results for ccA are presented in the following. The upper/lower part of the NbSe₂ flake are characterized with two-terminal measurements with ccC/ccD.

7.2. Temperature dependence of the differential resistance measured across the constriction

Figure 7.2 shows the temperature and current bias dependence of the differential resistance measured in four-terminal configuration (ccA) in absence of magnetic field. Some characteristic maxima/minima in the differential resistance are denoted by \mathcal{A} through \mathcal{E} . Since all of them appear at a voltage bias which is larger than the NbSe₂ superconducting gap 1.764 $k_{\rm B}T_{\rm c}$, they cannot be spectroscopic features, such as multiple Andreev reflection peaks. We trace their origin to the nucleation of PSLs in NbSe₂ [255, 271, 272]. For temperatures above 4 K, these features are no longer visible.

Label \mathcal{A} denotes the central minimum with finite value around zero current. Its depth and width get smaller while increasing the temperature. The fact that no strictly zero voltage drop is observed for low current bias could be due to inadequate filtering, demolition of the constriction by etching from above or oxidation from the side.

Features \mathcal{B} to \mathcal{E} exhibit a clear concave curvature towards the zero current line for positive current bias. Their temperature dependence resembles strongly that of PSL in NbSe₂ observed by Paradiso et al. [255]. Our observed PSLs do not seem to converge in a single point but they show the typical temperature dependence of the phenomenological BCS gap given by $\Delta(T) \propto \tanh(1.74\sqrt{T_c/T}-1)$ [4]. Features \mathcal{D} and \mathcal{E} have an extrapolated critical temperature of ~ 5 K but for features \mathcal{B} and \mathcal{C} , it is ~ 3.5 K.

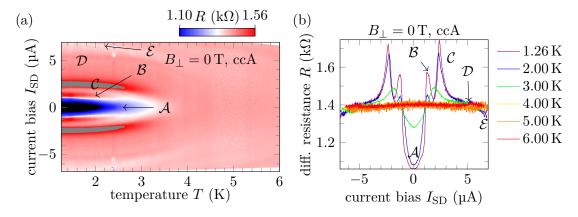


Figure 7.2.: (a) Differential resistance of the constriction plotted as a function of current bias and temperature for ccA. (b) Corresponding line traces for selected temperatures. The prominent minima and maxima in the differential resistance R are named with the curved letters \mathcal{A} through \mathcal{E} .

This could be two different places where the PSLs nucleate. Note that feature \mathcal{E} is a resistance minimum and not a maximum, which is usually the case for PSLs.

7.3. Magnetic field behavior of the differential resistance measured across the constriction

Figure 7.3 displays the dependence of the differential resistance on current bias $I_{\rm SD}$ and perpendicular magnetic field B_{\perp} measured in four-terminal configuration across the constriction (ccA). Similar to figure 7.2, the characteristic features in differential resistance are denoted by \mathcal{A} through \mathcal{E} . An additional feature at (0 µA, 4 T), labeled with \mathcal{F} , is present. The color plot in subfigure 7.3(a) is symmetric with respect to zero current bias. Feature \mathcal{A} labels a minimum in differential resistance with finite value of ~ 1.05 kΩ around zero current bias. Unfortunately, no zero voltage drop is observed in this current region. These would unambiguously indicate the presence of superconductivity. With rising perpendicular magnetic field, the width and depth of this minimum is decreased. Feature \mathcal{C} is a pronounced maximum in differential resistance. Its width stays rather constant and its critical current decreases in good approximation linearly while increasing the field strength. For $B_{\perp} > 3$ T, \mathcal{C} merges into feature \mathcal{F} . The origin of the latter is not completely clear. It could stem from both \mathcal{A} (transforming a dip into a peak) or from \mathcal{C} .

From subfigure 7.3(b), it is clear that increasing the magnetic field to 7.5 T does not further change the trace measured at 4 T. D/\mathcal{E} denote a maximum/minimum in differential resistance, which can hardly be resolved with our measurement setup. The evolution of their critical current cannot be traced up to zero current while increasing the field in the color plot. But one may extrapolate a critical field of ~ 1.6 T (at zero current) for both. Note that the critical currents of all features discussed up to now show

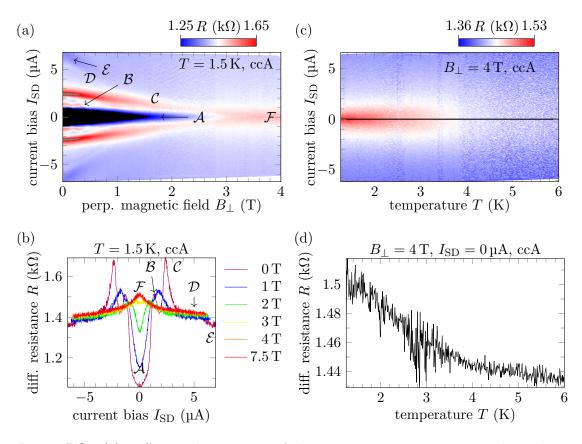


Figure 7.3.: (a) Differential resistance of the constriction *Majorana 20* plotted as a function of current bias and perpendicular magnetic field (perpendicular to the NbSe₂ plane) for ccA. (b) Corresponding line traces for selected field values. (c) Temperature and current bias dependence of ccA at $B_{\perp} = 4$ T. (d) Line cut along the horizontal black line of panel (c). The prominent minima and maxima in the differential resistance are named with the curved letters \mathcal{A} through \mathcal{E} with an additional feature \mathcal{F} . The latter was not present in the temperature dependence shown in figure 7.2.

7. Constriction in niobium diselenide

a linear behavior in perpendicular magnetic field. As reported for plain NbSe₂ films, a perpendicular magnetic field washes out the PS resistance maxima quite rapidly. The behavior, that we observe, resembles more that of PSC nucleation in 1D superconductors, as for proximitized CNTs or intrinsically superconductive CNT bundles [49, 70]. In such systems, the current triggering the peaks is linearly decreased with increasing field. This is also what we observed in the CNT-NbSe₂ hybrid system discussed in chapter 6. Last but not least, feature \mathcal{B} is observed for fields up to about 0.5 T. The origin of its slightly oscillatory behavior is unknown.

Panel 7.3(c) displays the differential resistance measured across the constriction (ccA) as a function of current bias I_{SD} and temperature T at $B_{\perp} = 4 \text{ T}$. Only feature \mathcal{F} is visible. This peak can be decreased slightly in height while increasing the temperature, see also panel 7.3(d). This trace corresponds to the temperature sweep at zero current bias, indicated with the black horizontal line in subfigure 7.3(c).

7.4. Temperature and magnetic field behavior of the banks

Having measured the constriction part in four-terminal configuration, we will now have a look at the upper (ccC) and lower (ccD) bank of $NbSe_2$.

Figure 7.4 shows that the two-terminal DC *IV* characteristics exhibit a perfect ohmic behavior and no dependence either on (a) temperature or (b) perpendicular magnetic field. No features indicative of superconductivity could be detected in the AC measurements

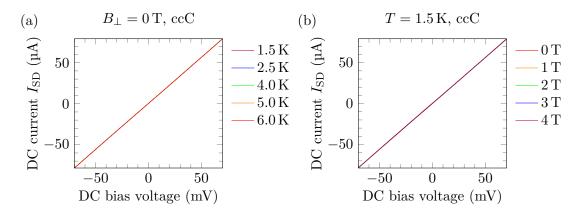
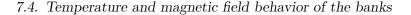


Figure 7.4.: (a) Temperature and (b) magnetic field behavior of ccC (upper bank) of sample *Majorana 20*. The two-terminal DC *IV* characteristics are perfectly linear and show no dependence on temperature or magnetic field, indicating that the upper bank does not show signs of superconductivity. Note that in both plots, the *IV* characteristics of all given temperature and magnetic field values are indeed plotted, but they are all perfectly superimposed.

either. The upper bank is most likely exclusively normal conductive. By performing a linear fit, we can extract the inverse slope of the data giving a resistance of 890Ω which



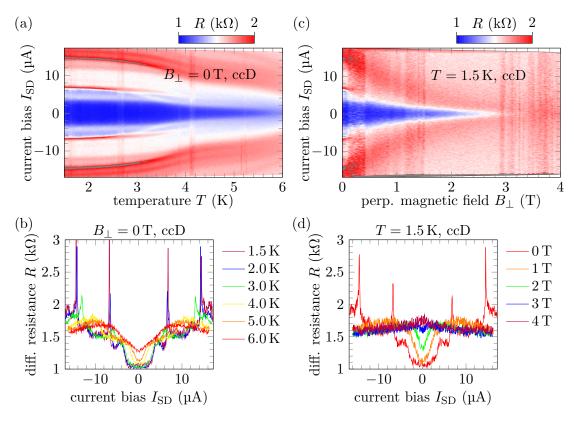


Figure 7.5.: Transport characteristics of ccD (lower bank) of sample Majorana 20. (a) Dependence of the differential resistance on current bias and temperature in absence of magnetic field. (b) Traces for selected temperature values. (c) Dependence of the differential resistance on current bias and perpendicular magnetic field at T = 1.5 K. (d) Traces for selected field values.

is nearly identical to the room temperature value directly after etching the constriction (see table 7.1).

Figure 7.5 shows the electric transport characteristics of ccD (lower NbSe₂ bank). In panel 7.5(a) the differential resistance R is plotted as a function of temperature T and current bias $I_{\rm SD}$. Panel 7.5(b) shows some traces for selected temperature values. The data for both plots were acquired in absence of magnetic field. Note that the current range is about one order of magnitude larger than for ccA (across the constriction) and similar to the findings to reference [255]. We identify the resistance peaks as PSLs in NbSe₂. Their critical currents bend concavely towards the zero current line, typical for a BCS gap. All PSLs seem to converge in a single point at a temperature much higher than the considered temperature range. Interestingly, a kink at ~ 4 K can be observed as well as a splitting of a PSL at (3.2 K, 6 μ A). For temperatures > 4.5 K, even more PSL, that have a nucleation current larger than 18 μ A at 1.5 K, are discernible.

Analogously, the panels 7.5(c,d) represent the magnetic field dependence of the differ-

7. Constriction in niobium diselenide

ential resistance at T = 1.5 K. *Perpendicular* means perpendicular to the NbSe₂ plain. Unlike ccA, the critical current of the very dominant PSL falls linearly up to 1 T, but slightly convexly for higher fields with increasing magnetic field. The value of ~ 3 T can also be considered as the critical magnetic field here. Most of the features are washed out very rapidly up to small fields of 0.5 T, very typical for PSLs [110]. Unlike for ccA, no emergence of a resistance maximum is observed for $I_{SD} = 0 \,\mu A$ fields above 3 T, compare feature \mathcal{F} in subfigure 7.3(a,b).

From our findings, one can try to identify the influence of the constriction. Since we observed a perfect ohmic behavior for ccC, see figure 7.4, one can state that the upper bank can be ruled out as a source of superconductivity and hence for an area of PSL nucleation. Hence, our observed features must stem from the constriction or the lower bank. It is worth noting, that both, the temperature and the magnetic field dependence measured for ccA and ccC, show a similar behavior. Since the exchange of current and voltage drop lines (ccA versus ccB) for the four-terminal measurement across the constriction gives identical results, one may state that the two pairs of voltage drop contacts need to be able to probe a common spatial region. Consequently, this region will probably be located inside the constriction or in the lower bank. Such an argument is not possible for the two-terminal measurement in ccD. Since it is expected that PSLs should wash already at fields up to 0.5 T, it might be possible that the prominent feature in subfigure 7.5(c), which survives up to 3 T, stems from the constriction part due to the nucleation of PSCs (linear field behavior).

Similar results were obtained in another sample constriction 18 [268]. For details see appendix D.8. Based on these findings, Lorenz Bauriedl was able to measure the magneto-ciral anisotropy of $NbSe_2$ in our group.

In conclusion, we have demonstrated that it is not only possible to pattern very long and narrow nanowires in 2D NbSe₂ but also that they still show unambiguously signatures of superconductivity.

8. Summary and outlook

In the first phase of this work, an alternative fabrication technique for quantum dot (QD) devices based on suspended carbon nanotubes (CNTs) has been developed. The method is based on a simultaneous mechanical stamp-transfer of pristine CNTs onto an array of 45 Ti/Pd electrode structures fabricated in advance. This technique is characterized by high reliability (optimized up to $\sim 50\%$ stamp success) and reproducibility. The asstamped CNT-QDs were characterized electrically at room temperature and at 20 mK. A gate dependence at room temperature and Coulomb blockade physics could be observed at low temperatures. The array stamping approach is very versatile and can be extended and customized to more complicated electrode layouts, for example adding several lead or gate fingers, and to the individual needs of the intended experiments. Furthermore, it enables us in principle to use pre-patterned contacts made of ferromagnetic or superconducting metals.

The second major topic focused on CNT-NbSe₂ hybrid systems, compatible with Majorana fermion (MF) detection [238]. It was essential for our project to first establish the CNT growth from thin Co films. Using our standard chemical vapor deposition (CVD) growth recipe for CNTs, a film thickness of 1 nm and a growth temperature of 950 °C turned out to give optimal results. This allowed us to observe the growth of relatively long ($\gg 10 \,\mu$ m) and straight CNTs grown mostly in the gas flow direction. The yield of CNT per catalyst point is roughly estimated to be < 1/100. Consequently, the individual CNTs are arguably separated from each other, which is excellent for stamping two-dimensional (2D) van der Waals (vdW) Materials (NbSe₂, hBN, graphite).

The typical layout consisted of depositing a CNT on a NbSe₂ flake along a length of 2 up to $10 \,\mu\text{m}$. The relevant part of NbSe₂ is protected as best as possible against photo-oxidation with hBN. In order to still be able to electrically contact the relevant parts of the device (NbSe₂ flake, two ends of the CNT), several more graphite flakes were first applied before the top hBN flake was added.

To reduce the number of stamping steps required for this and thus the risk of unintentionally destroying the device, to the best of our knowledge at the time, similar to graphene [162], one-dimensional (1D) edge contacts on NbSe₂ were realized by us for the first time. Also, similar to references [184, 210], zero-dimensional (0D) edge contacts to CNTs were successfully implemented for the first time in Regensburg.

In the early generations of samples, a Coulomb charging pattern typical of a chain of multiple QDs was observed several times at low temperatures. An occurring gap must probably be attributed to disorder and less to superconducting effects, based on the measurements in the perpendicular magnetic field.

By refining the stamping process in N_2 atmosphere, using an underlying graphite layer as well as a complete encapsulation in hBN and developing and implementing the above

8. Summary and outlook

mentioned edge contacts, the contact resistance of CNT to NbSe₂ could be reduced from several 10 M Ω to a few k Ω . Even more strikingly, a completely different sample behavior was observed. We could detect signatures of a large supercurrent through a 2 µm long portion of bundle of few CNTs not in contact with NbSe₂ reaching up to the Au edge contact with a large conductance of ~ 120 e^2/h , beating the normal conductance limit of a single wall carbon nanotube (SWCNT) of $4 e^2/h$. Especially from the comparison of the measurement result in perpendicular and parallel magnetic field, we can argue that the superconductivity inside the CNT bundle is extrinsic and that we see clear signatures of phase slip centers (PSCs) inside the proximitized CNT and phase slip lines (PSLs) stemming from the NbSe₂ flake.

All these results represent important building blocks on the way to the detection of MFs in CNTs. In the framework of the new CRC 1277 funding period, based on these findings, hybrid systems, in which one CNT is contacted with two NbSe₂ flakes, will be investigated.

In the third section, the transport properties of 1D nanowires in hBN encapsulated few-layer NbSe₂ were investigated. For the fabrication, electron beam lithography (EBL) and reactive ion etching (RIE) techniques were used. For this project, as for the previous one, the determination of the exact etch rates of the used vdW materials as well as SiO₂ of our RIE machine was of great importance in order to treat the samples as gently as possible. The two-terminal contact resistances at room temperature were typically in the 100 Ω to low k Ω regime and degraded only slightly during the etching of the constriction. By performing four-terminal measurements across the constriction and two-terminal measurements on the NbSe₂ banks, one can attribute the observed signs of superconductivity and phase slip (PS) events to certain areas of the sample. By comparing the nucleation currents, the temperature and the magnetic field behavior with the results of the above discussed hybrid system, one can also discriminate on the one hand some of the PS events as PSLs stemming from the 2D character of the banks. On the other hand, the critical current of other PS events show a linear dependence in perpendicular field, typical of PSCs in 1D superconductors.

A. General sample fabrication details

This chapter A presents some basic techniques in sample fabrication that have been used in this work.

A.1. General techniques

Scribing, breaking and cleaning of subtrate materials as well as EBL and atomic force microscope (AFM) techniques are presented in this section.

A.1.1. Cutting of wafer chips

We are making use of a scribing machine in order to cut our wafers and substrates into the desired size. Table A.1 gives an overview of the scribing machine parameters. Breaking

lever arm (mm)	scribing lines				
4	2				
4	2				
4	2				
6	3				

Table A.1.: Parameters for the scribing machine.

of the scribed crystals is done in the plexiglass box. After finishing the activity, the entire workplace must be cleaned thoroughly. Gloves must be worn for this process to avoid contamination.

A.1.2. Substrate and wafer chip cleaning

In order to remove protective coats, polymethyl methacrylate (PMMA) or dirt from the surface of a sample chip, the chip is put into acetone for 2 min. In case that there are no delicate parts on top (2D vdW flakes, metal with bad adhesion), the chips can be exposed to an ultra sonic treatment. Afterwards, the samples are put into isopropyl alcohol for 20 s to wash off the acetone. Thereupon, the chip is blown dry with N₂. Optionally, the chips may be treated in an O₂ plasma ashing treatment (1 to 5 min, 50 %, 2×10^1 mbar O₂ pressure) in order to eliminate organic impurities.

A. General sample fabrication details

A.1.3. Electron beam lithography

The various PMMA resists used for EBL are solved in anisole. A few droplets ($\sim 0.1 \text{ mL}$) of this PMMA solution are deposited on a chip using glass pipettes. The spinning parameters listed in table A.2 give typical resist heights of $\sim 350 \text{ nm}$ and $\sim 90 \text{ nm}$ for PMMA 200 k 9% and PMMA 950 k 2%, respectively. In order to remove the solvent,

Table A.2.: Spinning parameters of PMMA 200 k $9\,\%$ anisole and PMMA 950 k $2\,\%$ anisole.

Step	Time (s)	Number of revolutions $(\frac{1}{\min})$	Acceleration
1	5	3000	2000
2	30	6000	4000

the samples are put on a hot plate set to 150 °C. For the fabrication of etch masks or electrode structures, a single resist layer is normally used. For the production of catalyst dots, however, a double layer is used to ensure a clean undercut and thus an optimum lift-off. Typically, an area dose of 300 to $330 \frac{\mu C}{cm^2}$, spacing 10 to 30 nm, $30 \mu \text{m}/120 \mu \text{m}$ aperture for smaller/bigger structures are utilized. After the EBL step, the chips are put into a solution of methyl isobutyl ketone (MIBK) and isopropyl alcohol at a ratio of 1:3 for 20 s/90 s for PMMA 950k 2%/PMMA 200 k 9% or double layers and thereupon into pure isopropyl alcohol for 45 s. Then the chips are blown dry with N₂.

For the lift-off, the metalized sample is stored in a glass closed with a plastic cap located on a heating plate set to $60 \,^{\circ}\text{C}$ for several hours (over night). In order to assure a convenient PMMA removal, the glass is held into an ultra-sonic bath for 20 s. Afterwards clean acetone is injected with a syringe for two times. All the acetone is removed with isopropyl alcohol for 10 s. The sample is finally blown dry with N₂.

EBL enables the fabrication of extremely small structures almost to size of atoms. By scanning an electron beam across a surface coated with PMMA, energy is deposited in the requested patterns in the film. The electron beam is formed and controlled inside the column which typically consists of an electron source, several lenses and deflecting mechanisms. Furthermore, stigmators correct any astigmatism. Apertures inside the beam path are tiny holes which the beam transmits on its way down the column and which thus defines the beam. A blanking aperture turns the electron beam on and off. Focusing and locating marks on the sample are enabled by the electron detector. The entire system is controlled by a computer and isolated against vibration [20, 117].

A.1.4. Atomic force microscope parameters

For the morphological analysis, an AFM was used in tapping mode with a tip diameter of ~ 10 nm. The maximal scanning size was $50 \,\mu\text{m} \times 50 \,\mu\text{m}$ with scanning speed of $1 \,\frac{\mu\text{m}}{\text{s}}$ and a resolution of 128×128 up to 1024×1024 pixels. The integral gain was set to 0.8. For the AFM data analysis the Gwyddion software was used.

A.2. Chemical vapor deposition growth and scanning electron microscope imaging of carbon nanotubes

An AFM allows a mapping of solid surfaces with atomic resolution. This experimental technique is based on measuring the forces between a sharp tip on a cantilever and the sample surface. The reflection of a laser beam is measured by a position-sensitive photodiode. The sample is held in position with the precision of ± 1 pm by piezoelectric actuators. A computer calculates line-by-line of the x - y-position of the scanning probe. The resulting numbers are converted into voltages and afterwards amplified in order to meet the high voltage requirements of the actuators. Elevations on the sample are displayed brighter in false colors. The distance between tip and sample is supervised by a closed-loop feedback system. The tapping mode is a dynamic operation mode where the amplitude of the cantilever is the control parameter. The tip is oscillating in the vicinity of resonance frequency and occasionally has contact with the sample. The oscillation amplitude is detected with a lock-in amplifier [72, 119].

A.2. Chemical vapor deposition growth and scanning electron microscope imaging of carbon nanotubes

For this thesis two kinds of catalysts for CNT growth were used: the standard catalyst solution and nominally 1 nm thick Co films. The details about their application are given in this section.

A.2.1. Standard carbon nanotube growth catalyst solution

- Composition of the standard catalyst solution (inspired by [42])
 - $-40 \operatorname{mg} \operatorname{Fe}(NO_3) \cdot 9H_2O$
 - $-30 \text{ mg Al}_2\text{O}_3$ nanoparticles (diameter 14 nm)
 - $-8 \text{ mg} [CH_3COCH=C(O-)CH_3]_2 MoO_2 (Bis(acetylacetonato)-Dioxomolybdenum)$
 - 30 ml methanol
- Deposition (and lift-off when working with catalyst dot structures)
 - Before catalyst solution deposition: ultrasonic bath treatment for at least $30\,\mathrm{min}$
 - Deposition of 0.1 mL of catalyst solution on a desired chip with a fresh glass pipette
 - Dry blowing with N_2 after 10s waiting time
 - Baking on a hot plate set to $150\,^{\circ}\mathrm{C}$ for $5\,\mathrm{min}$
 - Preparation warm acetone in a closed glass vial placed on a hot plate set to $60\,^{\rm o}{\rm C}$
 - Holding and stirring of the sample in warm acetone for $2\min$
 - Placing the sample in isopropanol for 10s
 - Dry blowing with N_2

A. General sample fabrication details

A.2.2. Thin cobalt films

The fabrication of thin Co films as catalyst structures used for CNT growth works as follows.

- Deposition of nominally $1\,\mathrm{nm}$ thick Co films via thermal evaporation
- Standard lift-off, see subsection A.1.3
- Application of a plasma ashing process only if absolutely necessary to remove all organic residues

A.2.3. Chemical vapor deposition growth process of carbon nanotubes

The steps listed below describe the standard CVD growth process. The specific parameter settings for CNT growth within the *array stamping* are indicated in blue. The process in total takes approximately 2 h.

- Put on gloves
- Put sample onto a glass chip (for clean growth) and position it inside a quartz tube (*CNT growth only III*)
- Position the quartz tube in the stove such, that sample is located close to the temperature sensor (at a quarter of the stoves' length)
- Close quartz tube at both ends
- Open gas bottles (Ar, H_2 , CH_4), the black lower and the green values, open the manual mass flow controllers (MFCs) up to maximum and set the two electronic MFCs to *bypass*
- Flush system for 2 min with all process gases
- Set the two electronic MFCs to mass flow (not for array stamping)
- Adjust gas flow values
 - Ar 1500 sccm (1500 sccm)
 - H₂ 20 sccm (192 sccm)
 - CH₄ 10 sccm (815 sccm, add C₂H₄ 5 sccm for 100 µm long CNTs)
- Close all green gas valves except for Ar
- Close the stove and set the growth temperature between 850 and 1040 °C (1040 °C)
- Open H_2 and CH_4 values, close Ar value
- Readjust gas flow values if needed

A.3. Deposition of various materials

- Grow CNTs for 20 min
- Open Ar valve, close CHF_3 (and H_2) valve
- Switch off furnace and open it, it will cool down automatically
- Close the H₂ valve at 300 °C (not for array stamping)
- Close green Ar valve when temperature is below $180 \,^{\circ}\text{C}$ and remove the sample
- Restore everything
- Fill in lab book

A.2.4. Scanning electron microscope imaging of carbon nanotubes

For scanning electron microscope (SEM) imaging of CNTs (and 2D vdW structures), we set the acceleration voltage to 2 kV and the working distance to 6 mm. We use the 30 µm aperture and use the in-lense mode in order to be more sensitive to surface charges. The image is focused directly on the chip near the position to be examined.

A.3. Deposition of various materials

Table A.3 gives an overview of the parameters used to deposit certain materials [237].

material	system	type	parameters	rate $\left(\frac{\text{\AA}}{\text{s}}\right)$
Со	Univex A	e-Beam	poti 1.6	0.1 to 0.2
Co	Univex A	res. heating	$100\mathrm{A}$	0.1 to 0.2
Cr	Univex A	res. heating	$100\mathrm{A}$	0.1 to 0.2
Au	Univex A	res. heating	150 to $200\mathrm{A}$	1.0 to 5.0
Ti	Univex A	e-beam	poti 1.4	0.5
Ti	small UHV	e-beam	$100 \mathrm{mA}$	0.5
ReMo	small UHV	sputtering	$70\mathrm{W}$	1.2
Nb	small UHV	sputtering	$200\mathrm{W}$	0.5
Pt	small UHV	e-beam	$500\mathrm{mA}$	0.3 to 0.5
Pd	small UHV	e-beam	$280\mathrm{mA}$	0.1
AI_2O_3	ALD	ALD	$80^{\circ}\mathrm{C}$	0.9\AA/cycle
HfO ₂	ALD	ALD	$35^{\circ}\mathrm{C}$	0.8 Å/cycle
SiO ₂	PECVD	PECVD	$650\mathrm{mTorr}$	6.9

Table A.3.: Deposition parameters for various materials. The abbreviations "e-beam"/"res. heating" stand for "electron beam evaporation"/"resistive heating".

A. General sample fabrication details

A.4. Bonder parameters

The old Al-Bonder (power 180, time 100 ms) and the new Au-bonder (300-180 ms-150 mN, 300-200 ms-300 mN, $100 \,^{\circ}\text{C}$) were used to attach small wires between bond pads on the sample and the pins of the standard chip carrier. The bonding order always went from chip carrier to sample.

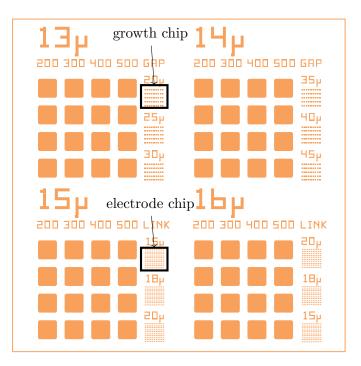
B. Fabrication details for array stamping of carbon nanotubes

In this chapter B, the various fabrication steps for the *array stamping of CNTs* are presented in more detail.

B.1. Details on the growth chip fabrication

The following steps are necessary to produce growth chips.

- Cutting (mass piece on the lever arm of scriber at 6 cm mark) of $8\times8\,\rm{mm}$ SiO_2 chips (thickness 500 $\mu\rm{m},$ double side polished)
- Chip cleaning with acetone for 1 min in ultrasonic bath, 30 s isopropyl alcohol and plasma O_2 (50 %, 1 min)
- Dry blowing with N_2
- Triple spin coating (7000 rpm, acceleration 0, 30 s) of the chips with the optical resist AZ9260 (height ~ 21 µm) and subsequent baking on the heating plate set to 110 °C for 2:45 min (Allow the chip to cool down to room temperature between coating processes for rehydration of the resist)
- Use of the optical mask CNT11P2V2: "GAP 20μ " (schematic sketch see figure B.1)
- Exposure of the entire chip except the plateau structures with ultraviolet (UV) light for 9 min, intensity $1.8 \frac{\text{mW}}{\text{cm}^2}$ (default)
- Removal of the exposed resist using a mixture of developer AZ400K with H_2O (dist.) water in a ratio of 1:3 for 7:30 min with occasional swinging of the beaker
- Termination of the development process by placing the chip in a beaker filled with $H_2O~({\rm dist.})$ for 30 s
- Dry blowing with N_2
- RIE etching of SiO_2 : CHF₃[50 sccm]/O₂[6 sccm] at 55 mTorr and 150 W, etching for 30 min, then pumping for 10 min, total net etching time: 5 h (see table B.1)
- Removal of the remaining optical resist with acetone for $5 \min$ in ultrasonic bath, 30 s isopropyl alcohol and plasma oxygen (50 %, $5 \min$)



B. Fabrication details for array stamping of carbon nanotubes

Figure B.1.: Sketch of the optical mask CNT11P2V2. The relevant structures for fabrication of the growth/electrode chip by optical lithography (OL) are marked with the upper/lower black rectangles. The outer dimensions of the whole optical mask are $10 \text{ cm} \times 10 \text{ cm}$ (outer orange rectangle).

- Dry blowing with N_2
- Renewal of the developing solution after two samples, disposal in canister "E"

B.2. Deposition of catalyst solution on stamp chip and growth of carbon nanotubes

The following list describes all relevant steps for the deposition of standard catalyst solution on top of growth chips.

- Ultrasonication of the catalyst solution (see section A.2.1) for at least 30 min
- Deposition of a few droplets of catalyst solution on a stamp chip with a fresh pipette
- Dry blowing with N_2
- Baking of the stamp chip on a heating plate set to 150 °C for 5 min
- Parameters for the CVD growth of CNTs can be found in section A.2.3

Date	Etching gases	Time (h)	$\mathbf{Depth} (nm)$	Rate $\left(\frac{\mu m}{h}\right)$
03-16-2016	Standard	2	2683.24	1.34
03-21-2016	Standard	5	6084.37	1.22
<u> </u>	CUE [100]/	o [a]		

Table B.1.: Etching rates of SiO_2 for stamp chip fabrication.

B.3. Details on the electrode chip fabrication

The following steps are necessary to produce *electrode chips*.

- Cutting (mass piece on the lever arm of scriber at 4 cm mark) of $4.5 \text{ mm} \times 4.5 \text{ mm}$ Si++/SiO₂ (total thickness 525 µm, single side polished, SiO₂ thickness 500 nm)
- Chip cleaning with acetone for 1 min in ultrasonic bath, $30 \,\mathrm{s}$ isopropyl alcohol and plasma oxygen ($50 \,\%$, 1 min)
- Dry blowing with N_2
- Single spin coating (7000 rpm, acceleration 0, 30 s) of the chips with the optical resist AZ9260 (height $\sim 7 \,\mu$ m) and subsequent baking on the heating plate set to 110 °C for 7 min
- Use of the optical mask CNT11P2V2: "LINK 15μ " (see figure B.1)
- Exposure of the entire chip except the plateau structures with UV light for 8 min with intensity $1.8 \frac{mW}{cm^2}$ (default)
- Removal of the exposed resist using a mixture of developer AZ400K with H_2O (dist.) water in a ratio of 1:3 for 2:30 min with occasional swinging of the beaker
- Termination of the development process by placing the chip in a beaker filled with $H_2O~({\rm dist.})$ for 30 s
- Dry blowing with N_2
- RIE etching of SiO_2 and Si: parameters listed in table B.2
- PECVD of a morphous SiO_2 : parameters listed in table B.3, use of conditioning program before if SiN was used in the previous session
- Removal of the remaining optical resist with acetone for $5 \min$ in ultrasonic bath, 30 s isopropyl alcohol and plasma oxygen (50 %, $5 \min$)
- Optional deposition of $20 \text{ nm } Al_2O_3$ via ALD

Standard: $CHF_3[100 \text{ sccm}]/O_2[6 \text{ sccm}]$

 $^{55\,\}mathrm{mTorr},\,150\,\mathrm{W},\,417\,\mathrm{V}$ (30 min et. + 10 min pump.) $\cdot\,x$

B. Fabrication details for array stamping of carbon nanotubes

Step	Gas[flow]	t	p (mTorr)	$P(\mathbf{W})$
Etching SiO_2	$CHF_{3}[50 \operatorname{sccm}]/O_{2}[10 \operatorname{sccm}]$	$24\mathrm{min}$	55	150
Cleaning	Ar[40 sccm]	$30\mathrm{s}$	40	150
Etching Si	$CHF_3[3\mathrm{sccm}]/SF_6[5\mathrm{sccm}]$	$15\mathrm{min}$	25	40
Cleaning	$Ar[40 \operatorname{sccm}]$	$30\mathrm{s}$	40	150

Table B.2.: RIE parameters for etching of the electrode chip for array stamping of CNTs.

Table B.3.: Parameters for deposition of amorphous SiO_2 via PECVD on electrode chips for array stamping of CNTs.

Step	Gas[flow]	t	$T/^{\circ}\mathrm{C}$	p (mTorr)	$P(\mathbf{W})$
SiO ₂	$\begin{array}{l} SiH_4[170\mathrm{sccm}]/\\ N_2O[710\mathrm{sccm}] \end{array}$	$4 \times 3 \min, 2 \min$ pause	150	650	20

- Dry blowing with N_2
- Spin coating of the sample with PMMA $200k\,9\,\%$ (see table A.2) and subsequent baking on the heating plate set to $150\,^{\circ}\mathrm{C}$ for $8\,\mathrm{min}$
- Removal of the exposed resist using a mixture of MIBK and isopropyl alcohol in a ratio of 1:3 for 90 s
- Termination of the development process by placing the chip in a beaker filled with isopropyl alcohol for 30 s
- Dry blowing with N_2
- Deposition of 20 nm Ti (thermal) and 100 nm Pd (e-gun)
- Remaining of the vaporized samples in acetone for several hours
- Performance of a lift off with a syringe filled with acetone
- Washing off the acetone with isopropyl alcohol for 30 s
- Dry blowing with N_2

B.4. Details on the carbon nanotube stamp transfer and subsequent annealing

B.4.1. Stamp transfer per se

• Clean a glass plate which can be placed like an optical mask in the mask aligner with acetone and isopropyl alcohol

B.4. Details on the carbon nanotube stamp transfer and subsequent annealing

- Blow it dry with N_2
- Put a rather small droplet of PMMA rests with a pipette onto the middle of the plate
- Put your stamp chip (with hopefully CNTs on top) on it (do not press too much)
- Bake out the resist for $5\min$ at $150\,^{\circ}\mathrm{C}$

B.4.2. Annealing in the chemical vapor deposition furnace under argon atmosphere

This step serves the purpose to assure a better contact between CNT and connecting lines by melting the metal a bit. The process is performed inside the CVD stove and can improve the contact resistance by one order of magnitude. The process takes approximately 30 min in total.

- Put on gloves
- Put the sample on a clean growth carrier in the middle of the quartz tube *Nicola cleaning* (It has to be a clean tube)
- Close quartz tube
- Open the Ar bottle inside the cabinet
- Open the lower black valve, set the manual mass flow controller of Ar to 14 and open the green valve of Ar (You do not have to flush the lines with gas first)
- Close the stove and set $400\,^{\circ}\mathrm{C}$
- The heating-up takes about 5 min
- At 400 °C wait for $5 \min$
- Put on he heat protection glove, open the stove and fix the lead with the chain, the stove cools down automatically in less than 20 min
- At 150 °C, you can close the Ar
- Restore everything the other way around
- Take out your sample
- Fill in the lab book

B. Fabrication details for array stamping of carbon nanotubes

B.5. Cleaning of growth and electrode chip for reuse

- Growth chip
 - Prepare a 1.5 molar NaOH lye in a beaker
 - Bathe the growth chips in this lye on a hot plate at 40 °C
 - Put stamp chip into acetone in the ultrasonic bath and leave it there for $10\,\mathrm{min}$
 - Put sample in isopropyl alcohol for $30\,\mathrm{s}$
 - $-\,$ Blow sample dry with N_2
 - Perform an oxygen plasma process (5 min at 50 %) for both sides of the chip before catalyst for a new growth is deposited
- Electrode chip
 - Check if the sample in general and the leads in particular are looking fine under an optical microscope
 - Perform an O_2 plasma treatment (20 s at 30 %) in order to remove all CNTs and other organic residues

C. Details on the exfoliation and stamping of van der Waals materials

In this chapter C, we will give a detailed overview of the various steps needed in the process of exfoliating and stamping of the vdW materials used in this thesis. Gloves should be worn at all steps to protect the crystals, samples, and oneself from contamination.

C.1. Exfoliation and search for flakes

Both hBN and graphite can be processed under ambient conditions. NbSe₂ is always handled in N₂ atmosphere. In the last case, all required items are placed in the glove box and this is flushed afterwards with N₂ gas for half an hour before further activity to minimize the O_2 content.

- Sticking an AI foil on the lab bench to have an antistatic and clean work surface
- Cutting of a rectangular piece of PDMS ($\sim 25 \text{ mm}^2$), removal of the protective foils with the help of two tweezers and application to the edge of a short side of a clean slide avoiding unevenness and bubbles
- Preparation and labeling of several such glass slides
- Cutting of a strip of blue tape about 10 cm long, tape around the ends for about 1 cm, sticking of the blue tape onto an object carrier for easier handling
- Preparation and labeling of several such pieces of blue tape
- Picking of a crystal part from a white tape with a blue tape
- Multiple subsequent thinning of the crystal by using multiple blue tapes
- Placement of the polydimethylsiloxane (PDMS) on a promising site of the opened crystal (only light pressing)
- Pulling off the blue tape as quickly as possible
- Search for suitable crystals under the optical microscope $(20 \times \text{magnification for a quick overview})$
- Taking photos of suitable flakes with 100× (with and without the A-Stop filter), 20× and 4× magnifications

C. Details on the exfoliation and stamping of van der Waals materials

C.2. Stamping of van der Waals flakes

The following steps can be performed inside or outside the glove box. The optical devices, the computer as well as the piezo stage (controlled by a LabView program) are initially switched on.

C.2.1. Dry stamping technique

- Applying a double-sided adhesive tape to the entire surface of the specimen holder of the piezo stage
- Applying one (or two layers) of insulating tape along one side of the specimen holder in order to be able to place the target substrate at a tilt angle
- Apply the substrate in such a way that one corner is on the insulating tape
- (Optional:) Heating of the glass slides with PDMS on the hot plate (temperature $110\,^{\circ}\mathrm{C})$
- Inserting the glass slide into the micromanipulator with the flakes on the PDMS pointing downwards
- Moving down the glass slide until just before contact and align the flake relative to the coordinate system of the chip
- Slow establishment of complete contact between PDMS and substrate (meniscus must have migrated over the entire flake)
- Very slow upward movement of the glass slide, successful stamping process recognizable by change in flake color
- Repeat the stamping process if the flake does not adhere
- Lifting the chip from the double-sided tape with scalpel and tweezers
- Creating photos of suitable flakes with 100× (with and without the A-Stop filter), 20× and 4× magnifications
- Heating chips that have been stamped on to 150 °C for 5 min in forming gas atmosphere (pressure $1\times10^1\,\rm mbar)$

C.2.2. Hot pick-up stamping technique

- Fabrication of a PDMS lens
 - Stirring of a 1:10 volume mixture of PDMS curing agent and PDMS base material, silicone elastomer, in a beaker (formation of bubbles)
 - Reduction of bubbles by ultrasound sonication

- Transfer of a droplet of this mixture onto a freshly acetone and isopropylalcohol cleaned glass slide
- $-\,$ Baking of the thus fabricated "lens" on a heating plate set to $150\,^{\rm o}{\rm C}$ for $10\,{\rm min}$
- Fabrication of thin layers of polycarbonate (PC)
 - Usage of a mixture of 3 to 5 % PC and anisole by weight
 - Ultrasonication until all PC is dissolved completely
 - Preparation of two cleaned glass (isopropyl alcohol) slides and a pipette
 - Covering approximately one third of a glass slide with the PC/anisole mixture using the pipette
 - Placing a second glass slide on the film, gently rubbing back and forth until the film is homogeneous
 - Quickly pulling off the top glass slide
 - Curing the liquid film by placing the glass slide on a hot plate set at 150 °C for 20 min
- Merging of PDMS lens and PC layer
 - Making a hole in a strip of Scotch $\mathrm{Tape^{\mathrm{TM}}}$ using a hand punch
 - Apply Scotch TapeTM with hole to a PC film, cutting of the PC along the tape edge with a scalpel
 - Carefully peel off the tape and then apply the PC film under tension to a cleaned PDMS lens in such a way that there is no Scotch TapeTM on the lens
 - Fixing of the PC/Scotch TapeTM with a more heat resistant TesaTM strip
- Actual pick-up and stamping process
 - Usage of the copper specimen holder with hole for the suction vacuum on the piezo stage
 - Placing the glass slide with PDMS lens and PC film on a hot plate set to 100 °C for good contact between lens and PC
 - Placing and fixing the substrate (from which the desired flakes shall be pickedup) on the specimen holder by means of the aspiration vacuum
 - Inserting the glass slide with the PDMS lens into the micromanipulator (lens pointing downwards)
 - Positioning of the piezo stage such that the flakes to be picked up are under the PC film (bubbles and light scratches can be used for alignment later)
 - Lowering of the glass slide in the direction of the substrate until contact is made (meniscus should just not be above the target flake)
 - Heating up the copper block to 124 °C by setting 30 V at the direct current (DC) power supply

C. Details on the exfoliation and stamping of van der Waals materials

- Making marks on the television (TV) screen that transmits the image of the zoom lens with foil pen (flake position relative to concise strokes or scratches) for later alignment purposes
- Quick and complete retraction of the glass slide as soon as the copper block has reached a temperature of 124 °C (The flake should now be lifted from the substrate to stick to the PC. This flake can now be used to pick up further flakes subsequently in the same way and/or to stamp these onto a new target substrate)
- Switching off the power supply and allowing the copper block to cool down to 60 °C before further pick-ups/stamping follow
- Final stamping: Complete melting of the PC film by heating the copper block to $185\,^{\circ}\mathrm{C}$
- Slow and complete retraction of the glass slide as soon as the copper block has reached a temperature of $185\,^{\circ}\mathrm{C}$
- Removal of the PC film in a chloroform bath for $2\,\mathrm{min},\,\mathrm{dry}$ blowing with N_2
- Creating photos of the transferred stack with 100× (with and without the A-Stop filter), 20× and 4× magnifications
- Heating of the chip onto which has been stamped on to $150 \,^{\circ}\text{C}$ for $5 \,\text{min}$ in forming gas atmosphere (pressure $1 \times 10^1 \,\text{mbar}$)

In this chapter D, further developed techniques as well as samples that represent essential stages of this thesis are presented.

D.1. Using tungsten disulfide nanotubes in nano-fabrication

This section presents the proof of principle of two small-scale complementary side projects. These fabrication methods were not further utilized afterwards but can easily be applied to other materials. They open thus a wide playground for more complex devices. WS_2 nanotubes are used as local masks for the lithographic definition of device features exceeding the size scales of OL and EBL.

Firstly, WS_2 multi walled nanotubes are used as etch mask in a RIE process, leading to a narrow and straight protected area of the substrate below. Secondly, the nanotubes are used as shadow mask during metal deposition, for the fabrication of straight and narrow gaps in metal regions.

The WS_2 nanotubes were fabricated in the group of M. Remškar at the Institute Jožef Stefan Ljubljana, Slovenia. The nanotubes typically have a diameter of several 10 to 100 nm and are several 10 to 100 µm long [137].

D.1.1. Using a tungsten disulfide nanotube as an etch mask for niobium diselenide

The definition of a long and narrow, quasi 1D channel in a thin superconductor such as a NbSe₂ flake may enable the observation of quantum phase slips [62, 141]. With this objective in mind, the feasibility of using a WS₂ nanotube as etch mask has been tested. We want to use a WS₂ nanotube as an etching mask in order to create a very narrow superconducting channel in a NbSe₂ flake. Figure D.1 shows the schematic device fabrication process. A NbSe₂ flake is deposited by dry stamping on a Si++/SiO₂ chip in N₂ atmosphere [167]. Using the hot pick-up method [175], a hBN flake is first picked up and then used to pick up a WS₂ nanotube from another substrate. The resulting stack is then transferred on top of the NbSe₂ flake. By means of an optical microscope, we estimate the combined thickness of the hBN and NbSe₂ flakes to ~ 12 nm and the diameter of the WS₂ nanotube encapsulated by them to ~ 60 nm [235].

Next, four 1D-edge contacts to the $NbSe_2$ layer are fabricated similar to [162, 195]. In a first EBL step, the contacts to $NbSe_2$ are patterend in a layer of a PMMA resist. The resist serves as etch mask for the subsequent RIE process where the unprotected

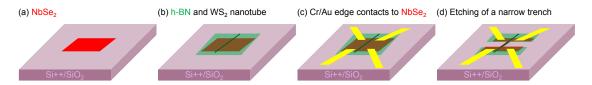


Figure D.1.: Schematic sample fabrication process using a WS_2 nanotube as an etching mask for $NbSe_2$. (a) A $NbSe_2$ flake is stamp-transferred on top of a Si ++/SiO₂ chip. (b) Afterwards a WS_2 nanotube picked-up with a hBN flake is put on top. (c) Then the $NbSe_2$ flake is edge-contacted with Cr/Au leads. (d) After a RIE process, only a narrow strip of $NbSe_2$ underneath the WS_2 nanotube remains as link between the pairwise contacts.

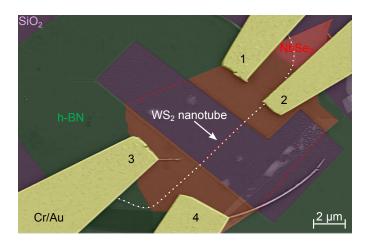


Figure D.2.: Colored SEM image. The WS_2 nanotube is highlighted with the dotted white line. The red dashed lines indicate the initial size of the red-colored $NbSe_2$ flake.

areas of the 2D crystals are removed completely. CHF_3/O_2 at a flow of $40 \operatorname{sccm}/6 \operatorname{sccm}$, a pressure of $35 \operatorname{mTorr}$ and a forward power of $35 \operatorname{W}$. Directly afterwards, $1 \operatorname{nm} \operatorname{Cr}$ as adhesion layer and $100 \operatorname{nm} \operatorname{Au}$ as contact metal for the $NbSe_2$ flake are deposited using electron beam assisted evaporation.

After a lift-off step, the device is characterized at a probe station. At room temperature, this technique resulted for this particular sample in a contact resistances of $\sim 1 \text{ M}\Omega$ in two-point geometry for all combinations of electrodes.

In a second EBL step, we define a rectangular etch window cutting across the 2Dmaterial stack. Within this etch window, only the WS₂ nanotube covers the stack, protecting the narrow region below it from anisotropic RIE etching. An earlier work in Regensburg has determined a nominal etching rate of $\sim 0.8 \frac{\text{nm}}{\text{s}}$ for graphene/hBN stacks [247] for the above mentioned RIE process. In order to ensure complete etching through the stack, we choose an etch time of 2 min, i. e., a nominal etch depth of 96 nm in hBN. Figure D.2 shows a colorized SEM image of an as fabricated sample. The WS₂ nanotube is still visible after the lift-off whereas the NbSe₂ in the L-shaped etching is removed completely. The red-dashed line indicates the original size of the $NbSe_2$ flake. Inside this area some residues attributed to the etching process are visible.

In two-point measurement, we could still measure a resistance between contacts 1-2 and 3-4 of $\sim 1 \,\mathrm{M}\Omega$. Unfortunately, the RIE process was far too aggressive and we could not measure a current across the small strip underneath the WS₂ nanotube. It was precisely the result of this device that let us redetermine the etch rates of the vdW materials we used, as described in section 5.8.

D.1.2. Creating narrow trenches in metal strips using a tungsten disulfide nanotube as a shadow mask

We want to define narrow trenches of a gap width down to $\sim 10 \text{ nm}$ in metal structures using WS₂ nanotubes. With standard EBL, it can become difficult to achieve a proper lift-off when the gap width shall become smaller than 30 nm and its width longer than a few µm [211, 237].

The schematic sample fabrication process is depicted in figure D.3. For a proof of



Figure D.3.: Schematic sample fabrication process using a WS_2 nanotube to create narrow gaps in metal films. (a) WS_2 nanotubes are transferred onto a $Si + +/SiO_2$ chip into the desired position. (b) A metal film 1 nm Cr/100 nm Au was thermally evaporated on top. (c) Usage of an ultrasonic bath removes the WS_2 nanotubes and thus defines the trenches.

concept, we transferred several WS_2 nanotubes onto this chip by picking them up from a growth substrate with blue tape. For envisioned applications, a desired WS_2 nanotube can instead be transferred from the growth substrate to a predefined position using the pick-up stamping technique similar to [175] as described in section D.1.1. The deposited WS_2 nanotubes are located on the chip via optical microscopy. In an EBL process, we define the areas where the desired metal film (in our case 1 nm Cr/100 nm Au) is deposited. After a lift-off with a syringe, the chips are placed in an ultrasonic bath for 1 min, which lifts the nanotubes off the chip. For this purpose, the chips are placed in a container filled with iso propylalcohol. They are then blown dry with N₂.

Figure D.4 shows SEM images with the as-defined trenches for three different devices. Note that for all devices the trenches are completely straight and the edges are very sharp, especially when compared to standard EBL/lift-off techniques. In figure D.4(a), the nanotube diameter is for sure larger than the metal height. In this case, a trench is naively expected to occur. Additionally, even when the WS_2 nanotube diameter is smaller than the metal height such that it is fully covered by metal, the ultrasonication process results in a well-defined trench, see figures D.4(b,c). The diameter of the WS_2

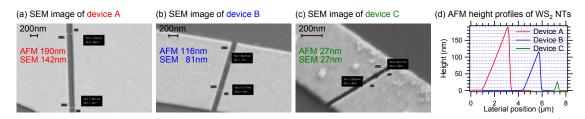


Figure D.4.: (a) - (c) SEM images of three different devices. The upper numbers in each panel indicates the AFM-determined thickness of the used WS_2 nanotube. The lower number notes the width of the resulting trench measured by an SEM. (d) AFM height profiles of the three different devices.

nanotube, determined via AFM, is comparable to the SEM-determined width of the resulting trench. In particular for tubes with large diameter, the AFM will overestimate their diameter due to the finite tip size.

D.2. Carbon nanotube contacted with two graphite flakes (sample 055)

In the beginning, it was not clear at all that a CNT could be electrically connected to a $NbSe_2$ flake. Hence, our activity started with the idea of electrically contacting a CNT with two graphite flakes. This is a natural choice since both graphite and CNT consist of the same chemical building block, namely graphene.

An SEM image as well as the room temperature gate trace are shown in figure D.5. At room temperature the device shows a conductance of ~ 4 μ S. Exfoliation and stamping were performed at ambient conditions by Anh-Tuan Nguyen [213]. The length of the measured CNT portion is ~ 10 μ m. The graphite contacts froze at ~ 100 K when measured in three different cryogenic setups and came back to life when going to higher temperatures again. We blame water present somewhere in the sample stack to cause this freezing out.

D.3. First electrical contact between carbon nanotube and niobium diselenide (sample 052)

Encouraged by the results gained from the sample described in section D.2, the next step toward the MF detection device was to contact a CNT not only with graphite flakes but also with a NbSe₂ flake. Figure D.6(a) shows an optical image of a sample where a CNT (indicated with the dotted white line) is contacted with flakes of graphite (framed with black lines) and NbSe₂ (framed with red line). NbSe₂ itself is also contacted with green line) from the top. The graphite flakes are labeled from 1 to 7 and contacted via 1 nm Cr/100 nm Au leads (not shown in the image). Exfoliation and stamping were performed

D.3. First electrical contact between carbon nanotube and niobium diselenide (sample 052)

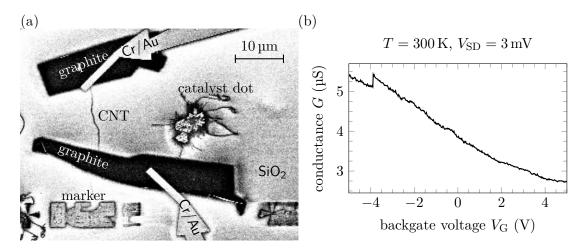


Figure D.5.: Sample 055 (first electrical contact between CNT and graphite). (a) The SEM image shows a CNT contacted with two graphite flakes (CNT length between flakes $\sim 10 \,\mu\text{m}$). The graphite flakes themselves are then equipped with metal contacts (1 nm Cr/100 nm Au). (b) At room temperature, the DC conductance G becomes smaller by a factor of two as the gate voltage $V_{\rm G}$ increases.

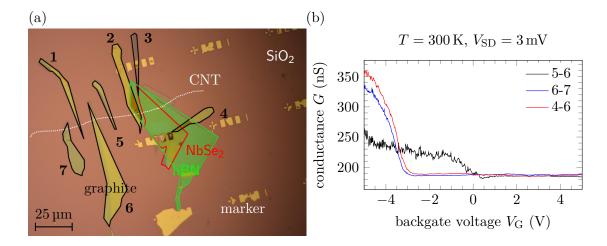


Figure D.6.: (a) Optical image of sample 052 (first electrical contact between CNT and NbSe₂). The CNT is highlighted with the dotted white line. The black surrounded flakes are graphite contacts (labeled from 1 to 7). A NbSe₂ flake (red surrounded) is covered with a hBN (green area). (b) Room temperature gate traces for the three pairs of working contacts.

at ambient conditions by Anh-Tuan Nguyen [213].

The number of pairwise contacts showing a conductance as well as the corresponding room temperature gate sweep are shown in figure D.6(b). The lengths of the measured CNT portions vary from 10 to $25 \,\mu\text{m}$. The resulting resistance is about 2.86 to $5.45 \,\text{M}\Omega$. This was the first successful demonstration of a CNT-NbSe₂ electrical contact. Due to a lack of cryostat time, this sample could not be measured right after fabrication. After five weeks in vacuum, the sample did not show any conductance anymore. Note that this was the first usage of CNTs grown from Co in 1D-2D hybrid vdW device fabrication in Regensburg.

D.4. First Majorana fermion detection device at low temperatures (sample 103)

The sample layout and the results of the transport measurements of the first MF detection device (sample 103) working at low temperatures is presented in figure D.7. We attribute the rather large charging energy to a gigantic defect. Coulomb diamonds only touch each other in clean systems [165]. The contact resistance between CNT and NbSe₂ was determined to be $\sim 22 \text{ M}\Omega$. Exfoliation and stamping were performed at ambient conditions by Anh-Tuan Nguyen [240]. The metal leads (1 nm Cr/100 nm Au) were fabricated by Lorenz Bauriedl [227] within his bachelor's thesis.

D.5. First edge contacts to a carbon nanotube in Regensburg (sample 150)

Figure D.8 presents the sample layout and the results of the transport measurements of sample 150. This was the first sample on which the fabrication of 0D edge contacts to CNTs was tried for the first time in Regensburg - with success. Exfoliation and stamping were performed at ambient conditions by Michaela Eichinger [248] within her master's thesis. At room temperature, the contact resistance values are in order of M Ω . At low temperatures, the resistance becomes 2 orders of magnitude worse.

D.6. First edge contacts to niobium diselenide in Regensburg (sample 167)

For the first time, edge contacts on (half-encapsulated) NbSe₂ were realized in sample 167. It is a four-terminal device, of which all contacts worked. Figure D.9 shows an optical image and a table of pairwise contact resistances. This sample served as a proof of principle and was not tested at low temperatures. Exfoliation and stamping was performed by Michaela Eichinger in N₂ atmosphere [248]. The pairwise contact resistance values range from tens of k Ω to tens of M Ω .

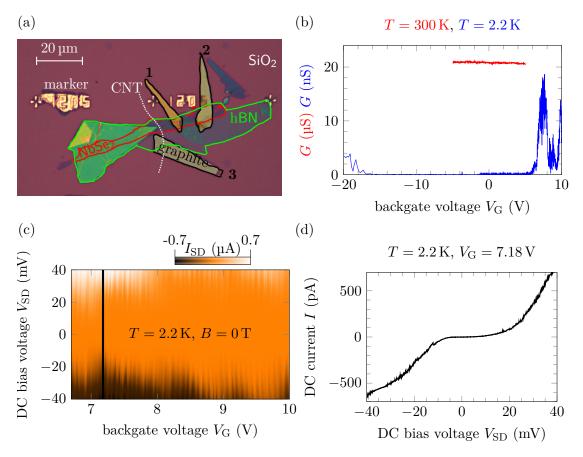


Figure D.7.: Sample 103 (first MF detection device at low temperatures). (a) The optical image shows a CNT (marked with dotted white line) on which a NbSe₂ flake (outlined in red) has been stamped. This as well as the CNT was then covered with graphite flakes (outlined in black). The contacts are numbered from 1 to 3. Contact 2 did not work. The following measurements always took place between contacts 1 and 3. (b) Conductance G as a function of gate voltage $V_{\rm G}$ at room temperature (red) and at 2.2 K (blue). In the former case, only a very small gate voltage dependence (< 3%) is discernible. At low temperatures, a large gap is observed. The conductance has its maximum in the region of $V_{\rm G} \sim 7 \,\mathrm{V}$ and is about three orders of magnitude lower than at room temperature. (c) The stability diagram shows a Coulomb charging pattern characteristic of a chain of QDs [50, 57, 67]. (d) Cut along the black vertical line in (c). In the linear region of the IV characteristic ($|V_{\rm SD}| > 16 \,\mathrm{mV}$), a linear fit can estimate the contact resistance between CNT and NbSe₂ to ~ 22 M\Omega.

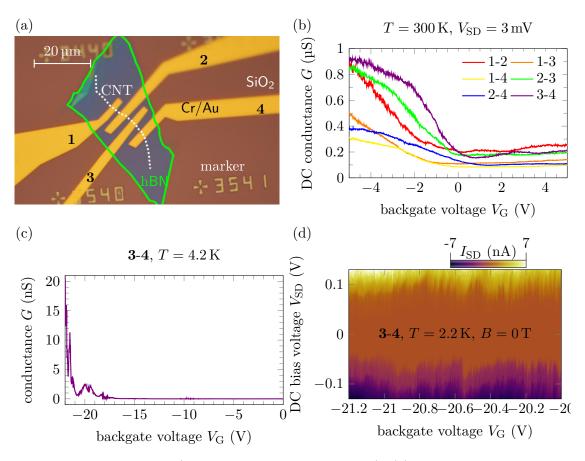
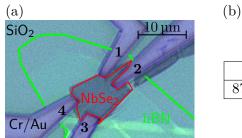


Figure D.8.: Sample 150 (first 0D edge contacts to CNT). (a) The optical image shows a hBN flake (outlined in green) stamped onto a CNT (highlighted by dotted white line) grown on an $Si++/SiO_2$ substrate. Through an RIE process and metalization (1 nm Cr/100 nm Au), four 0D edge contacts to the CNT (numbered from 1 to 4) were fabricated. (b) Conductance of all pairwise contact possibilities as a function of the gate voltage at room temperature. The conductance is greater for negative voltages than for positive voltages. (c) The conductance of contacts 3-4 shows a current flow two orders of magnitude lower than at room temperature only beyond 4.2 K in the negative gate voltage range. (d) The stability diagram of the same contact configuration shows a Coulomb charging pattern that is characteristic of coupled QDs [50, 57, 67].

D.7. Majorana fermion detection device with low contact resistance (sample 160)



`	$T = 300 \mathrm{K}$						
[1-2	1-3	1-4	2-3	2-4	3-4	
	$87\mathrm{k}\Omega$	$91\mathrm{k}\Omega$	$77\mathrm{M}\Omega$	$3.7\mathrm{M}\Omega$	$83\mathrm{M}\Omega$	$71\mathrm{M}\Omega$	

Figure D.9.: Sample 167 (first edge contacts to $NbSe_2$). (a) Optical image of a hBN (marked green) half-encapsulated $NbSe_2$ flake (marked red). The four Cr/Au edge contacts are numbered from 1 to 4. (b) Table with contact resistances in pairs at room temperature.

D.7. Majorana fermion detection device with low contact resistance (sample 160)

Once the edge contacts to CNTs were established in Regensburg, the MF detection devices fabricated with them included those with relatively low contact resistance $\ll 100 \text{ k}\Omega$. As an example, sample 160 is presented in figure D.10. At that time, the low contact resistance of this sample was *suspicious* that there might be an overlooked failure during fabrication. After the short transport measurement, this sample was discarded. After months this sample was not alive anymore. Exfoliation and stamping was performed by Michaela Eichinger in N₂ atmosphere [248] within her master's thesis.

D.8. Constriction in niobium diselenide (constriction 18)

In this section, we present the sample layout and low temperature transport results on another sample with a constriction patterned in a $NbSe_2$ flake similar to the device presented in chapter 7.

Figure D.11 shows an optical image of sample constriction 18. Using dry-stamping, a NbSe₂ flake (red dashed line) was transferred onto a Si++/SiO₂ substrate. Afterwards it was half encapsulated with hBN (green dashed line) from the top. By means of optical contrast, one may estimate a layer number variation between bilayer (right end) to five-layer (center part). The exfoliation and stamping was performed by Ferdinand Hölzl within his bachelor's thesis [268]. By means of EBL, RIE and thermal evaporation several edge contacts (1 nm Cr/100 nm Au) were designed. A constriction (width 350 nm, length 4 μ m, aspect ratio 1 : 11.4) was manufactured afterwards using EBL and RIE techniques.

As indicated in figure D.11, three edge contacts did not show an electric connection to $NbSe_2$ (labeled as "dead"). Contact 3 is trivially shorted to the contact to its right via an Au artifact due to a defective lift-off. For the relevant measurements, only the contact labeled "3" out of these two was used. Table D.1 summarizes the three different contact configurations used for the low temperature measurements. The latter were performed in

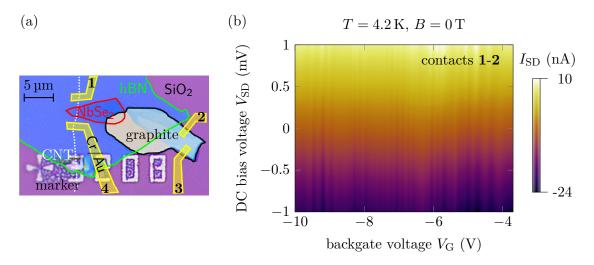


Figure D.10.: Sample 160 (MF detection device with low contact resistance). (a) The optical image shows a CNT (indicated by the dotted white line) onto which a NbSe₂ flake (outlined in red) and then hBN (outlined in green) have been stamped. NbSe₂ is contacted with a graphite flake (outlined in black). The CNT and graphite were contacted in one step with edge contacts (1 nm Cr/100 nm Au, not visible in the image, indicated in yellow). The contacts are labeled from 1 to 4. Contact 4 did not work. (b) Stability diagram at 4.2 K. Source and drain contact were applied to contact 1 and 2, respectively. The contacts were extremely transparent and showed a contact resistance of ~ 40 k\Omega.

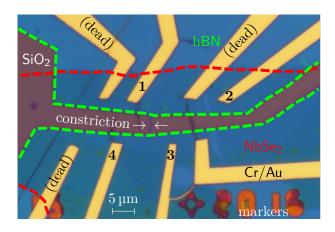


Figure D.11.: Optical image of sample *constriction 18*. Via EBL and RIE techniques a constriction (width 350 nm, length 4 μ m, aspect ratio 1 : 11.4) is patterend in a hBN (green dashed line) half encapsulated NbSe₂ flake (red dashed line) contacted with Cr/Au edge contacts.

Table D.1.: Overview of contact configurations used in low-temperature transport measurements of sample *constriction 18. I* and V label the contacts which where used to measure the current/voltage drop according to subsection 3.3.2.

name	contact 1	contact 2	contact 3	contact 4
ccA	I (source)	V	V	I (drain)
ccB	I (source)	I (drain)	_	_
ccC	_	_	I (source)	I (drain)

a 1 K-stick.

Figure D.12 displays the dependence of the differential resistance R, measured with four terminals across the constriction, on current bias, temperature and perpendicular magnetic field for contact configuration (cc) A. Panel D.12(a) displays the differential resistance as a function of both, temperature and current bias and panel D.12(b) shows some selected temperature traces in absence of perpendicular magnetic field B_{\perp} . At low temperatures, a series of peaks in the differential resistance, corresponding to non-linear IV characteristics and typical of PS events, is discernible. In the region of low current bias $I_{\text{SD}} \leq 1 \,\mu\text{A}$, a minimum is instead observed which is not zero but has a finite value. We relate this effect either to a normal conducting region inside the constriction or to insufficient filtering. While increasing the temperature, the peaks bend towards zero current and the minimum is elevated. None of these features are detectable above 4 K.

Panel D.12(d) displays a contour map of the differential resistance plotted as a function of current bias $I_{\rm SD}$ and perpendicular magnetic field B_{\perp} at T = 1.5 K and panel (e) displays selected line traces. The critical currents of the maxima in the differential resistance are reduced by increasing the magnetic field. From a field of 3 T at the latest, the peaks are no longer visible. In contrast to sample *Majorana 20*, the behavior here is not linear, but curved and the maxima are not visible up to the zero current line at higher fields. The baseline of the differential resistance shifts to larger values for $B_{\perp} \ge 2$ T. As in sample *Majorana 20*, increasing the field turns the minimum at low current bias $I_{\rm SD} \le 1 \,\mu\text{A}$ into a maximum. The resistance value of this maximum can be slightly decreased when increasing the temperature from 1.5 to 6 K, as shown in panel D.12(c) (brown trace). The saturation field here is slightly higher than in sample *Majorana 20*.

The black traces in panels D.11(c,f) present the temperature/magnetic field dependence of the differential resistance at $I_{\rm SD} = 0 \,\mu \text{A}$ and $B_{\perp} = 0 \,\text{T}/T = 1.5 \,\text{K}$, respectively. The differential resistance increases by increasing temperature as well as magnetic field and saturates at 4.5 K/5 T.

Despite the fact that in this sample again no zero voltage drop could be measured across the constriction, the maxima in differential resistance as well as the minimum for low current bias are very characteristic signs for PSLs, compatible with reference [255].

A dependence of the differential resistance R on gate voltages $-30 \text{ V} \leq V_{\text{G}} \leq 30 \text{ V}$ applied to Si++ could not be observed at low temperatures. Attempts to use an Li ion-based substrate for solid ion gating in other samples have been unsuccessful [196,

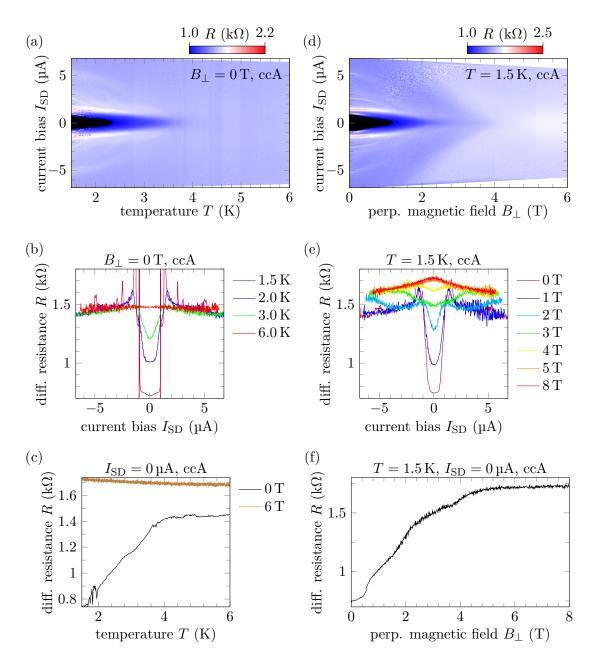


Figure D.12.: Low temperature transport characteristics of sample *constriction 18*, ccA. (a) to (c) temperature and (d) to (f) perpendicular magnetic field dependence of the differential resistance.

207, 236].

The constriction divides the NbSe₂ flake into an upper (ccB)/lower bank (ccC). Figure D.13 shows their low temperature transport characteristics in panels (a,b)/(c,d), respectively. These measurements were each performed only with two-terminals according

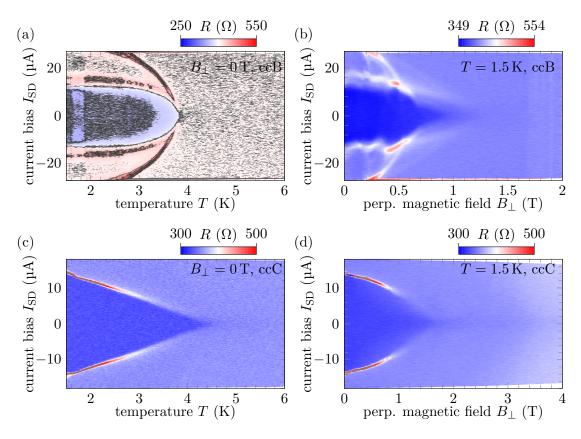


Figure D.13.: Temperature and magnetic field behavior of the differential resistance R of the NbSe₂ banks (sample *constriction 18*) for (a,b) ccB and (c,d) ccC. These data were aquired using a two-terminal measurement according to table D.1.

to table D.1. In the left/right column, the current bias and temperature/magnetic field dependence of the differential resistance is shown in the form of a contour plot.

In subfigure D.13(a), the various resistance maxima of the upper bank unite at a common point $(3.8 \text{ K}, 0 \,\mu\text{A})$, as it is the case in reference [255]. The critical current also lies in the $\sim 10 \,\mu\text{A}$ range. The magnetic field behavior in subfigure D.13(b) instead differs. It shows oscillations up to fields of 0.6 T. For higher fields, the PSLs get washed out before reaching zero current.

At the lower bank, only a single PSL is noticeable in the examined current bias range. Its critical current drops almost linearly to zero current with temperature, see panel D.13(c). In the perpendicular magnetic field, see panel D.13(d), it is concave for positive currents. For fields above 1 T this line blurs.

More than another ten constriction samples were processed as part of this work. Some of them became unusable in the course of fabrication due to demolition (rupture of the flake during spin-on of PMMA or during lift-off, bubbles). Others showed no conduction over the constriction after etching. Still other samples showed low contact resistances of below $1 k\Omega$, but only perfect ohmic behavior and no sign of superconductivity, due to an oxidized bulk crystal at low temperatures.

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Eidesstattliche Erklärung

Ich erkläre hiermit an Eides statt, dass ich die vorliegende Arbeit ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt habe; die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe des Literaturzitats gekennzeichnet.

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Die Arbeit wurde bisher weder im In- noch im Ausland in gleicher oder ähnlicher Form einer anderen Prüfungsbehörde vorgelegt.

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