Coulomb Blockade Measurements on MoS_2 Nanotubes and Nanoribbons



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1. Introduction

Since the fabrication of the first integrated circuits, the exponential increase of computational power has been driven by continuous miniaturization of semiconductor devices. This was famously encapsulated by Moore's prediction that the number of components per chip would double every 18–24 months [Moore, 1965]. This empirical trend, known as Moore's law, held for several decades and became the foundation of modern electronics (figure 1.1(a)). A retrospective analysis, however, showed that the the transistor density (transistors per unit area) evolved through two logistic regimes, with doubling times of 17 and 33 months, respectively (figure A.1(a)). Since about 1999, the density increase has departed from exponential growth, progressing instead in successive technological waves (figure 1.1(b)), each driven by innovations in materials and device architecture. Examples include the introduction of the metal-oxide-semiconductor (MOS) field effect transistor (FET) in 1964 [Norman and Stephenson, 1969] (line B) and the development of high-density short-channel MOSs [Koo, 1976] leading to the Intel *i486* in 1989 (line E). With physical scaling limits now manifesting through leakage currents and power dissipation, further advances in information processing demand a fundamental shift in technology.

Today, commercial logic transistors approach sizes as small as 2 nm [Bautista, 2025], and large-scale production is currently centered around the 3 nm node. At these dimensions, short-channel effects, quantum tunneling, and process-induced variability severely constrain performance. In this context, beyond-silicon materials are considered a key avenue for extending and transforming semiconductor technology. Among them, two-dimensional (2D) materials, such as the Transition Metal Dichalcogenides (TMDCs), have garnered significant interest due to their atomic-scale thickness, superior electrostatic control, and prospect of building van-der-Waals heterostructures with tunable properties for a wide range of applications [Novoselov et al., 2016, Tang et al., 2025]. As shown in figure 1.2, TMDCs have already been identified on the technology roadmap for next-generation field-effect transistors [Qiu et al., 2024,

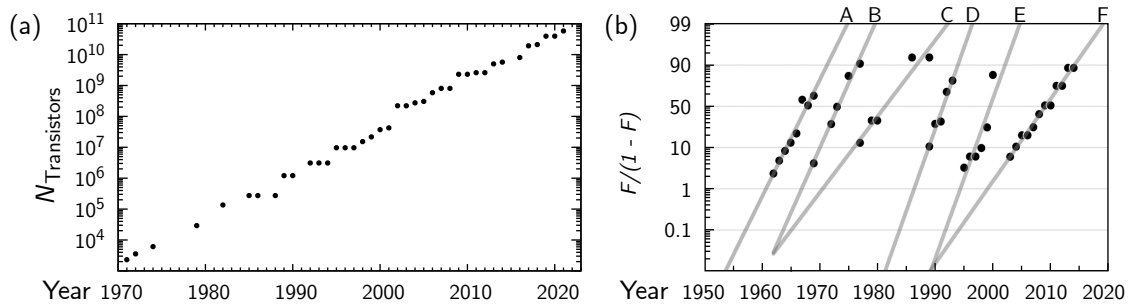


Figure 1.1.: Visualization of Moore's law. (a) Number of transistors per chip over the last five decades [Rupp, 2022]. (b) Decomposition of Intel processor transistor density into individual logistic growth components, each representing a distinct phase of technological evolution. Approximated second derivative. Figure adapted from [Burg and Ausubel, 2021].

Lockhart de la Rosa and Sankar Kar, 2025], and a notable milestone was recently achieved with the demonstration of wafer-scale fabrication of a 32-bit microprocessor based entirely on monolayer MoS_2 [Ao et al., 2025]. These developments demonstrate that 2D semiconductors can serve not only as research platforms, but also as viable candidates for industrial integration, showing improved processing speeds and reduced power consumption in logic circuits [Tang et al., 2025].

In parallel, quantum information science has emerged as a new paradigm for computation, with the potential to outperform classical computers in selected tasks such as quantum simulation and cryptography. Since Feynman's seminal proposal in 1981 to harness quantum systems for simulating quantum dynamics [Feynman, 1981], the realization of quantum computing has become a central research challenge across physics and engineering [Preskill, 2023]. Among the various hardware platforms under investigation, electrostatically defined Quantum Dots (QDs) in semiconductor materials offer a promising route toward scalable and coherent quantum computing architectures [Loss and DiVincenzo, 1998]. In materials such as GaAs, SiGe, bilayer graphene, carbon nanotubes (CNTs), etc., QDs have already demonstrated long coherence times and control over individual spins and charges, enabling prototype implementations of quantum gates [Chatterjee et al., 2022, Recher and Trauzettel, 2010, Burkard et al., 2023].

TMDCs have emerged as highly versatile host materials for quantum devices. They cover a wide range of electronic characteristics, from metallic (e.g. $NbSe_2$) and semimetallic (e.g. WTe_2) to semiconducting (MoS_2) and insulating (e.g. hexagonal boron nitride (hBN)). Their intrinsic 2D geometry enforces strong electro-

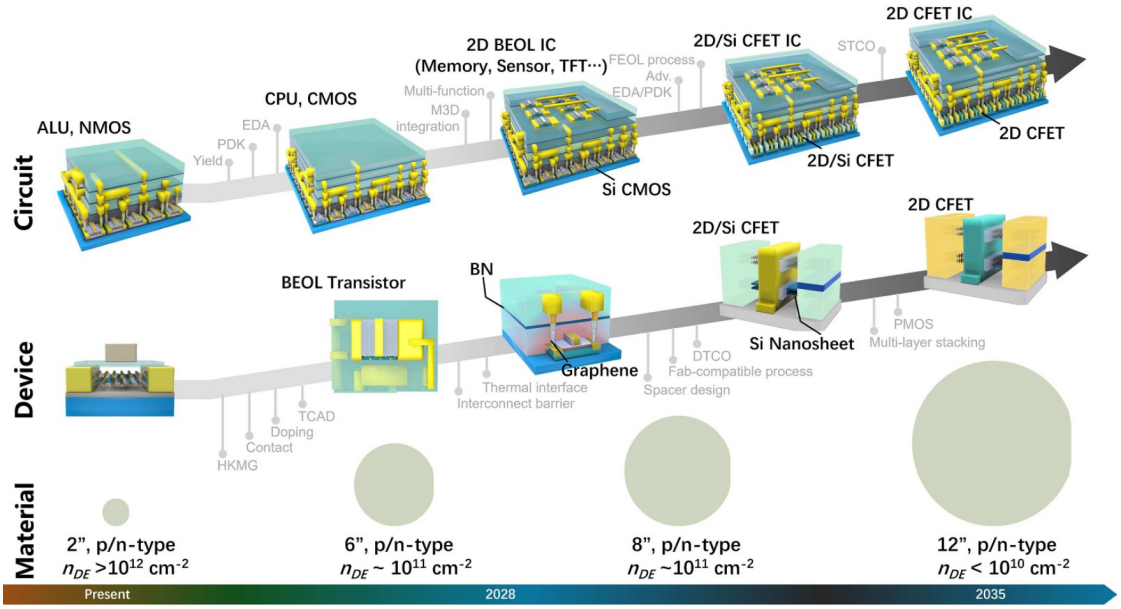


Figure 1.2.: Roadmap illustrating the envisioned development of 2D materials from synthesis to large-scale electronic integration. The progression from current Si-based Complementary Metal–Oxide–Semiconductor (CMOS) technology toward hybrid 2D/Si and ultimately fully 2D Complementary Field-Effect Transistor (CFET) architectures is shown across material, device, and circuit levels. Each stage highlights improvements in wafer size, carrier density uniformity, and functionality, projecting advances from present 2 inch substrates to 12 inch wafers by 2035. Adapted from [Qiu et al., 2024].

static confinement perpendicular to the plane. The heavy transition-metal atoms endow the bands with strong atomic spin-orbit coupling (SOC). In monolayers, the lack of inversion symmetry allows SOC to lift the spin degeneracy at the K/K' valleys, yielding pronounced spin–orbit splittings and spin–valley locking [Kormányos et al., 2014, Wang et al., 2012, Novoselov et al., 2016]. In addition, isotopic purification can suppress hyperfine interactions, creating opportunities for spin–valley qubits with long coherence times [Avdeev and Smirnov, 2019]. The capability to vertically stack different 2D crystals, each with distinct band structures and properties, further expands the design space for engineered heterostructures and device architectures [Novoselov et al., 2016].

Within this material family, MoS_2 stands out as a semiconducting member that combines strong SOC with a direct band gap in the monolayer limit and excellent optical properties [Ye et al., 2015]. Remarkably, intrinsic superconductivity has also been demonstrated under ionic gating [Ye et al., 2012, Hsu et al., 2017]. These

features establish MoS_2 as a promising platform for exploring coherent quantum transport and hybrid quantum states.

A central challenge, however, lies in contacting 2D semiconductors. Contact resistances frequently dominate device performance and limit reproducibility [Wang and Chhowalla, 2022]. Even in bulk silicon, decades of work were required to optimize metal–semiconductor interfaces [Tung, 2014]. In 2D systems the situation is further complicated, as conventional transfer and fabrication methods often introduce disorder and contamination that can degrade contacts. Recent advances have mitigated this issue by employing semi-metallic contact materials. In particular, bismuth- and antimony-based contacts have been shown to yield ultra-low resistances approaching the quantum limit for 2D semiconductors [Shen et al., 2021, Li et al., 2023b]. This marks an important step toward highly transparent, non-invasive contacts that are essential for quantum devices.

Despite these advances, MoS_2 imposes stringent requirements on device geometry due to its comparatively large effective electron mass. With approximately $m_{\mathrm{eff}} \approx 0.5\, m_{\mathrm{e},0}$, compared to $\approx 0.067\, m_{\mathrm{e},0}$ in GaAs, the resulting level spacings are small, which necessitates extremely strong spatial confinement [Kormányos et al., 2014]. Achieving such minuscule confinement is therefore a prerequisite for realizing well-defined QDs and accessing the single-level transport regime in MoS_2 nanostructures.

One particularly attractive approach to narrow electronic confinement is the use of quasi-one-dimensional geometries. Nanotubes (NTs), in contrast to planar structures, intrinsically confine carriers in the radial and azimuthal directions, requiring only the lithographic confinement along the NT axis. NTs of MoS_2 have been known for nearly three decades [Feldman et al., 1995], and their synthesis by chemical vapour transport (CVT) yields high-quality, multi-wall structures with diameters down to 20 nm and lengths up to several 100 µm, exhibiting low defect densities [Remškar, 2004].

In this thesis, MoS_2 NTs are combined with this new class of contact materials to realize clean, contact-defined QDs. The resulting devices exhibit pronounced Coulomb blockade (CB) and excited-state transport, with evidence suggesting quantum confinement across the full contact-defined region. Furthermore, an analysis of fabrication strategies aimed at minimizing substrate-induced disorder and reducing contamination and defect formation during processing is presented. The findings establish the technological feasibility of QDs in MoS_2 NTs and represent a significant step toward the scalable integration of TMDC materials into quantum electronic devices.

This work is structured as follows:

- In chapter 2 the underlying physics of the system is described starting with an introduction to TMDC materials, followed by the theory of metal to semiconductor contacts. Then, NTs are examined, beginning with CNTs as a reference framework for the subsequently investigated MoS_2 NTs. Finally, the physics of QDs are discussed.
- Chapter 3 describes the device fabrication processes as well as the measurement equipment.
- Chapter 4 provides a brief overview of previously achieved advances of QDs in TMDC materials as published in literature.
- Chapter 5 details the advances developed in this work for realizing transparent and non-destructive contacts to MoS_2 NTs. The quality of these contacts is confirmed by room-temperature characterization, and the effects of fabrication methods and optimizations are analyzed to enable reproducible device fabrication.
- In chapter 6, CB measurements of devices fabricated directly on the SiO_2 dielectric are presented. These measurements provide evidence of single-level transport through QDs confined within the MoS_2 NTs. However, the observed disorder indicates that the amorphous SiO_2 substrate has a detrimental effect on the device quality.
- Chapter 7 documents experiments to mitigate substrate-induced disorder by suspending the NTs between the contacts and evaluating these devices at low temperatures.
- In chapter 8, an alternative approach is given to reduce substrate-induced disorder through the use of hBN, a highly crystalline 2D insulator, as the dielectric, and few-layer graphene (FLG) as uniform gate electrodes.
- Chapter 9 reports the investigation of NT-based QDs in parallel and perpendicular magnetic fields. Here, effective Landè g factors determined and the spin-splitting is evaluated.
- In chapter 10 the findings of this thesis are summarized, concluding with a discussion of potential future improvements and developments.

2. Theory

This chapter introduces the fundamental physical concepts relevant to the present work. As the central objective is the fabrication and characterization of QDs in MoS_2 NTs, a brief overview of the material is first provided, forming the basis for the discussed device structures.
Subsequently, the physics of semiconductor contacts is introduced, as these represent a key factor in the formation and control of QDs within semiconducting NTs. The general properties of NTs are then discussed, beginning with CNTs, which have been extensively studied and serve as an instructive reference. Based on the parallels between CNTs and MoS_2 NTs, the unique opportunities and remaining challenges of the latter, which remain comparatively unexplored, are outlined.
The chapter concludes with a focused discussion on QDs, the core physical entities at the heart of this work, including the basic mechanisms of charge quantization and energy-level formation that underlie their functionality.

2.1. Transition Metal Dichalcogenides

Before truly two-dimensional crystals were considered feasible, Kroto et al. uncovered fullerenes in 1985 [Kroto et al., 1985] and Iijima reported CNTs in 1991 [Iijima, 1991], yet monolayer graphite was still thought to be too unstable to isolate. In 2004, Novoselov and Geim demonstrated that simple mechanical exfoliation could yield graphene [Novoselov et al., 2004], prompting a reassessment of what was possible in low-dimensional materials. Within a year, this technique had been applied to a variety of van-der-Waals–bonded compounds, including TMDC, phosphorene, hBN, and other layered crystals [Novoselov et al., 2005]. These newly accessible monolayers displayed electronic and optical characteristics distinct from their bulk counterparts, sparking interest in their potential for nanoscale devices.
Figure 2.1 illustrates the basic geometry shared by atomically thin materials: a single plane of atoms arranged in a regular lattice and held together by strong in-plane

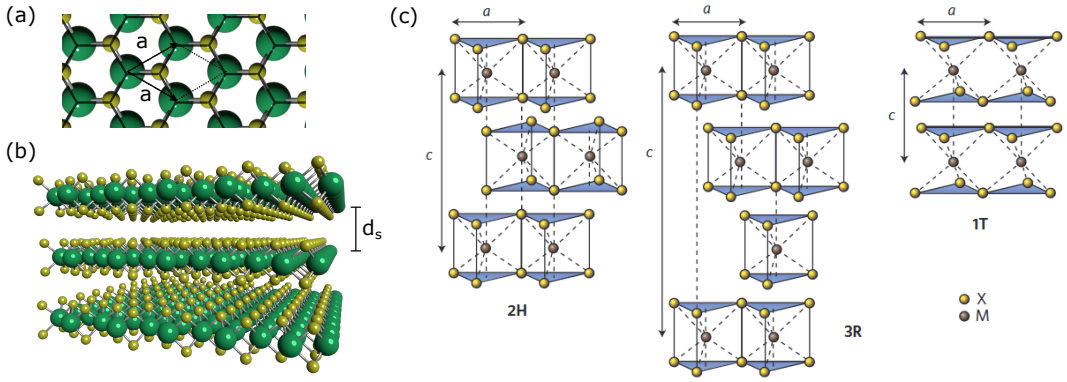


Figure 2.1.: Schematic of TMDC geometric parameters. (a) Hexagonal lattice superimposed on a TMDC in top view with the unit cell and the lattice constant a. (b) Side view on a van-der-Waals bound stack with the interlayer distance d_S. (c) Different possible structural polytypes of TMDC materials: 2H with trigonal-prismatic coordination, 1T with octahedral coordination, and 3R rhombohedral symmetry and trigonal-prismatic coordination. Adapted from [Wang et al., 2012].

bonds, with adjacent layers coupled only by weak van-der-Waals forces. In the simplest case, such as graphene, the honeycomb lattice arises from sp^2-hybridized carbon atoms sitting at the vertices of hexagons. More generally, 2D crystals can adopt a variety of lattice symmetries, such as hexagonal, square or even rectangular, depending on their underlying chemistry. Different stacking sequences not only alter the relative positions of atoms between adjacent layers but also reshape the phonon spectrum and interlayer electronic coupling. TMDCs occupy a distinctive niche: each monolayer consists of a plane of transition-metal atoms sandwiched between two planes of chalcogen atoms (see figure 2.2(b)). The precise coordination of the metal atom dictates the polytype: trigonal-prismatic coordination gives the so-called 2H phase (e.g. MoS_2 and WS_2), whereas octahedral coordination yields the 1T phase (e.g. TiS_2) shown in figure 2.1(c). In the former coordination, the sandwich structure sets the in-plane lattice constant (typically 3.1 Å to 3.2 Å for MoS_2) and leads to broken inversion symmetry in monolayers. This can, in turn, lead to spin–orbit splitting [Novoselov et al., 2016, Kormányos et al., 2014].

2.1.1. Band Structure of MoS_2

Depending on the base atoms and their coordination, TMDCs can either be metallic, semi-metallic or semiconducting. This thesis is restricted to the properties of

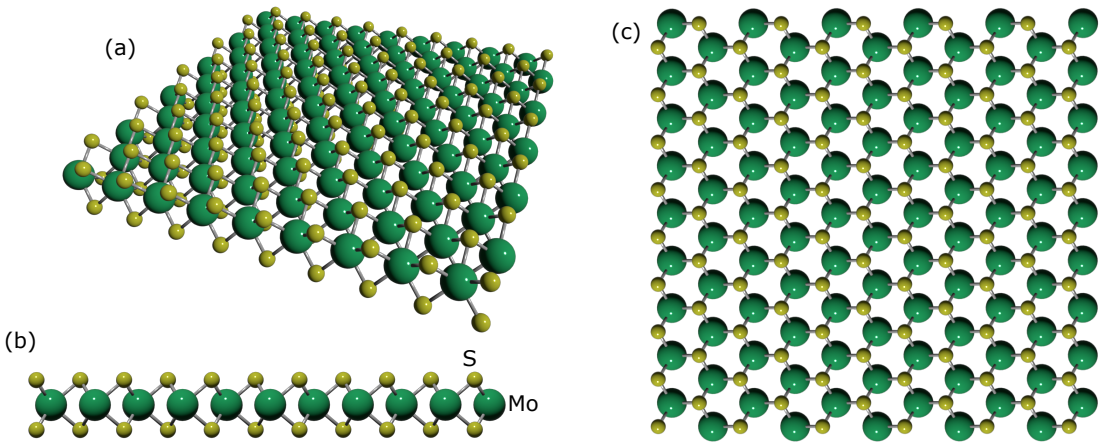


Figure 2.2.: Schematic of a single TMDC material layer of the 2H polytype with trigonal-prismatic coordination. The green atoms are the transition metal (e.g. Mo, W, Te, ...) and the yellow atoms the chalcogenides (e.g. S, Se, ...). (a) Perspective view, (b) side view and (c) top view.

semiconducting TMDCs, since the NTs investigated here are derived from these 2D materials.

Among the possible combinations, MoS_2 has received particular attention over the last decades. It is well known as a lubricant, due to the shearing effect between the loosely coupled stacked layers, since the last decade [William, 1929, Vazirisereshk et al., 2019]. Going from the bulk to the monolayer case a transition from an indirect band gap [Mattheiss, 1973] to a direct one (see figure 2.3) is observed, which also increases in its size (see table 2.1) [Lebègue and Eriksson, 2009]. The same effect can also be seen in the very similar $MoSe_2$, WSe_2, and WS_2 materials. As all of these materials are of the trigonal-prismatic polytype, they exhibit strong spin-orbit splitting in the valence bands. Together with their exciton-dominated optical spectra, this makes these materials an interesting platform for optoelectronics [Wang et al., 2012, Novoselov et al., 2016].

In addition to their band gap tunability, the effective mass of charge carriers in TMDC play a central role in determining their transport and confinement properties. The conduction and valence band curvatures, particularly near the K and Q points, set the scale for carrier mobility, tunneling rates, and quantization energies in low-dimensional devices. For instance, in monolayer MoS_2, the electron effective mass at the K-point is relatively large ($m_e^* \approx 0.45 m_0$), which enhances localization in QD geometries, while the hole mass is even larger due to strong spin–orbit coupling. The

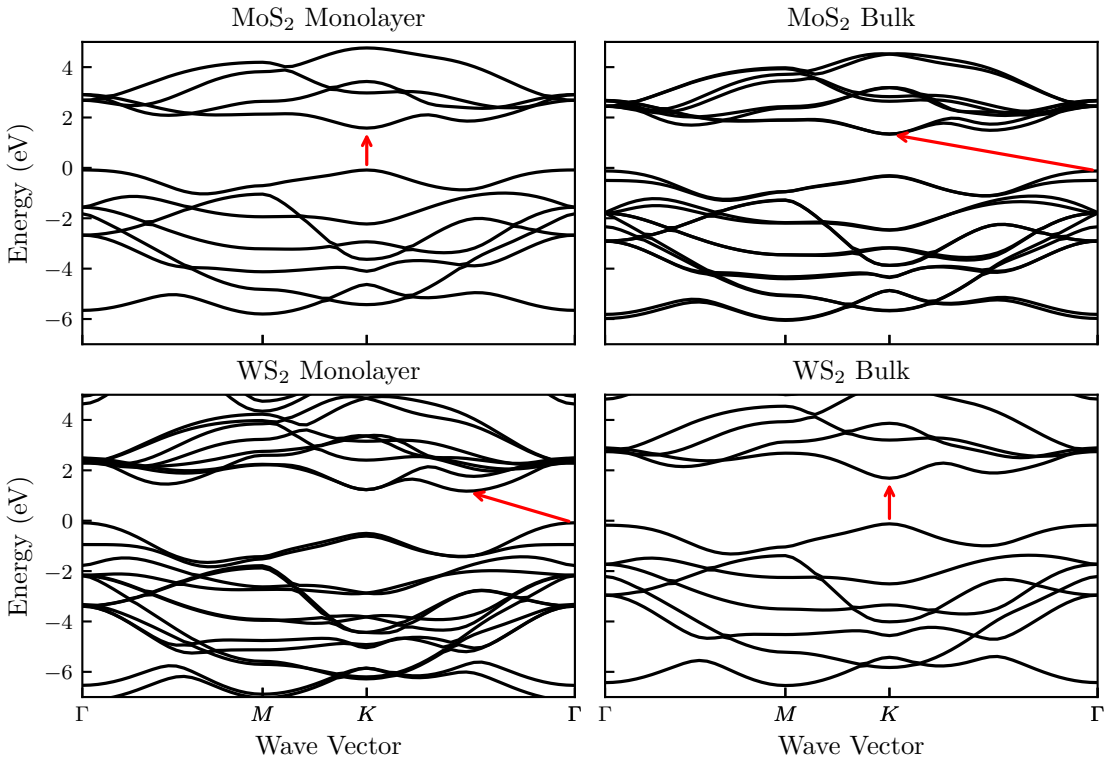


Figure 2.3.: Band structure of MoS_2 and WS_2 in both the bulk and monolayer case. The red arrows mark the band gap, showing a transition from direct to indirect for MoS_2 and the opposite for WS_2. Band structures were downloaded from the Materials Project [Jain et al., 2013].

values differ significantly across the TMDC family and between monolayer and bulk forms, reflecting the sensitivity of the band structure to both chemical composition and dimensionality. An overview of typical effective masses for electron and holes, lattice constants, and SOC at valence band maximum (VBM) and conduction band minimum (CBM) of different TMDCs are given in table 2.1.

Building on these band structure characteristics, it is natural to assess the intrinsic device limits of monolayer MoS_2 FET. Quantum transport simulations reveal that monolayer MoS_2 transistors exhibit exceptional electrostatic control due to their atomically thin body and sizable band gap, resulting in excellent subthreshold performance, with theoretical subthreshold swings approaching 60 mV decade^{-1} [Yoon et al., 2011]. While the ON-current is limited compared to III–V semiconductors due to the lower carrier velocities, ballistic transport models still predict competitive current densities, particularly when combined with high-k dielectrics [Liu et al., 2011]. In

Table 2.1.: Important geometric and electronic properties of a few exemplary TMDC materials. Given are the lattice constant a, the interlayer distance d_S, the band gap of both the bulk $E_{G,Bulk}$ and the monolayer $E_{G,1L}$, the effective masses of electrons m_e^* and holes m_h^*, and the spin-orbit splitting Δ_{SO} for the VBM and CBM.

	a (Å)	d_s (Å)	$E_{g,1L}$ (eV)	$E_{g,Bulk}$ (eV)	m_e^* (m_0)	m_h^* (m_0)	Δ_{SO}^{VBM} (meV)	Δ_{SO}^{CBM} (meV)
MoS_2	3.16[a]	6.18[b]	1.8[d]	1.2[d]	0.45[e]	0.64[b]	150[e]	1.5[g]
$MoSe_2$	3.30[a]	6.53[b]	1.5[d]	1.1[d]	0.43[h]	0.59[g]	183[g]	10.5[h]
WS_2	3.15[a]	6.22[b]	2.1-1.9[d]	1.4[d]	0.33[h]	0.30[h]	426[g]	13.5[h]
WSe_2	3.29[b]	6.58[b]	1.7[d]	1.2[d]	0.36[h]	0.30[h]	546[g]	19[h]

[a] [Liu et al., 2011]; [b] [Kylänpää and Komsa, 2015]; [c] [Yu et al., 2015];
[d] [Wang et al., 2012]; [e] [Yoon et al., 2011]; [f] [Zhu et al., 2011];
[g] [Kormányos et al., 2014] [h] [Conti et al., 2020].

both studies the relatively heavy electron mass at the K-valley caps the attainable carrier velocity and ultimately positions monolayer MoS_2 as a low-power rather than a high-performance logic material. Experimentally, exfoliated MoS_2 placed on thermally grown SiO_2 almost invariably behaves as an n-type semiconductor, a behaviour attributed to unpassivated oxide surface states and extrinsic adsorbates that pin the Fermi level close to the conduction band edge [Radisavljevic et al., 2011, Li et al., 2012, Ghatak et al., 2011].

2.1.2. Intrinsic Superconductivity

Beyond the semiconducting behavior of MoS_2, an insulator-superconductor transition can be achieved through strong electrostatic doping via an ionic-liquid electric double-layer transistor (EDLT). By combining a high-capacitance ionic liquid gate (DEME-TFSI) with a conventional back-gate, [Ye et al., 2012] were able to quasi-continuously tune the two-dimensional carrier density n_{2D} from the insulating regime into a superconducting dome peaking at $\approx 10.8\,\mathrm{K}$ around $n_{2D} \approx 1.2 \cdot 10^{14}\,\mathrm{m}^{-3}$. [Taniguchi et al., 2012] were able to independently confirm the onset of T_C in multilayer MoS_2 under similar ionic gating conditions. Importantly, the lack of inversion symmetry in monolayer MoS_2 locks spins out-of-plane, giving rise to an Ising superconducting state with in-plane upper-critical fields that substantially exceed the Pauli limit, characteristic of spin–orbit–protected two-dimensional pairing[Lu et al., 2015].

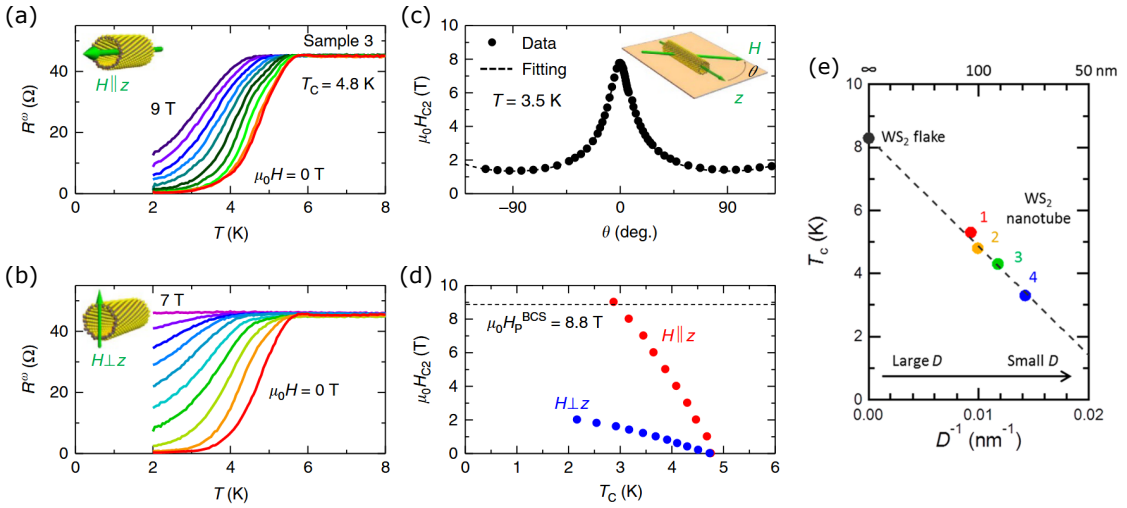


Figure 2.4.: Superconducting WS_2 NTs with ionic gating. Resistance vs. temperature plot for (a) different parallel magnetic fields and (b) perpendicular magnetic fields. (c) Angle dependence of the critical field fitted with an anisotropic Ginzburg-Landau model. (d) Evolution of the upper critical field H_{c2} with temperature for out-of-plane and in-plane magnetic field orientations. The Pauli limit is indicated by the dashed line for comparison. (e) Critical temperature of WS_2 NTs as a function of the radius of the nanotube. Adapted from [Qin et al., 2017] and [Qin et al., 2018].

More recently, analogous superconductivity has been reported in chiral WS_2 NTs, where the authors found a superconducting state similarly protected against parallel magnetic fields (and therefore in-plane, see figure 2.4(a-c)) with upper critical fields that seemingly go beyond the Pauli limit (see figure 2.4(d)) [Qin et al., 2017]. Later the authors were able to report a diameter dependent critical temperature, which followed the increasing radii up to the limit of planar WS_2 (similar to a NT with infinite radius), which can be seen in figure 2.4(e) [Qin et al., 2018].

2.2. Semiconductor Contacts

The following section provides an overview of the physics governing the Semiconductor (SC)–metal interface. The formation and origin of the Schottky barrier (SB) are discussed, followed by an examination of several theoretical models, including the Schottky–Mott rule, Fermi level pinning (FLP), and Metal induced gap states (MIGS). The influence of inhomogeneous SBs on the resulting transport characteristics is then addressed. A comprehensive review of these mechanisms are given in [Tung, 2014].

2.2.1. Schottky-Mott Rule

The first and most simple model of a SB at a metal-semiconductor-interface is given by the Schottky-Mott rule derived by Walter Schottky and Nevill Francis Mott in 1939 [Schottky, 1939, Mott, 1939]. Here, one can argue, the "actual" interface between the two materials is completely neglected. The electronic state of the system is kept invariant from the bulk case without any surface specific adjustments nor any interaction between metal and SC. Therefore, the barrier height is solely dependent on bulk material properties.

To determine the barrier height, the electronic states of the two materials must be compared. For the metal, the energy bands are occupied up to the Fermi energy E_F, and the metal work function ϕ_M is defined as the energy difference between E_F and the vacuum energy of a free electron. As the name implies, this is the energy needed to remove an electron from the metal. Similarly, for the SC, the ionization energy I_SC denotes the energy required to remove an electron from the valence band, while the electron affinity χ_SC corresponds to the energy gained when an electron enters the conduction band at E_CBM.

If an electron is to be transferred from the metal to the SC, the energy difference between ϕ_M and χ_SC of the SC must be overcome. Accordingly, the SB height is determined by the Schottky–Mott rule.

$$\Phi_{\mathrm{B},n} = \phi_\mathrm{M} - \chi_\mathrm{SC}. \tag{2.1}$$

Similarly, for hole transport, the same rule can be applied by a change of sign and substation of the electron affinity with the ionization energy

$$\Phi_{\mathrm{B},p} = I_\mathrm{SC} - \phi_\mathrm{M}. \tag{2.2}$$

This band alignment can be seen in figure 2.5(a). Both the metal and the SC remain unchanged at the interface, only the mean electrostatic potentials ($-e\bar{V}_{\mathrm{SC,M}}$) of the atomic lattice changes due to the mismatch between their structures without any relaxation effects. This is based upon the idea of a superposition of both the potentials upon contact, which is most certainly not the case in a real interface. However, due to its simplicity, it is still a useful starting point for determining the SB of an interface before more complex surface quantum-chemistry simulations.

2.2.2. Fermi Level Pinning

As it was indicated above, the Schottky-Mott rule does not describe the experimentally measured SB of the majority of metal-SC interfaces. One of the first ideas for a theory explaining the discrepancies came from semiconductor surface physics, with the so called charge neutrality level.

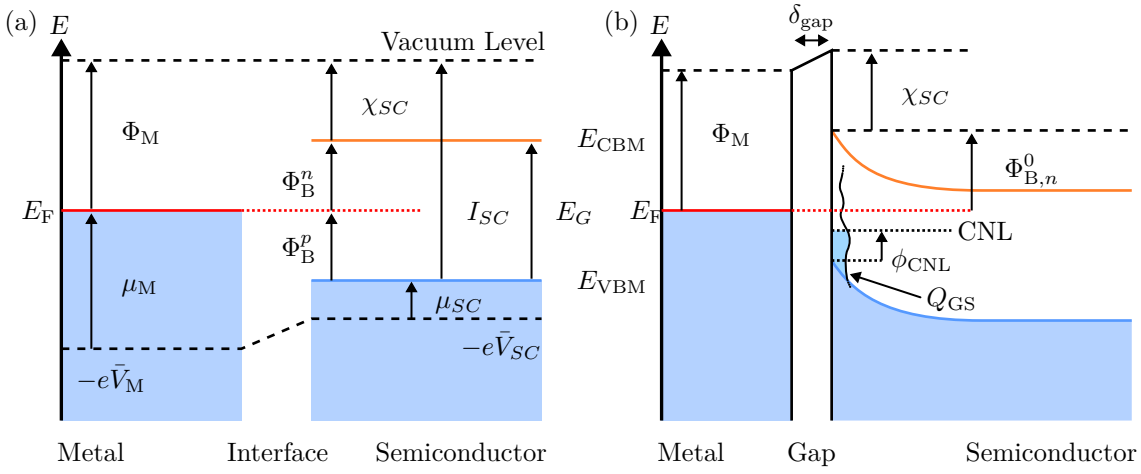


Figure 2.5.: Band diagrams of metal-semiconductor-interfaces. (a) Idealistic model of the Schottky-Mott rule. The electrostatic potential of both metal and SC, $-e\bar{V}$, is displayed as a dashed line. The filled states, up to the Fermi energy E_{F} for the metal and up to the Valence band maximum E_{VBM} for the SC, are shown with blue rectangles. The Schottky barrier height from the Schottky-Mott rule (equation (2.1)) for a n- and p-doped SC are denoted with Φ^n_B and Φ^p_B respectively. (b) The Fermi level pinning model proposed by [Bardeen, 1947]. A thin ($\delta_{\mathrm{gap}} < 2\,\mathrm{nm}$) gap or dielectric layer is assumed. The semiconductor bands are bend at the surface and filled through charge transfer with the metal. Based on equation (2.3), the barrier is given as $\Phi^0_{\mathrm{B},n}$. Adopted from [Tung, 2014].

At the surface, the regular structure of the bulk crystal is broken and the electronic state at the surface is dominated by defects, dangling bonds, and contamination. This

leads to a banding of the bands at the surface and a "natural" doping, introducing additional states inside the band gap of the semiconductor. In equilibrium, one would expect to find an uncharged state and therefore an energy level which ensures the neutrality of both surface and bulk of the crystal must exist.
In the case of a metal-SC interface, this process was first taken into account by [Bardeen, 1947]. The author proposed that upon contact a charge transfer happens between the metal and the surface states, creating an interface dipole. The first analytical model of this was given by the *fixed-separation-model*, which assumes a thin ($< 2\,\mathrm{nm}$) dielectric gap between metal and SC as can be seen in figure 2.5(b) [Cowley and Sze, 1965]. This separating layer ensures that both materials should remain unchanged, as it is expected for the Schottky-Mott rule, while simultaneously allowing a charge exchange from the metal to the SC resulting in these gap states (GS). This lead to a deviation from the original Schottky-Mott rule

$$\Phi^0_{\mathrm{B},n} = S_{\mathrm{GS}}\left(\phi_M - \chi_{\mathrm{SC}}\right) + \left(1 - S_{\mathrm{GS}}\right)\left(E_g - \phi_{\mathrm{CNL}}\right), \tag{2.3}$$

including the charge neutrality level (CNL) ϕ_{CNL} as well as S_{GS}, a theoretical constant depending on the dielectric gap δ_{gap}, density of GS D_{GS}, and the dielectric constant of the gap material $\varepsilon_{\mathrm{int}}$, given by

$$S_{\mathrm{GS}} = \left(1 + \frac{e^2 \delta_{\mathrm{gap}} D_{\mathrm{GS}}}{\varepsilon_{\mathrm{int}}}\right)^{-1}. \tag{2.4}$$

From this it follows, that for a vanishing density of states (DOS) at the semiconductor surface, the Schottky-mott-rule is recovered, while a large DOS reduces the dependence on the metal work function of equation (2.3). Especially at a high density of gap states, the interface Fermi level is expected to be effectively pinned close to the CNL. At a theoretical infinite D_{GS}, the barrier height would become independent of the metal and the Fermi level would be pinned exactly at the CNL. Even though, this can be used to explain linear deviations from the Schottky-Mott rule, the introduction of a dielectric intermediate layer is highly questionable. By now, it is established that under optimal conditions, metals and SC form rather intimate interfaces, without any insulating barriers caused by oxidation or other contamination [Tung, 2014]. Additionally, the electronic structure would not only be dependent on both metal and SC, but also on the dielectric material. Therefore, one would need to take into account the effects of an interface from metal to dielectric as well as from dielectric to SC.

2.2.3. Metal Induced Gap States

A more refined explanation for Fermi-level pinning at metal–semiconductor interfaces is provided by the concept of MIGS. In this model, electron wave functions in the metal decay exponentially into the SC, producing evanescent states within its band gap [Heine, 1965]. These MIGS form an intrinsic set of surface states, largely independent of the specific metal. They become populated due to the metal's proximity and contribute to the overall charge distribution at the interface. Crucially, MIGS generate an interface dipole that screens the semiconductor from the work function difference, effectively decoupling its band alignment from the metal. Like Bardeen's model based on surface states, the MIGS framework introduces a CNL, an energy level around which the Fermi level tends to pin, regardless of the metal's characteristics [Tersoff, 1985, Tersoff, 1984]. Despite their distinct mechanisms, both models ultimately describe how interface states dominate and regulate Schottky barrier formation, leading to equation (2.3).
As the *fixed-separation-model*, the MIGS sufferer from similar shortcomings in terms of the underlying physical reasoning. The MIGS model also relies on the presence of a separating layer in order to introduce states solely caused by the evanescent states of the metal. In a real interface however, distinguishing between electronic states caused by the metal and the SC is not possible [Tung, 2014].
A complete pictures for the formation of the SB can only be given by quantum chemical calculations giving exact information about the interface. The MIGS model can be understood as a phenomenological model describing the underlying mechanism of the interface dipole. However, several of its key assumptions contradict results obtained from *ab initio* calculations, such as the presumed independence of MIGS from the metal species and the notion that the CNL is solely a property of the SC [Dandrea and Duke, 1993, Tung, 2001]. Moreover, for epitaxially grown $NiSi_2$/Si(111) interfaces, density functional theory (DFT) studies have shown that the Fermi-level pinning predicted by the MIGS model does not occur [Das et al., 1989, Fujitani and Asano, 1990].

2.2.4. Inhomogeneous Schottky Barrier

Schottky barrier height (SBH) inhomogeneities are a well-documented phenomenon in metal–semiconductor contacts, as noted by [Palm et al., 1993]. These inhomogeneities arise from local variations at the interface, likely caused by structural

defects such as stacking faults, interfacial impurities, or vacancies. Even in carefully prepared systems, microscopic fluctuations in interface structure or chemistry can significantly alter the local barrier height. As a result, the interface does not exhibit a uniform SBH, but rather a distribution of barrier heights across the contact area. This has important implications for the interpretation of electrical measurements, as the idealized picture of a single, uniform barrier fails to accurately describe real device behavior.

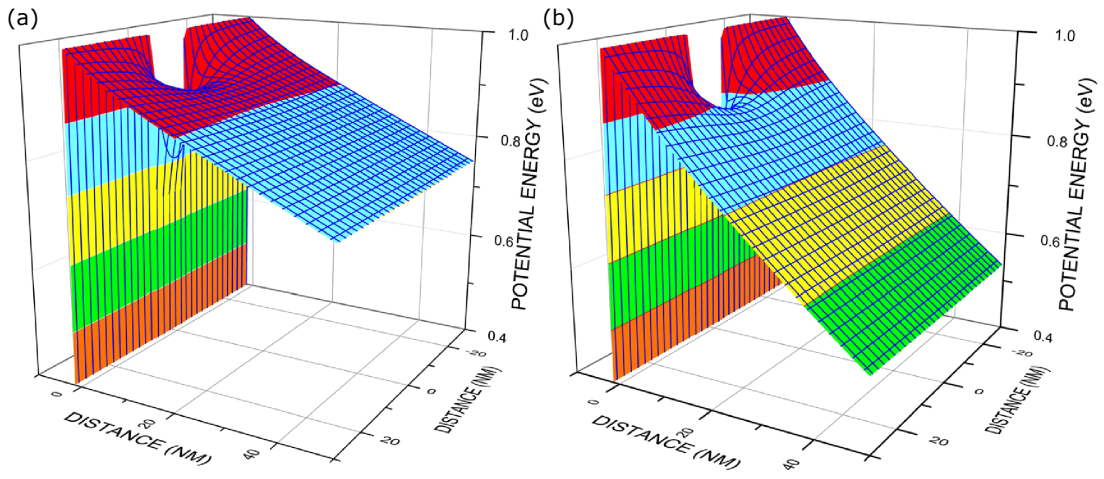


Figure 2.6.: Electrostatic potential distribution near a low SB height patch for (a) a lightly doped SC and (b) a more heavily doped SC. Figure from [Tung, 2014].

The impact of these SBH inhomogeneities becomes particularly evident in current–voltage (I–V) characteristics and is strongly influenced by the doping level of the semiconductor. At low doping levels, local deviations in the SB height affect the overall transport behavior less, as the potential decay on the semiconductor side is slow. However, in heavily doped semiconductors, the drop after the SB is much steeper and locally confined deviations act on regions with further decayed potentials, thereby creating a path with strongly reduced barrier height. This effect is displayed in figure 2.6 where the same pinch-off potential creates a path with a much lower barrier for higher doped SC. This effectively "short-circuits" the high-barrier regions and leads to a percolation effect, which improves the contact's electrical performance. Consequently, high doping in the contact region can mitigate the effects of SBH inhomogeneity and yield more ohmic-like behavior in otherwise rectifying contacts.

2.3. Nanotubes

This section introduces the physics of NTs. Although the primary material system discussed in this work are MoS_2 based NTs, a brief overview of CNTs is given, as these are the most thoroughly researched NT variants, in order to establish a conceptual framework. This will be useful to draw parallels and differences in their properties to the NTs investigated here. This is followed by TMDC based NTs, starting with different synthesis techniques, devoting particular attention to CVT growth, the method used to obtain the MoS_2 NTs examined in this work. Finally, a survey of the established properties of TMDC based NTs as revealed by both experimental studies and theoretical models is given.

2.3.1. Carbon Nanotubes

Since Kroto, Heath, O'Brien, Curl, and Smalley's landmark 1985 identification of C_{60} "buckminsterfullerene" unveiled the first hollow carbon nanostructure [Kroto et al., 1985], attention swiftly turned to tubular graphitic forms. In 1991, Iijima's transmission-electron micrographs confirmed the existence of multi-walled CNT, nested coaxial cylinders of sp^2-bonded carbon with diameters ranging from $\approx$ 1 nm to tens of nanometers and lengths up to microns. The material exhibits exceptional mechanical properties, with an axial Young's modulus of approximately 1 TPa and a tensile strength of up to 100 GPa, as well as electronic properties originating from the π-electron networks spanning the entire NT [Iijima, 1991, Dresselhaus et al., 1996]. Single-walled CNTs, which were later isolated using catalytic chemical vapor deposition, exhibit electronic properties that depend on their diameter and chirality. They can behave as one-dimensional metals or as semiconductors with tunable bandgaps ranging from 0 eV to 2 eV, while showing ballistic electron transport over micrometer length scales at low temperatures [Dresselhaus et al., 1998].

In order to understand their electronic behavior, their geometric structure has to be considered. Starting from a graphene sheet, the NT is "rolled" along the chiral vector $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ with n and m being integer values and a_1 and a_2 being the graphene lattice vectors. This vector connects lattices sides on opposite sites of the graphene sheet, which coincide after rolling it into a tubular structure. Based upon these chiral indices the NTs can be sorted into zig-zag ($m = 0$), armchair ($n = m$),

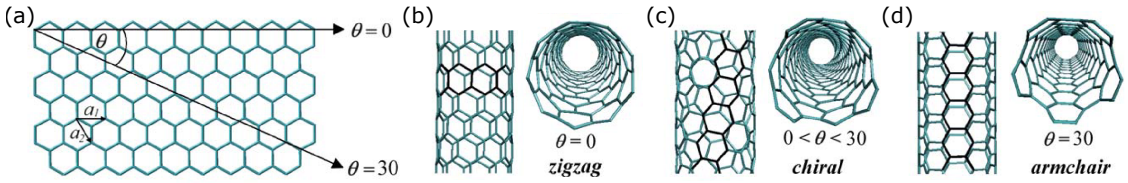


Figure 2.7.: Schematics displaying the wrapping of a graphene sheet into a CNT along the angle wrapping vector defined by the angle θ. (a) Graphene sheet privor to rolling with its units vetcors a_1 and a_2 and the wrapping vectors for $\theta = 0°$ and $\theta = 30°$, (b) (c) and (d) examples of a armchair, chiral, and zigzag NT respectively. Figure from [Galano, 2010].

and chiral ($n \neq m \neq 0$) geometries. Commonly, the chiral angle θ is defined as the angle between $\vec{C}$ and $\vec{a}_1$ (see figure 2.7) [Laird et al., 2015].

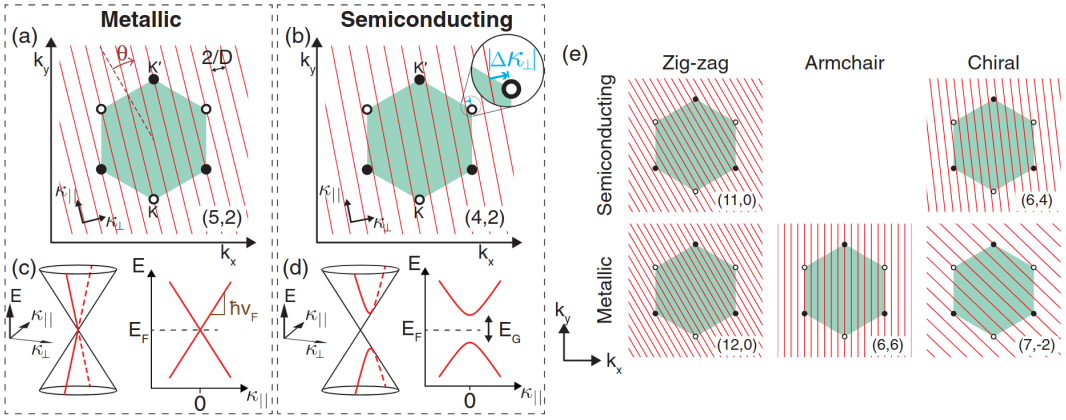


Figure 2.8.: Schematics of the zone-folding-approximation. An exemplary sampling of the k space is shown for a metallic (a) and a semiconducting (b) CNT. The resulting cuts along the Dirac cone and the dispersion relation are shown in (c) and (d) respectively. Further samplings for all three categories of NTs and their type of bandgap are shown in (e). Semiconducting armchair NTs do not exist. Adapted from [Laird et al., 2015].

The chiral vector does not only categorize the resulting NTs geometries, but also dictates the emerging one-dimensional band structure. In the zone-folding approximation [Saito et al., 1992, Hamada et al., 1992], one enforces the periodic boundary condition for the electron wavevector $\vec{k}$

$$\vec{k} \cdot \vec{C} = 2\pi p, \quad p \in \mathbb{Z}, \tag{2.5}$$

which fixes the component of the wavevector around the NT circumference to

$$k_C = \frac{2\pi p}{D}, \tag{2.6}$$

where D is the nanotube diameter. This quantization selects a discrete set of parallel "cutting lines" through the two-dimensional graphene Brillouin zone, yielding a family of one-dimensional subbands. The resulting dispersion relation of the nanotube is therefore obtained by slicing the graphene $E(\vec{k})$ surface along these quantization lines, and the subband whose cutting line lies closest to the original Fermi energy E_F governs the low-energy transport properties. Based on this, the NTs can be either be metallic or semiconducting depending if the quantization line cuts exactly through the Dirac point (metallic) or not (semiconductor). This is shown in figure 2.8.

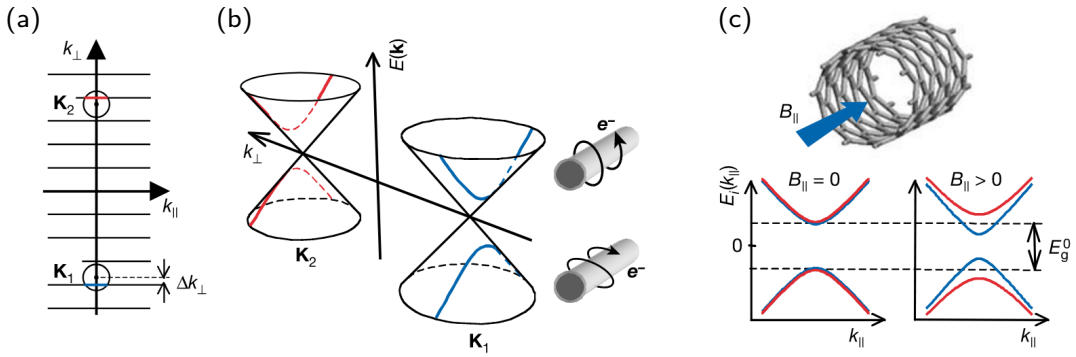


Figure 2.9.: Schematic showing the effect of a magnetic field on the energy levels of a CNT. (a) Sampling of the electronic band structure inside the NT along the orthogonal k-direction caused by the NT wrapping. (b) Schematic of the k-cones with the blue and red line marking the band structure of the NT as well as schematics associating the upper branch with anticlockwise and the lower with clockwise angular movement around the NT. (c) A magnetic field along the NT axis causes a splitting of the previously degenerate levels with the same angular moment. Adapted from [Minot et al., 2004].

Based upon the zone-fold-approximation two different response to a parallel magnetic field can be expected, depending on the type of CNT. Figure 2.9(a,b) show again, how the wrapping causes an effective cut through the Dirac cone. Generally, in the absence of a magnetic field, two degenerate bands for the K and the K' point (K_1 and K_2 in the figure) are generated. As the sketch in (b) shows, these bands correspond to electrons (and holes) moving in either clockwise or anticlockwise direction along the NT. If these cuts do not align with the Dirac point this results

in a semiconducting CNT. If a magnetic field is applied along the NT axis, the flux enclosed by the wavefunction around the nanotube causes an additional phase that has to be considered in equation (2.5). This leads to a shift of the cuts in the k-space based on the motion of the electron. This effectively "moves" the band up or down the Dirac cone, causing an energy splitting between clockwise and anticlockwise states. In the case of a metallic CNT, both K and K' would cut through the Dirac point. Then the energy shift for both valleys in either positive or negative direction would be the same, as the cone is symmetric around the Dirac point. Despite the opening of a gap between the electron and the hole band, the K and K' bands would therefore still remain degenerate [Minot et al., 2004].

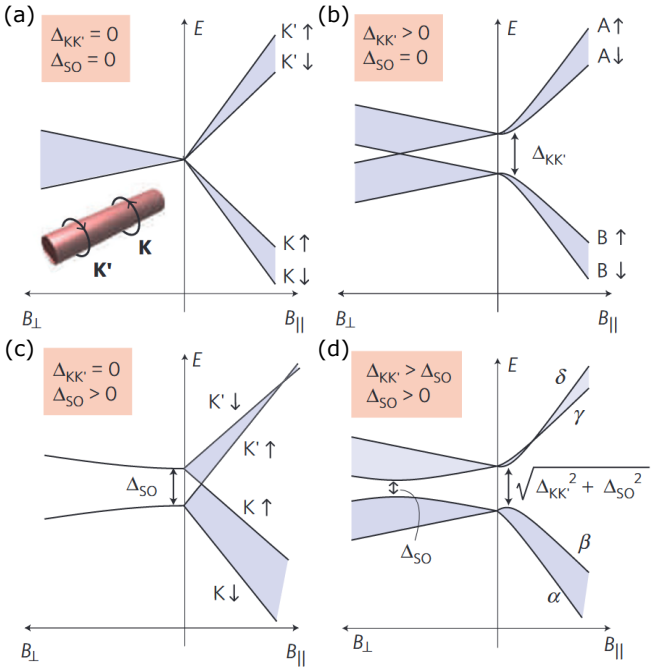


Figure 2.10: Effect of spin–orbit coupling (Δ_{SO}) and disorder-induced valley mixing ($\Delta_{KK'}$) on the energy spectrum of a CNT. Shown are calculated single-particle spectra of a conduction band quartet as a function of magnetic field applied perpendicular ($B_\perp$) and parallel ($B_\parallel$) to the CNT axis. The panels correspond to the limiting cases: (a) neither effect, (b) valley mixing only, (c) SOC only, and (d) both combined, with $\Delta_{KK'} > \Delta_{SO} > 0$. Reproduced from [Jespersen et al., 2011].

This can be further expanded by including SOC and disorder caused intervalley mixing $\Delta_{KK'}$. Due to the much smaller SOC in CNTs of $\Delta_{SO} \approx 0.3\,\text{meV}$ compared to TMDC materials (see table 2.1), there effect was masked by disorder and electron-electron interaction in multi-electron systems. However, [Kuemmeth et al., 2008] were able to directly measure Δ_{SO} in an ultraclean CNT with single electron and hole states. The effect of the magnetic field response for different combinations of Δ_{SO} and $\Delta_{KK'}$ can be seen in figure 2.10. Without both, a parallel field leads to splitting of both the bands and spin states, as can be seen in figure 2.9. For perpendicular fields only a splitting with a much smaller magnetic moment is observed, as the large effect in parallel direction is caused by motion around the NT [Minot et al., 2004].

Both finite SOC and intervalley mixing cause a splitting already without a magnetic field, but the Δ_{SO} splits states with different spin (c), whereas $\Delta_{KK'}$ causes an avoided crossing (b). In the case of larger intervalley mixing then SOC (d), the overall picture is similar to a purely $\Delta_{KK'} > 0$ picture, but the effect of the SOC causes an anti-crossing for perpendicular field with a splitting corresponding to Δ_{SO} [Jespersen et al., 2011].

Owing to their one-dimensional nature, CNTs have immediately gained interest as a platform for QDs. It is unsurprising that only six years after their discovery, the first measurements of a single electron transistor (SET) inside a CNT were published [Bockrath et al., 1997, Tans et al., 1997].

2.3.2. TMDC Based Nanotubes

The first synthesis of TMDC-based NTs was reported only a year after the seminal discovery of CNTs by [Iijima, 1991]. In 1992, [Tenne et al., 1992] demonstrated the formation of cylindrical WS_2 nanostructures, marking the beginning of research into inorganic fullerene-like compounds and layered NTs [Tenne et al., 1992]. This was soon followed by the successful fabrication of MoS_2 NTs by [Feldman et al., 1995]. Over the following years, the family of TMDC NTs was expanded to include compounds such as NbS_2 [Nath and Rao, 2001], HfS_2, TiS_2, TaS_2, and $NbSe_2$ [Nath and Rao, 2002], demonstrating the generalizability of the tubular morphology to a variety of layered TMDCs. A comprehensive overview of synthesis strategies for all types of NTs is provided in [Rao and Govindaraj, 2009].

Overview of Nanotube Growth Techniques

Several synthesis routes have been developed for TMDC based NTs, each leveraging different mechanisms of tubular formation.

Early approaches involved the sulfidation of transition-metal precursors. In one of the first demonstrations, thin tungsten or molybdenum films were annealed in a flowing H_2S atmosphere, leading to the spontaneous formation of nested, fullerene-like WS_2 particles and NTs [Tenne et al., 1992]. A related gas-phase reaction between molybdenum oxide and hydrogen sulfide similarly produced multi-walled MoS_2 NTs [Feldman et al., 1995].

Subsequent methods employed solid precursors with predefined morphologies. Sulfidation of MoSI nanowires, for example, yields MoS_2 NTs with narrow diameter and

wall-thickness distributions, although often accompanied by structural disorder and fullerene-like cores [Remškar et al., 2007, Remškar et al., 2010, Viršek et al., 2010, Strojnik et al., 2014]. Comparable conversion strategies include the selenization of WOx nanowires in hydrogen-containing atmospheres, resulting in consistently small-diameter WSe_2 NTs [Yomogida et al., 2020].

Solar ablation, employing concentrated sunlight, provides a photothermal route for the synthesis of MoS_2 nanostructures [Gordon et al., 2008]. The extreme temperature and radiation gradients generated during ablation induce localized vaporization and recondensation, yielding fullerene-like particles and multi-walled MoS_2 NTs with 20–25 layers and lengths up to 2 µm. In some cases, single-walled NTs with diameters close to the theoretical limit were obtained.

Vapor-phase synthesis has also been explored in several variants. Conventional chemical vapor deposition (CVD), mainly used for planar MoS_2 layers [Lee et al., 2012, Abdel Maksoud et al., 2021], has been adapted to produce MoS_2/MoO_2 core–shell nanowires and NTs under turbulent flow conditions [Goto et al., 2022]. Catalyst-assisted CVD employing FeO nanoparticles further enables the formation of hollow NTs and nanowires with rectangular cross-sections and armchair-like growth orientations [Weng et al., 2018, Mengting et al., 2017].

The vapor–gas–solid (VGS) method has proven effective for growing high-purity, crystalline WS_2 and MoS_2 NTs within a fluidized-bed reactor [Rothschild et al., 2000, Zak et al., 2009, Zak et al., 2010]. For WS_2, thin-walled NTs can be obtained by reacting volatile molybdenum suboxide species with sulfur–iodine vapor, where iodine enhances material transport and promotes tubular morphologies without templates [Chithaiah et al., 2020]. However, the authors report that a fluidized-bed configuration was less effective for MoS_2. Instead, a horizontal reactor with a porous-quartz reaction cell yielded superior results.

Finally, iodine-assisted CVT has emerged as a route to structurally pristine MoS_2 NTs with remarkable uniformity and crystallinity [Remškar et al., 1996, Remškar et al., 1998, Remškar, 2004]. Since this method was used for the fabrication of the NTs analyzed in this thesis, an in-depth description is provided in the following section. A broader overview of inorganic nanotube synthesis techniques can be found in the comprehensive reviews by [Rao and Govindaraj, 2009] and [Yadgarov and Tenne, 2024].

Iodine-assisted Chemical Vapor Transport

In the first step, the MoS_2 powder is produced by an 75 h annealing process, where pure molybdenum is mixed with sulfur and placed in a silica ampoule. This is then followed by the actual iodine-assisted CVT process, where the amorphous MoS_2 powder and elemental iodine I_2 are loaded into a quartz glass ampoule, which is subsequently evacuated to $10 \cdot 10^{-5}$ mbar and sealed by melting the quartz. The sealed ampoule for the CVT process is then mounted into a tube furnace. There a temperature gradient is established, with the hot end (containing the MoS_2 precursor) heated to $T = 860\,°C$ and the cooler recrystallization zone to $T = 736\,°C$ (see figure 2.11 (a)).

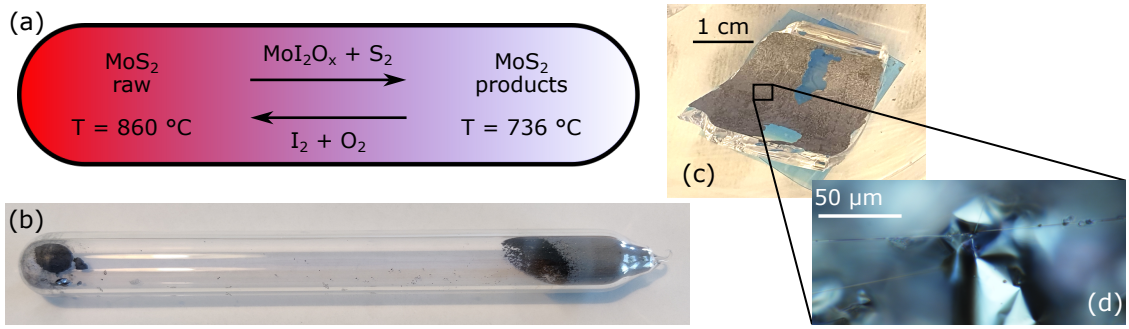


Figure 2.11.: MoS_2 NT growth process and resulting products. (a) Schematics of the growth conditions inside the ampoule. (b) Optical image of an ampoule after a finished growth process. (c) Part of the product side of an ampoule with MoS_2 material. (d) Micrograph of the grown MoS_2 material with large flakes and several NTs on top of the flakes.

At the hot end, residual oxygen O_2 liberated from the ampoule walls participates in the reaction:

$$MoS_2 + I_2 + O_2 \longrightarrow MoI_2O_X + S_2$$

The volatile species MoI_2O_X and S_2 diffuse along the temperature gradient and undergo reverse deposition in the cooler zone:

$$MoI_2O_X + S_2 \longrightarrow MoS_2 + I_2 + O_2$$

This cyclic transport continues as long as the temperature gradient (ΔT) and feedstock are maintained, typically for 500 h. These long durations together with the

specifically optimized temperatures ensure a slow growth resulting in high quality MoS_2 NTs with a very low defect density [Remškar, 2004].

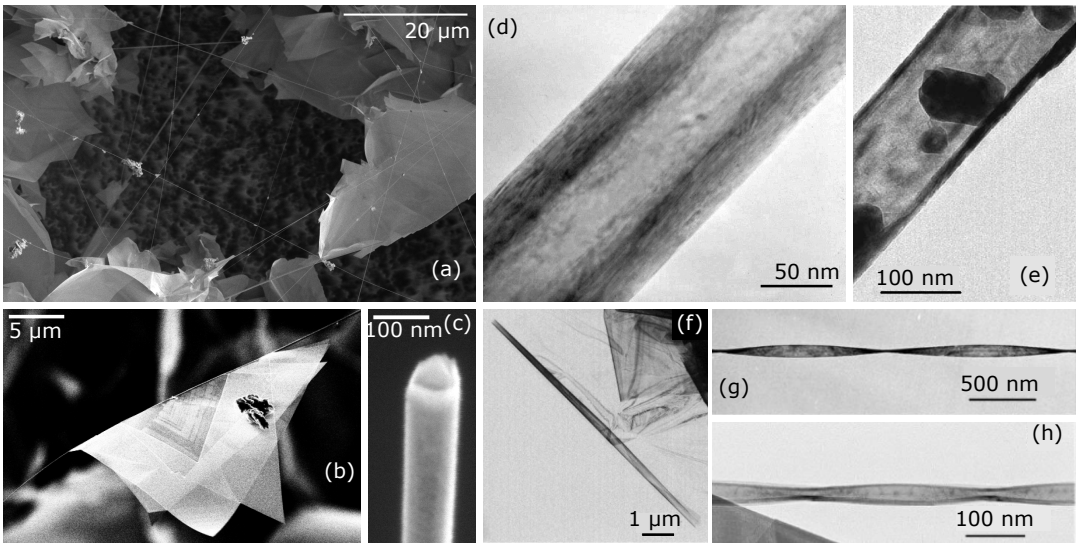


Figure 2.12.: Scanning electron microscopy (SEM) (a to c) and transmission electron microscopy (TEM) (d to h) images of different types of MoS_2 growth products. (a) Network of NTs on top of a variety of flake and bulk crystals. (b) 2D flake "hanging" over a NT. (c) Close up image of a NT end, showing a hollow core. (d) TEM scan over a NT with a diameter of 118 nm and a wall thickness of about 32 nm. (e) Fullerene-like nanoparticles in a so called "mamatube". (f) 2D flake rolling up into a NT. (g) Spiraling ribbon with a width of about 88 nm. (h) A "breathing" NT. Figure (c) adapted from [Reinhardt et al., 2019], (d) from [Schock et al., 2023], (e) from [Remškar et al., 2009], and (f) to (h) from [Remškar et al., 2022].

Upon completion, the furnace is allowed to cool slowly to ambient temperature before mechanically fracturing the ampoule to recover the deposits. On the growth side of the ampoule (figure 2.11(c)), a wide variety of MoS_2 products can be found, ranging from bulk crystals and multilayer to single-layer flakes, to more complex macromolecular structures such as NTs. The NTs originate from microfolds in bent flakes or thin crystals, which start to roll up [Remškar et al., 1998]. In figure 2.12, various examples of products are shown. It can be seen that on top of the first layer of flakes and crystals, a network of NTs forms, which indeed originate from the 2D products (see (a)). A reverse process also appears possible, where a flake forms on a NT (b).

Raman measurements confirm the MoS_2 nature of the material, see figure 2.13. For bulk MoS_2 two main Raman peaks are expected, the in-plane E^1_{2g} phonon mode near

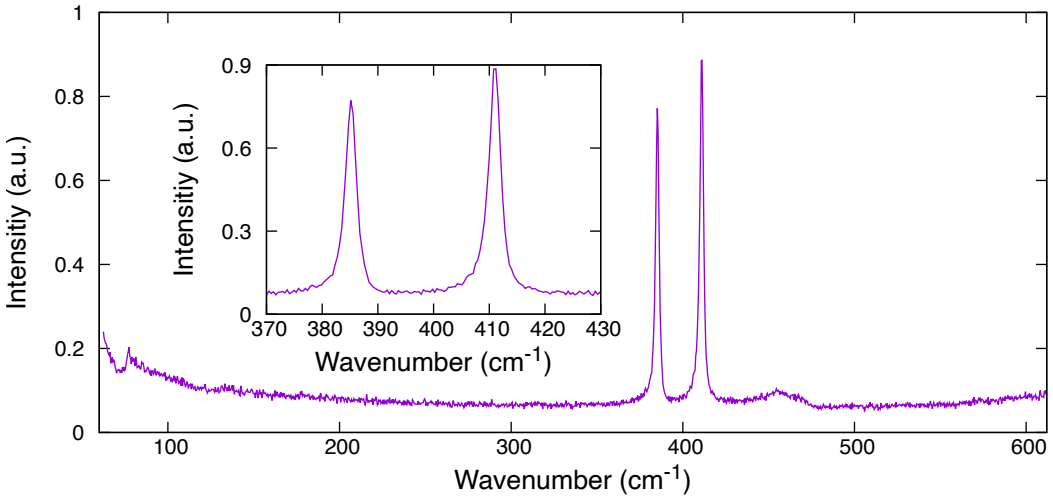


Figure 2.13.: Raman measurement of the material on the growth side of the ampoule. The inset shows the two characteristic peaks of MoS_2. This confirms that the material used here is indeed MoS_2. Measuremed in cooperation with Philipp Parzefall.

382 cm^{-1} and the out-of-plane A_{1g} mode close to 406 cm^{-1} [Lee et al., 2010]. As the peaks positions here are close to the reported, the material is confirmed to be MoS_2.

Collapsed Nanotubes as Nanoribbons

Taking an even closer look at the generated structures, the NTs are indeed hollow (figure 2.12(c)) and multi-walled (d). In (f) a NT originating form a 2D flake can be seen, giving evidence that the bending seams to lead to the NT growth. It was found that the growth of these tubular structures can continue until either the process is stopped (leaving an open end as seen in (c)) or until they reach an obstacle. This can results in NTs with lengths up to hundred of micrometers.

At obstacles, the growth can either terminate or the NT can "collapse" into a nanoribbon (NR) in order to avoid high strain from a bending "out of the way" of the obstacle [Remškar, 2025]. When collapsed, such a NT is no longer hollow, but forms a closed "pancake"-like stack of layers. TEM images of their cross-section (see figure 2.14) reveal their internal structure, with each layer consisting of a straight section and highly bent but still connected edges (see (b)). Due to their chiral structure, the ribbons tend to be helically twisted along their axis (see figure 2.12(g,h)).

Another type of nanostructure that can be found are the so called “mamatubes” (see figure 2.12(e)). With TEM images it was possible to detect nanoparticles grown inside a NT [Remškar et al., 2009]. However, these products seem to be predominantly generated through the template guided growth with $Mo_6S_2I_8$ nanowires mentioned above and only appear at a very specific temperature range.

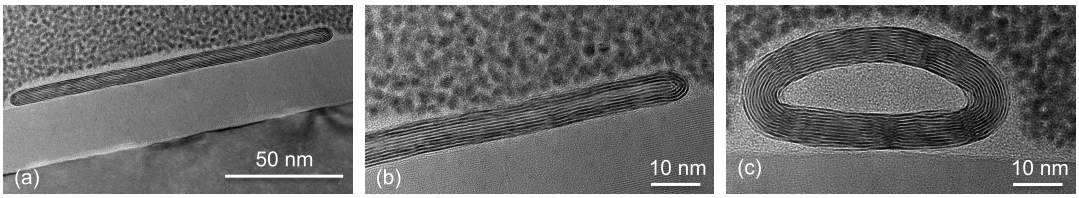


Figure 2.14.: TEM images of a nanoribbon (a, b) and a nanotube (c). Images were taken from [Fathipour et al., 2015]

As NRs actually constitute collapse NTs, from here on onward NTs will be used to refer to both, except when explicitly distinguishing between a specific nanotube or nanoribbon.

Mechanic and Electronic Properties

A very basic question about the structure of TMDC based NTs arises from the direct comparison to CNT: What is the impact of the “extended” thickness of the additional chalcogenide layers? As graphene is completely planar, bending a sheet into a NT causes only a very limited amount of strain and therefore NTs with diameters down to 0.4 nm have been observed [Peng et al., 2000]. In MoS_2 and similar materials, the additional sulfur layers are squeezed inside and stretched outside of the NT, which renders small diameters unstable. [Seifert et al., 2002] analytically found that MoS_2 or WS_2 strips of a width of $\pi \times 6.2$ nm with open ends are energetically more favorable then a single wall NT of diameter of 6.2 nm.
Despite this prediction, [Xiang et al., 2020] managed to fabricate single wall CNT, hBN, and MoS_2 nanotube heterostructures, with the MoS_2 NT diameters down to 3.9 nm [Xiang et al., 2020]. However, as these structures do not represent single wall nanotube (SWNT) of MoS_2 solely, a stabilizing effect from the inner NT is possible. In accordance, the authors only observed MoS_2 NTs on precursor NTs with diameters larger than > 3 nm. Another example of SWNT that reached below that limit were sub nanometer NTs reported by [Remškar et al., 2001], where they found self-assembled bundles with interstitial iodine with lengths up to hundreds of

micrometers when C_{60} was used as catalyst. However, the grouping and interstitial I seem to stabilize these exotic NTs.

In multilayer NTs, a winding of an MoS_2 layer with a thickness of $d = 0.6147\,\text{nm}$ causes a increased circumference of $\pi \times d$. Therefore, the next layer cannot be of the same chirality as underlying one, as $\pi \times d$ is not a multiple of the in-plane lattice parameter of MoS_2. In very thick-walled NTs this and the strain can lead to a reduced interlayer distance even below the value of planar MoS_2 [Remškar, 2004].

Similar to CNTs, NTs based on TMDCs exhibit exceptional mechanical properties. WS_2 NTs possess a Young's modulus of approximately 171 GPa, while MoS_2 NTs are predicted to be not only around 40 % lighter but also mechanically stronger, with a modulus reaching up to 238 GPa [Kaplan-Ashiri et al., 2004]. The interlayer spacing in both compounds is observed to be about 3 % larger compared to their planar bulk forms [Remškar et al., 1996]. Moreover, MoS_2 NTs appear to form exclusively in right-handed chiralities [Margulis et al., 1996].

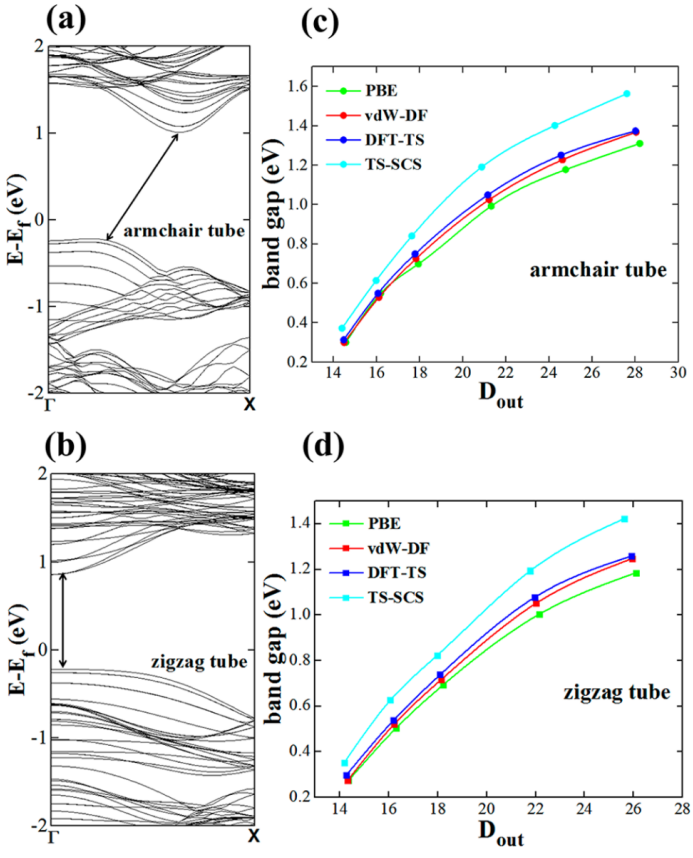


Figure 2.15: Calculated band structure of a single wall MoS_2 armchair (a) and zigzag (b) NT, with the direct/indirect energy gap marked with an arrow. In (c) and (d) the band gap size over the outer NT diameter given in nm for both chiralities are given as the result of different simulation methods. Figure adapted from [Li and Zhu, 2015].

While the *zone-folding-approximation* was proven to give reliable estimations of the bandstructure in CNTs, it only seems to be of a very limited use for TMDC based

NTs. This is obvious, if the major difference to their carbon counterpart is considered, namely the absence of a metalic configuration: in the case of a semiconducting TMDC a "cut" through the K-points can only result in a band gap of at least the same size as the flat material. In contrast, along an increase in strain energy, [Seifert et al., 2000] found that the band gap reduces with decreasing diameter staying well below the value of a bulk and monolayer MoS_2 for all considered radii (see figure 2.15(c) and (d)). They also found that the smallest armchair NTs can become metallic with a direct gap, whereas zigzag NTs always exhibit a non-zero indirect gap ((a) and (b)). The semiconducting nature of almost all NTs as well as the direct and indirect band gap of armchair and zigzag respectively was confirmed by further theoretical calculations [Ansari et al., 2015, Xiao et al., 2014, Milosevic et al., 2007, Li and Zhu, 2015].

[Ansari et al., 2015] also found that the effective mass of the carriers is dependent on both the chirality and the radius of the NT. While they calculated the effective electron mass to stay within a reasonable limit between that of planar MoS_2 and m_e, they found that m_{eff} of the holes increases for both zigzag and armchair NTs with the radius, reaching values as large as $m_{eff} = 5.8m_e$. Similar results for the effective carrier masses were found by [Yin et al., 2016].

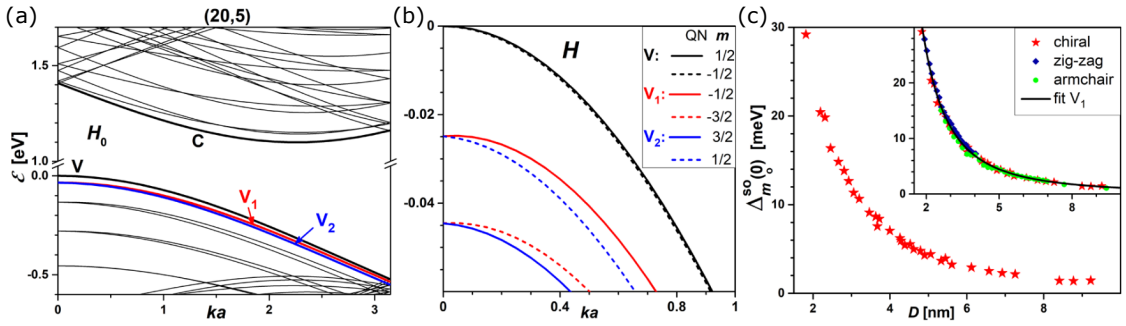


Figure 2.16.: Electronic properties of chiral NTs. (a) Band structure of a chiral (20, 5) NT. The lowest conduction band is marked with **C** and the highest valence band with **V**. The first spin split valence band and the split bands are marked with $\mathbf{V_1}$ and $\mathbf{V_2}$. (b) Spin-split valence bands near the VBM after inclusion of spin–orbit coupling ($H = H_0 + H_{SO}$); solid and dashed lines indicate spin up and down, respectively. (d) Spin splitting of the valence band $\mathbf{V_1}$ as a function of the NT diameter. The inset shows the splitting for all considered chiralities. Figure adapted from [Milivojević et al., 2020].

[Milivojević et al., 2020] were the first to systematically investigate the electronic band structure of chiral MoS_2 NTs, with a particular focus on SOC effects using

symmetry-based methods. They found that the band gap in chiral NTs can alternate between direct and indirect depending on the chiral angle and diameter. In contrast to armchair and zigzag NTs, where spin splitting is symmetry-forbidden due to the presence of a horizontal mirror plane and time-reversal symmetry respectively, chiral NTs lack such mirror symmetries, allowing SOC-induced spin splitting of all bands except at time-reversal invariant momenta (see figure 2.16(a)). The resulting spin polarization is constrained to lie along the NT axis due nontrivial rotational symmetry. The authors focus primarily on the valence band, where the spin splitting is found to be finite but generally smaller than in the monolayer and reduces with NT diameter (figure 2.16(c) inset). For conduction band states, the magnitude (generally below 9 meV at the CBM) and the presence of spin splitting vary irregularly with NT geometry, which is attributed to the switching between direct and indirect band gap character as a function of chirality. Furthermore, external symmetry-breaking fields can activate spin splitting in otherwise forbidden cases: a magnetic field along the NT axis removes the vertical mirror symmetry in zigzag NTs, while an electric field—particularly one applied perpendicular to the axis—breaks rotational symmetry and induces Rashba-type SOC [Milivojević et al., 2020].

Concerning defects, [Li and Zhu, 2015] simulated vacancies in an armchair NT and analyzed the resulting DOS (see figure 2.17). They found that all type of vacancies considered (Mo, S, S_2, and MoS_2) create in-gap states without a strong shift of the Fermi energy. Especially sulfur vacancies predominantly create states below the conduction band, with smaller gap remaining above the VBM. Additionally, these type of vacancies do no exhibit any spin moments, whereas both the Mo and the MoS_2 vacancies have an Landé g factor of 0.6 and 2 respectively.

To date, theoretical investigations have predominantly focused on SWNTs, as the large unit cells required for DFT calculations render simulations of multilayer systems computationally demanding. Only a single study has explored the band structure of multilayer TMDC NTs [Vadseth et al., 2024]. By comparing different combinations of chiral indices for inner and outer NTs, the authors identified metastable configurations (see figure 2.18) for all examined TMDC materials, with interlayer distances generally exceeding those of their planar counterparts. Similar to SWNTs, the band gap of the inner (and therefore thinner) NT was found to be significantly reduced. For certain chiralities and sufficiently narrow inter-shell separations, the system can even become metallic, depending on the outer NT's diameter. This behavior is attributed to radial compression, or *squeezing*, exerted by the outer shell.

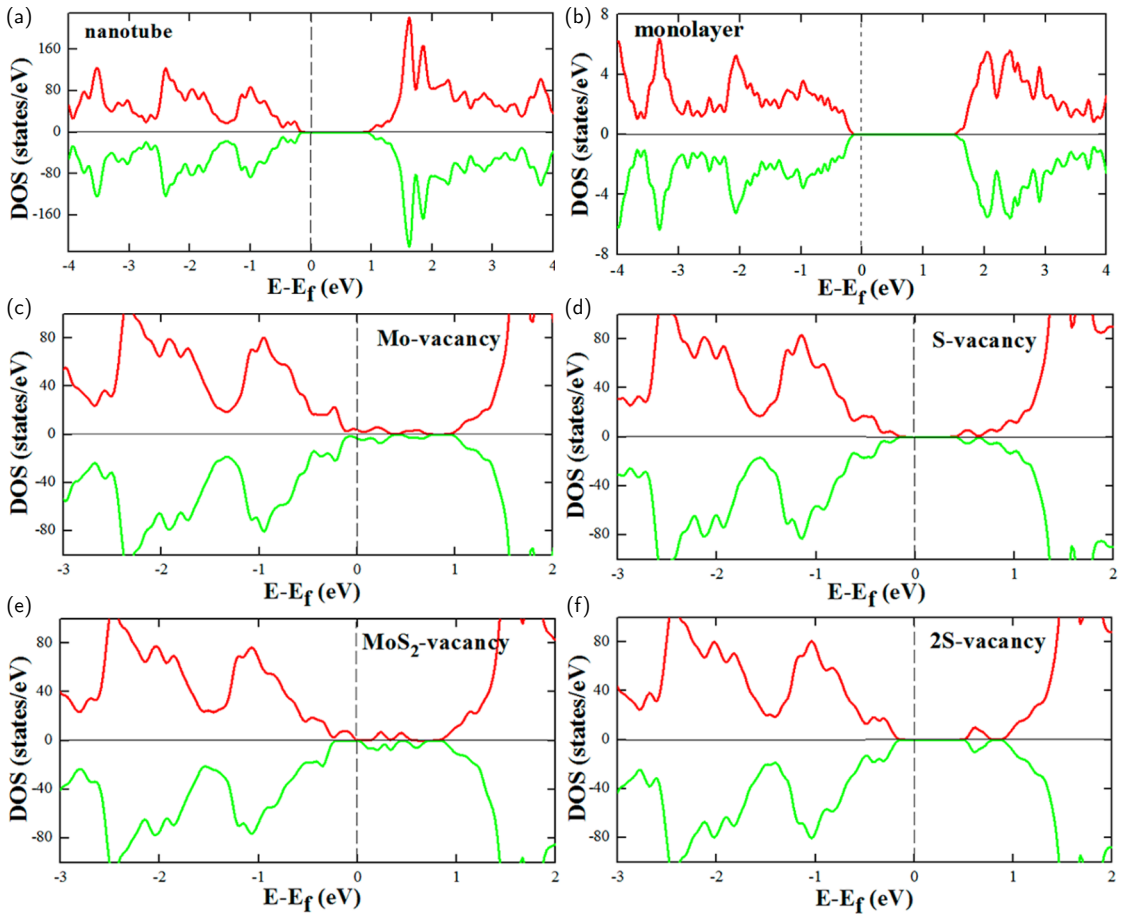


Figure 2.17.: Effect of vacancies on the DOS of an armchair MoS_2 NTs with a diameter of 24.6 Å. (a) DOS of a pristine NT and (b) DOS of similar monolayer. Different types of vacancies and the resulting DOS with (c) a Mo-vacancy, (d) a S-vacancy, (e) a MoS_2-vacancy and (f) a S_2 vacancy. Adapted from [Li and Zhu, 2015].

However, a zero band gap in the inner NT was observed only for $MoTe_2$ and WTe_2 in their most stable configurations (indicated by crosses in the figure). While the band gap of the outer shell can also be reduced, the energetically most favorable configurations generally retain a gap close to that of a SWNT of the same chirality and diameter.

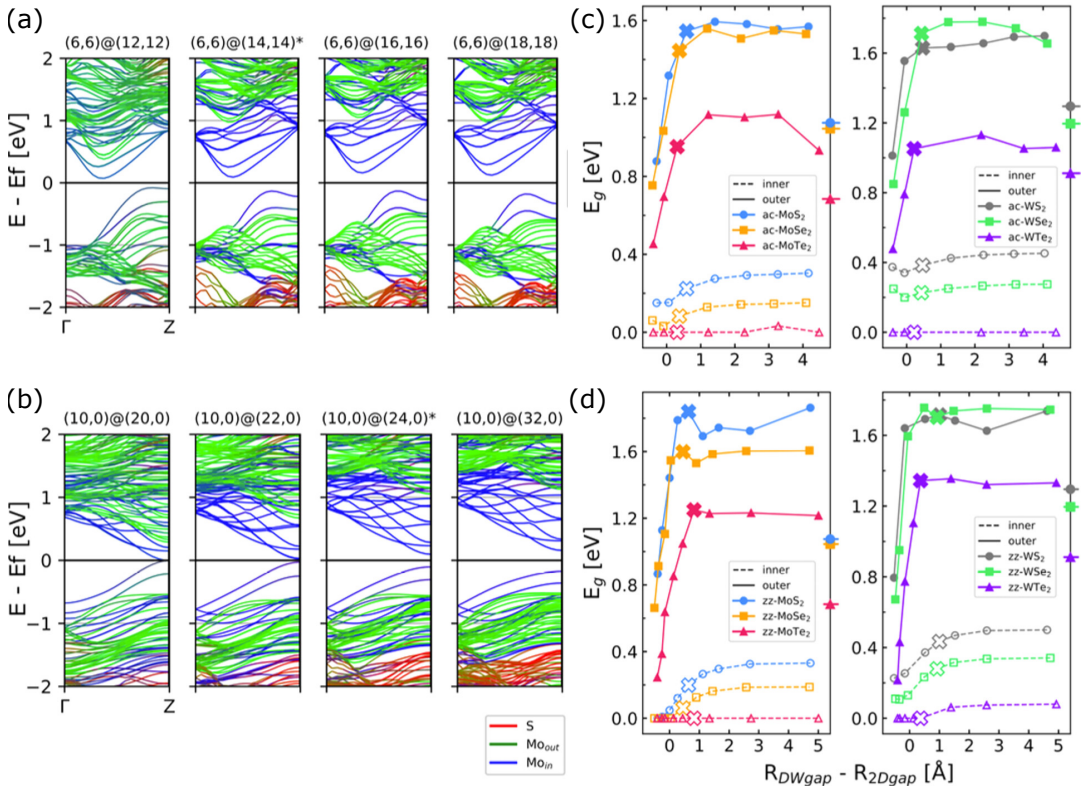


Figure 2.18.: Simulations of TMDC double-wall NTs. Band diagrams of MoS_2 NTs with different inner and outer chiral indices (a) inner index (6,6) and (b) inner index (10,0). Band gap of (c) armchair and (d) zigzag NTs as a function of inter-wall distance R_{DWgap} compared to the 2D interlayer distance $R_{\mathrm{2D\,gap}}$. Adapted from [Vadseth et al., 2024].

Rectangular NTs have been observed experimentally [Weng et al., 2018] as well as simulated [Zhang et al., 2021b]. They were predicted to be energetically favorable to the cylindrical counterpart for diameters below 3 nm due to the reduced strain of the four "unbent" sides. This geometry is mitigated by a uniquely five-coordinated Mo atom at each corner. However, surface energy is nearly constant owing to the high energy corner sides as opposed to the drastically decreasing surface energy with the diameter of cylindrical NTs. Despite these findings, the experimentally observed

rectangular NTs exhibited diameters in the range of tens of µm. They attribute this to the existence of a template formed by the catalyst [Hong et al., 2017].

2.4. Quantum Dots

The following chapter will be dedicated to the theory of electronic transport through QDs. First the mechanism of CB and the "classical" model of a SET will be discussed. The effects of disordered multi-QD systems are also considered. Subsequently, the transition from the quasi classical to a more quantum-mechanical description is examined. Finally, the influence of an external magnetic field on the energy spectrum within such systems is discussed.

More in depth introductions to both the classical and a quantum mechanical descriptions can be found in [Kouwenhoven et al., 2001], [Hüttel et al., 2005], and [Nazarov and Blanter, 2009].

2.4.1. Coulomb Blockade

A QD is a system in which electrons (or other charge carriers) are confined in all three spatial dimensions. The QDs considered here are formed in SC or metals and are therefore based on the underlying bulk crystal. This crystal consists not only of the confined conduction-band electrons but also of tightly bound core electrons and positively charged nuclei. According to Bloch's theorem, these charged constituents contribute only through a periodic potential, whose effect is already encoded in the electronic band structure. Hence, only the *accessible* electrons in the partially filled bands near the Fermi level are relevant for the QD. The crystal lattice itself enters only through material parameters such as the effective mass, dielectric constant, and g-factor. Inside the QD, a fixed number of electrons N resides, which, in a "classical" picture, interact only via Coulomb repulsion.

To add an additional electron to a QD, the Coulomb repulsion exerted by the electrons already residing on the QD must be overcome. In the classical picture of a metallic island, the total electrostatic energy associated with N excess electrons is expressed as

$$E(N) = \frac{Q^2}{2C} = \frac{(Ne)^2}{2C} = E_\mathrm{C} N^2, \tag{2.7}$$

where C is the total capacitance of the island, $Q = Ne$ is the total charge, and $E_\mathrm{C} = e^2/(2C)$ is the charging energy scale. The energy cost of adding one additional electron to a QD containing N electrons is then

$$\Delta E = E(N+1) - E(N) = E_C(2N+1). \tag{2.8}$$

This quantized addition energy reflects the discrete nature of charge on the dot and is the origin of the CB phenomenon [Kulik and Shekhter, 1975, Averin and Likharev, 1986]. In addition to the electrostatic cost E_C, quantum mechanics imposes that each electron as a fermion must occupy a distinct level, separated by the level spacing δ_S (apart from degeneracies). In general, quantum confinement leads to discrete energy levels whose spacing decreases as the spatial extent of the confining potential increases. Therefore, if large QDs with many electrons ($\delta_S \ll E_C$) are considered, the quantum mechanical contribution to the energy cost of adding an electron can be ignored. However, in small semiconducting QDs with a small number of electrons in the conduction band, this does not hold any longer, which will be discussed later.

Now a realistic device geometry in which the QD is coupled to source and drain electrodes via tunnel barriers and capacitively coupled to a back-gate voltage V_G, as illustrated schematically in figure 2.19(a) is considered. Neglecting quantum confinement effects, the QD can be approximated as a metallic island characterized by a total capacitance C_Σ, giving a charging energy

$$E(N) = \frac{1}{2C_\Sigma}(Ne - C_G V_G)^2, \tag{2.9}$$

with the total capacitance $C_\Sigma = C_G + C_D + C_S + C_{rest}$. Here $C_{G,D,S,rest}$ denote the capacitances between the QD and the gate, drain, source, and any additional surrounding electrodes, respectively. The ratio between the gate and total capacitance, often referred to as the *gate lever arm*,

$$\alpha_G = \frac{C_G}{C_\Sigma}, \tag{2.10}$$

quantifies how effectively the gate couples to the QD.

When the source–drain bias voltage is small $V_{SD} \approxeq 0\,\mathrm{V}$ (therefore $eV_{SD} \ll k_B T_e, \hbar\Gamma$, with Γ being the tunneling rate to the QD), and the electron temperature T_e inside the leads is smaller then the charging energy

$$k_B T_e \ll E_C \tag{2.11}$$

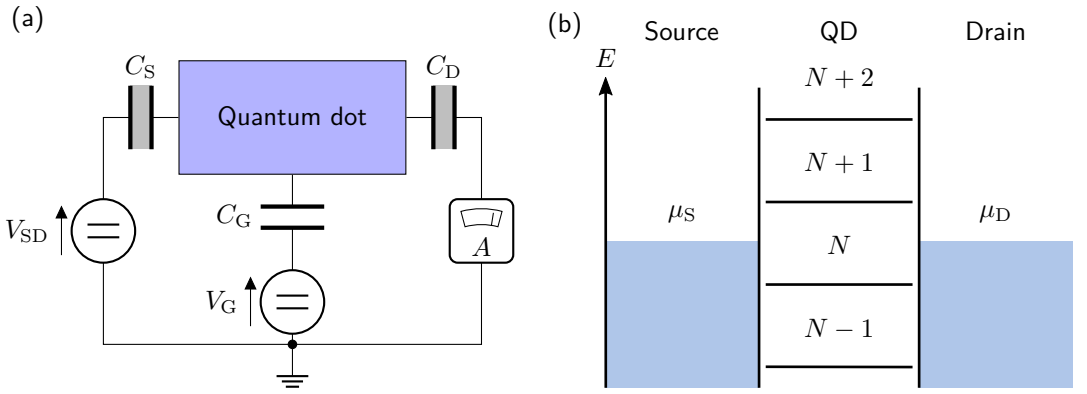


Figure 2.19.: Schematics of a QD contacted through two tunnel barriers C_S and C_D to source and drain (a). The charge on the QD is controlled via the voltage V_G applied at the capacitance C_G. In (b) the energy diagram is depicted. The blue rectangles mark the electron states filled up to the Fermi energy in the leads (μ_S and μ_D). Inside the QD, the black lines mark the chemical potential where two states with e.g. N and $N+1$ electrons have the same energy.

current can only flow through the QD if the charge can fluctuate between N and $N+1$ electrons. This is only possible, if the energy difference of both states, which can defined as the chemical potential μ_{QD} of the QD, is equal to the chemical potential of the leads μ_S and μ_D (figure 2.19)

$$E(N+1) - E(N) \equiv \mu_{QD} = \mu_S = \mu_D. \tag{2.12}$$

As the energy in the QD can be controlled through the gate voltage (equation (2.9)), it can be tuned to match this condition. Then one electron can tunnel from the source side into the QD and then find a empty energy level at μ_D to tunnel out of the QD on the drain side. This characteristic transport of single electrons gives these systems the name SET.

As the gate voltage is changed, the electrochemical potential of the QD is shifted relative to the leads. Each time the system reaches a point where the difference in energy of two charge states, e. g. N and $N+1$, is equal to the chemical potential of the leads, a conduction channel opens and a peak in conductance is observed (see figure 2.20(a)). Between these peaks, transport is suppressed by CB. This results in a series of sharp conductance oscillations, from here on referred to as Coulomb peaks, as a function of gate voltage (see figure 2.20(b)).

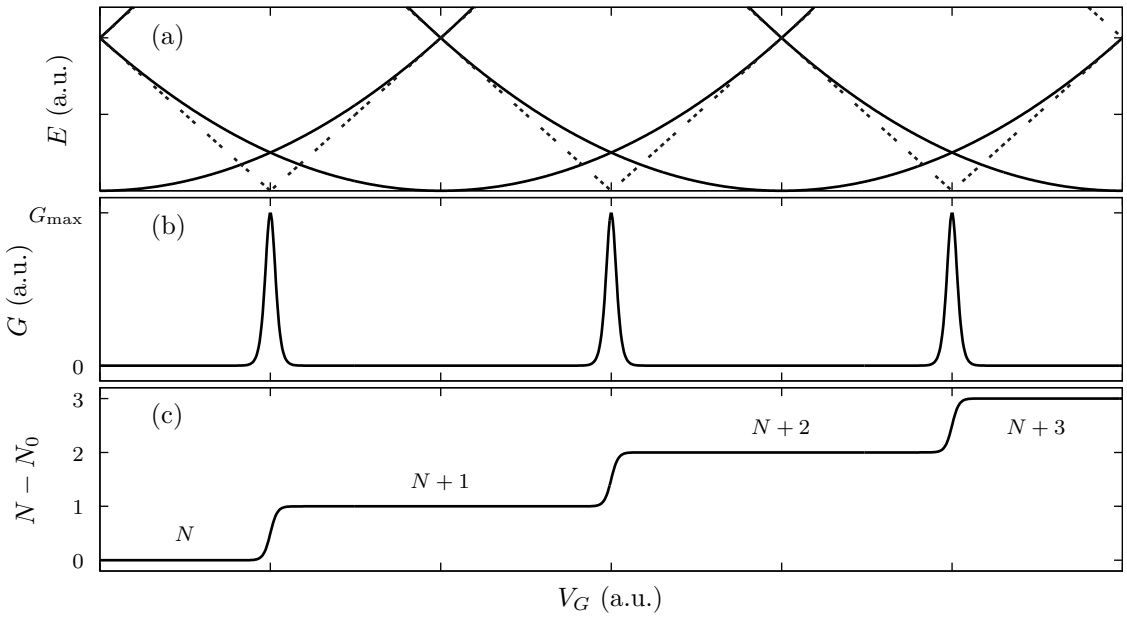


Figure 2.20.: Displayed is the classical model of CB. (a) Energy as a function of gate voltage V_G of the QD with each solid black line representing the electrostatic energy of state with different number of electrons residing on the QD and dashed lines the energy difference between successive states. In (b) the conductance through the QD is shown, which is non-zero at the gate values where two states from (a) intersect, and in (c) the time averaged number of charges on the QD as function of the gate voltage V_G. Adapted from [Hüttel et al., 2005].

Based upon equation (2.9) and equation (2.12), the gate voltage difference ΔV_G required to observe the next CB peak for $N+1$ and $N+2$ can be derived as

$$\Delta V_G = \frac{e}{\alpha_G C_\Sigma} = \frac{e}{C_G}. \tag{2.13}$$

From this, it follows that the difference is independent of the number of electrons N. In the case of a constant α_G, the distance only dependence on the capacitance of the gate. Then equi-distant peaks follow as a function of the gate voltage (figure 2.20(b)).

The tunnel barriers required in order to observe CB strike a delicate balance between isolating the island to preserve charge quantization and permitting sufficient electron tunneling for measurable currents. If the barrier resistance R_T is too high, tunneling events occur too infrequently and the current falls below detectable levels; if R_T is too low, charge quantization is washed out by rapid charge exchange with the leads. This trade-off is succinctly captured by comparing the charge-discharge time $\tau_{RC} = R_T C_\Sigma$

to the characteristic quantum uncertainty time $\hbar/E_\mathrm{C}$. Requiring $\hbar/\tau_\mathrm{RC} \ll E_\mathrm{C}$ yields the condition

$$G_\mathrm{T} = \frac{1}{R_\mathrm{T}} \ll G_Q \equiv \frac{e^2}{h}, \tag{2.14}$$

so that the junction conductance remains below the conductance quantum G_Q. In practice, thin oxide layers (e.g. native Al_2O_3, $\sim 1\,\mathrm{nm}$ to $2\,\mathrm{nm}$ thick) or Schottky barriers at metal–semiconductor interfaces naturally fulfill these criteria, providing tunnel rates while maintaining $G_\mathrm{T} \lesssim G_Q$ and $k_\mathrm{B}T, \Gamma \ll E_\mathrm{C}$.

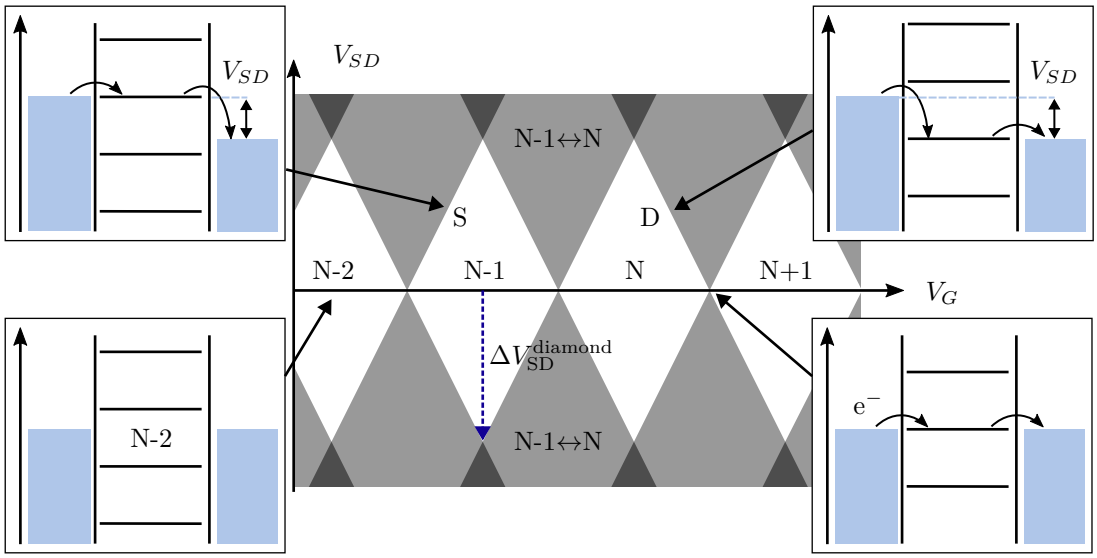


Figure 2.21.: A schematic depiction of a typical CB measurement. The greyscale plot shows the current through a QD as a function of source–drain bias V_SD and gate voltage V_G. White, diamond-shaped regions (labeled by N, $N-1$, etc.) denote blockade regions with a fixed electron number, where conductance is suppressed. Along the $V_\mathrm{SD} = 0$ line, the intersections of successive diamonds correspond to the zero-bias Coulomb oscillations. Finite bias opens a transport window, leading to resonance edge lines (S and D) where the QD's electrochemical potential aligns with μ_S or μ_D, respectively.

When a finite source–drain bias V_SD is applied, the transport window between the source and drain chemical potentials, μ_S and μ_D, opens and the simple picture of periodic conductance peaks at $V_\mathrm{SD} = 0$ evolves into a characteristic "diamond" pattern in the V_SD–V_G plane. In each Coulomb-blockaded region (white diamond shaped areas in figure 2.21), also called Coulomb diamond (CD), no available transition in the QD lies within the bias window, so current is suppressed. At the

boundaries of these diamonds, the electrochemical potential of the QD for adding (or removing) the N^{th} electron aligns with μ_S or μ_D, allowing tunneling through the QD. These boundaries, labeled with **S** and **D**, show up in differential conductance measurements as lines. They are given are given by the conditions

$$\mu_S = E_{\text{C}}(N + \frac{1}{2}) + e\left(\alpha_{\text{G}} V_{\text{G}} + \alpha_{\text{S}} V_{\text{SD}}\right) \quad \text{and} \tag{2.15}$$

$$\mu_D = E_{\text{C}}(N + \frac{1}{2}) + e\left(\alpha_{\text{G}} V_{\text{G}} + (1 - \alpha_{\text{S}})\, V_{\text{SD}}\right), \tag{2.16}$$

respectively, with the conversion factors $\alpha_{\text{S}} = \frac{C_{\text{S}}}{C_\Sigma}$ for the source (and $\alpha_{\text{D}} = \frac{C_{\text{D}}}{C_\Sigma}$ for the drain). The slopes of these lines are determined by the ratios of the capacitance e C_S, C_D, and C_G

$$S_{\text{D}} \equiv \left.\frac{\mathrm{d}V_{\text{G}}}{\mathrm{d}V_{\text{SD}}}\right|_{\text{D}} = -\frac{\alpha_{\text{S}}}{\alpha_{\text{G}}} = -\frac{C_{\text{S}}}{C_{\text{G}}} \tag{2.17}$$

$$S_{\text{S}} \equiv \left.\frac{\mathrm{d}V_{\text{G}}}{\mathrm{d}V_{\text{SD}}}\right|_{\text{S}} = -\frac{1 - \alpha_{\text{S}}}{\alpha_{\text{G}}} = -\frac{C_\Sigma - C_{\text{S}}}{C_{\text{G}}} \tag{2.18}$$

which can be used to extract the gate conversion factor from the CB measurement with

$$\alpha_{\text{G}} = \frac{1}{|S_{\text{S}}^{\text{t}}| + |S_{\text{D}}^{\text{t}}|}. \tag{2.19}$$

In addition to the conversion factor, the charging energy of the QD can be estimated based on the full height of the CD along the V_{SD} axis

$$e\Delta V_{\text{SD}}^{\text{diamond}} \approxeq E_{\text{C}}. \tag{2.20}$$

2.4.2. From SET to Quantum Dot

So far, the mechanisms of CB were purely derived from the electrostatic energy cost of charging a metallic island.

Constant Interaction Model

To capture quantum-mechanical effects beyond the charge quantization, namely the requirement that each additional electron must occupy a distinct quantum state,

the charging energy E_C can be extended with a single-particle term. The *constant interaction model* [Glazman and Shekhter, 1989, McEuen et al., 1991] assumes that all electron–electron interactions are encapsulated in a fixed total capacitance C_Σ, and are thereby treated purely classical, while the single-particle spectrum $\{\varepsilon_i\}$ remains unchanged as electrons are added.

Under these assumptions, the total energy of a QD with N electrons is

$$E(N) = \sum_{i=1}^{N} \varepsilon_i + E_{\text{classic}}(N) = \sum_{i=1}^{N} \varepsilon_i + E_C N^2,$$

where $E_C = e^2/(2C_\Sigma)$ as before. The electrochemical potential for adding the N^{th} electron is then

$$\mu(N) = E(N) - E(N-1) = \varepsilon_N + E_C(2N-1).$$

Hence the addition energy between successive charge states becomes

$$\Delta E_{\text{add}}(N) = \mu(N+1) - \mu(N) = \underbrace{\varepsilon_{N+1} - \varepsilon_N}_{\delta_S(N)} + \frac{e^2}{C_\Sigma}.$$

In the limit $\delta_S \ll E_C$, the classical Coulomb peaks recover with constant separation; when $\delta_S \sim E_C$, the peak spacings acquire an additional, level-dependent contribution.

Because the QD is capacitively coupled to the gate electrode via C_G, each conductance peak occurs when $\mu(N)$ aligns with the leads. The corresponding spacing in gate voltage (equation (2.13)) is adjusted to

$$|\Delta V_G(N)| = \frac{\Delta E_{\text{add}}(N)}{e\alpha} = \frac{\frac{e^2}{C_\Sigma} + \delta_S(N)}{e\alpha_G} = \frac{1}{e\alpha_G}\delta_S(N) + \frac{e}{C_G}. \tag{2.21}$$

Thus, deviations from uniform peak spacing can reveal the influence of discrete level spacing in small or semiconducting QDs.

Reaching the bandgap of a semiconductor, no further states can be occupied below the CBM (VBM for holes). Therefore, a CD with a width corresponding to the bandgap is expected. Simulations for graphene based QDs show such an expected CD for a transport measurement around the bandgap edge (see figure 2.22). Additionally, the CD size above the band gap decreases due to lower additional energy requirement for higher number of electrons [Moulhim et al., 2022].

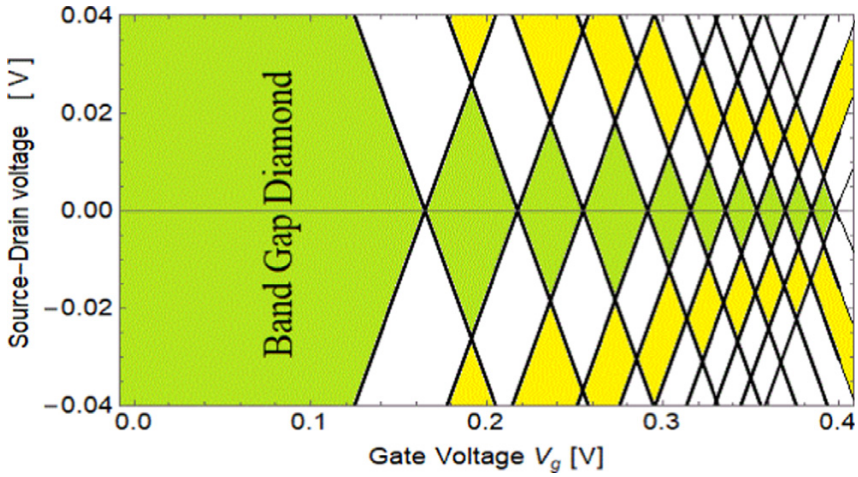


Figure 2.22.: Simulated CB measurements of a graphene based QD near the band gap. The green area corresponds to the blocked region with a fixed number of electrons on the QD and the white and yellow indicate current running through the system. Figure adapted from [Moulhim et al., 2022].

2.4.3. Coulomb Peak Shapes

Based upon the level spacing δ_S, the electrostatic charging energy E_C, and the lifetime broadening $\hbar\Gamma$ of a single level, three regimes in terms of temperature can be defined:

- Classical limit: $\hbar\Gamma \ll \delta_S \ll k_B T \ll E_C$

  When both the lifetime broadening and the level spacing are smaller then the thermal energy, the system acts like a "classical" metallic island [Kulik and Shekhter, 1975, Averin and Likharev, 1986, Beenakker, 1991]. Here, electrons tunnel in and out of multiple levels inside the QD as multiple are accessible through the thermal energy. Also the electrostatic energy is by far the largest component of the charging energy and therefore the Coulomb peaks are spaced in regular intervals of V_G. With the DOS inside the QD D and the tunneling rates of both source Γ_S and drain Γ_D the conductance is given by

$$G(V_G, T) = G_{max} \frac{e\alpha_G (V_G - V_{G,0})}{k_B T} \sinh^{-1}\left(\frac{e\alpha_G (V_G - V_{G,0})}{k_B T}\right)$$
$$\simeq G_{max} \cosh^{-2}\left(\frac{e\alpha_G (V_G - V_{G,0})}{2.5 k_B T}\right) \tag{2.22}$$

with a maximum conductance of

$$G_{max} = \frac{e^2 D}{2} \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D}, \tag{2.23}$$

see [Beenakker, 1991]. Equation (2.22) gives a peak width that follows the thermal broadening of the leads, whereas the peak height, in equation (2.23), is independent of the temperature.

- Thermally broadened single level transport: $\hbar\Gamma \ll k_B T \ll \delta_S \lesssim E_C$

  As the temperature decreases (or the size of QD is decreases and in turn increase δ_S and E_C) electrons are no longer able to tunnel into a multitude of levels inside the QD. Instead tunneling occurs only into a single level and the level spacing is comparable to the electrostatic charging energy. Consequently, the spacing of the Coulomb peaks becomes irregular, as the additional energy required to access successive levels varies, or may vanish when tunnelling occurs into a (for example, spin-) degenerate state. The conductance is found to be

$$G(V_G, T) = G_{max} \cosh^{-2}\left(\frac{e\alpha_G (V_G - V_{G,0})}{2 k_B T}\right) \tag{2.24}$$

  with a maximum conductance of

$$G_{max}(T) = \frac{e^2}{4 k_B T} \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D}. \tag{2.25}$$

  This relation was first discovered by [Beenakker, 1991]. Compared to the "classical" limit, the peak width given by the $\cosh^{-2}$ in equation (2.24) is slightly larger but still follows the electron temperature. The peak height, however, becomes inversely proportional to the temperature.

- Lifetime broadened single level transport: $k_B T \ll \hbar\Gamma \ll \delta_S \ll E_C$

In the case above, the maximum conductance increases with reducing temperature, which would imply that in the limit $T \to 0$ the conductance exceeds G_0 and goes to infinity. This can only be possible with a superconductor, which is certainly not the case here. Therefore another regime with $G_{\max} \leq G_0$ must exist.

In the previous regime, transport was limited by the DOS inside the leads which can tunnel into the single level of the QD. As the temperature is reduced, the Fermi distribution of electrons inside the leads became sharper and the number of carriers which can tunnel increases. Now, in the same picture, one can think of the lead distribution getting sharper than the energy uncertainty broadened level ($\hbar \leq \Delta E \Delta t$ with $\Delta t \propto 1/\Gamma$). Then the conduction is dominated by the lifetime Γ of the single level, as given by the Breit-Wigner formula

$$G(V_\mathrm{G}, \Gamma) = G_{\max} \frac{\left(\frac{\Gamma}{2}\right)^2}{\left(\frac{\Gamma}{2}\right)^2 + \left(e\alpha_\mathrm{G}\left(V_\mathrm{G} - V_{\mathrm{G},0}\right)\right)^2} \tag{2.26}$$

where the maximum conductance

$$G_{\max}(\Gamma) = \mathcal{G}\frac{e^2}{\hbar}\frac{\Gamma_\mathrm{S}\Gamma_\mathrm{D}}{\Gamma_\mathrm{S} + \Gamma_\mathrm{D}}\frac{4}{\Gamma} \tag{2.27}$$

is again independent of the temperature [Beenakker, 1991]. $\mathcal{G}$ gives the degeneracy of the level involved.

In a realistic experimental setup, the lifetime broadening is often close to the thermal energy $\hbar\Gamma \approxeq k_\mathrm{B}T$ and therefore a mixed regime of thermal broadened and lifetime broadened single level transport has to be considered. Then, as [Goldhaber-Gordon et al., 1998] derived, the full width half maximum (FWHM) is given as a convolution of a Lorentz curve of Γ and the derivative of the Fermi function of the leads

$$\mathrm{FWHM}(\Gamma, T) = 0.7\frac{\hbar\Gamma}{e} + 3.52k_\mathrm{B}T. \tag{2.28}$$

This can be used to extract the tunneling rates in the $T = 0\,\mathrm{K}$ limit.

Excited State Spectroscopy

Previously, only the case of transport through single levels inside the QD in the linear ($V_{\mathrm{SD}} \cong 0\,\mathrm{V}$) response regime was discussed. There the QD is always transitioning between ground states, where every successive level is filled and, as the gate voltage is shifted, an electron can be moved into the next unoccupied level. The QD can hence only be in two states, the ground state of the N electron and the ground state of the $N+1$ electron system.
If a finite bias voltage is applied, the conductance peaks broaden, following the lines **S** and **D** in figure 2.21 forming the blocked CDs. In the case of single level transport, the additional energy from the bias voltage eV_{SD} can allow for transport through further states, which are energetically unfavorable compared to the ground state. The energy $E^*(N+1)$ of such a state, for example the $(N+1)$th electron in second lowest unoccupied level, would lie in between $E(N+1)$ and $E(N+2)$, making it inaccessible in the linear regime.

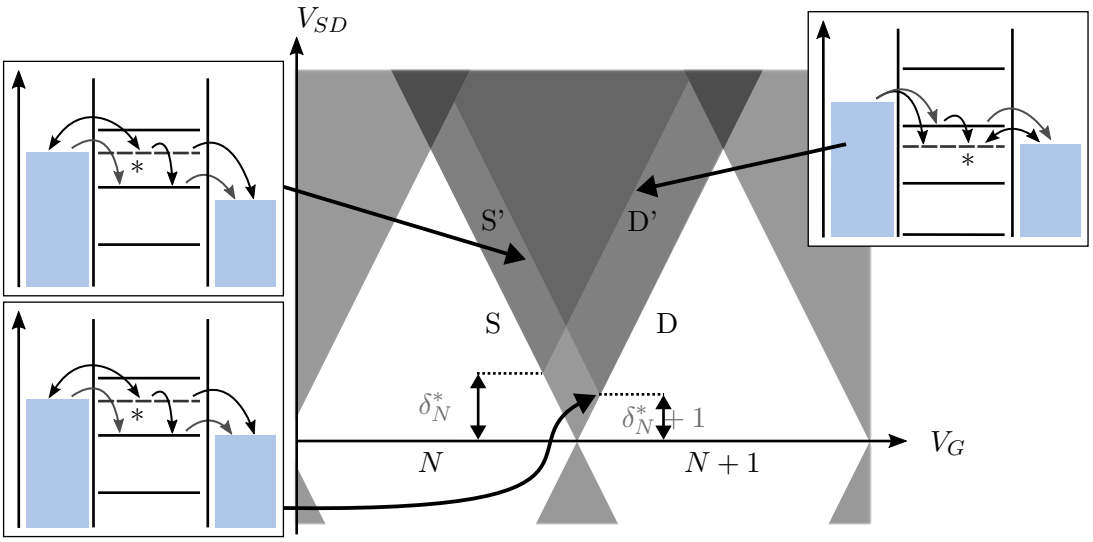


Figure 2.23.: Schematic of transport through excited states. In addition to the lines **S** and **D** two lines of elevated conduction are display **S'** and **D'**. These correspond to emergence of additional conduction channels through excited states of the QD (see insets). The energy spacing between the ground and excited state δ^* can be determined through the intersect point of **S'** and **D** (**D'** and **S** respectively).

With a finite bias voltage $eV_{\mathrm{SD}} > 0$ enough energy is provided in order to tunnel from a lead into such an excited state instead of the ground state. This additional transport channel will then manifest as a change in current, showing up as a section

of different color in the V_G vs. V_{SD} map (see figure 2.23). At the edges, marked with S' and D', the chemical potential of the leads are

$$\mu_S = E^*(N+1) - E(N) > E(N+1) - E(N) \tag{2.29}$$

and

$$\mu_D = E(N+1) - E^*(N) < E(N+1) - E(N), \tag{2.30}$$

respectively. With these condition, the energy difference between the ground state $N+1$ and $(N+1)^*$ can be extracted from the intersection point of the line S' and D (or D' and S). At these points the chemical potential of the leads match the energy difference between the excited state and the corresponding ground state $\delta_N^* = eV_{SD}$ (see the left lower inset in figure 2.23).

It should be noted that tunneling into an excited state does not necessarily result in an increase in current. The resulting transport characteristics depend sensitively on the properties of the excited state, its lifetime, coupling strength to the leads, and wave-function overlap, which determine the respective tunnel rates. For instance, if an excited state exhibits strong coupling to the source but weak coupling to the drain, electrons will frequently tunnel into this state. However, due to the low tunneling probability into the drain and the long lifetime of the state, the electron will remain trapped for a comparatively long time before decaying. During this period, the QD is already in the $N+1$ charge state, preventing additional electrons from entering the ground state and contributing to transport. Only after the excited state has decayed or the electron has tunneled out to the drain, transport through the ground state can resume. Consequently, the total current is reduced which will show up as a line of negative conductance in differential conductance measurements. Such phenomena fall under the overall term "transport blockade".

2.4.4. Effect of Magnetic Fields on Single Level Transport

Thus far, the potential degeneracy of specific quantum-dot energy levels, such as ϵ_N and ϵ_{N+1}, has not been explicitly addressed. In such cases, the level spacing $\delta_S(N+1)$ vanishes, and the addition of an extra electron requires only the electrostatic charging energy. The most prominent example of this type of degeneracy is the spin degeneracy of electronic states. When a magnetic field $\vec{B}$ is applied, this degeneracy is lifted due to the Zeeman effect, which introduces an energy splitting between the

spin-up and spin-down components of each orbital level. In the simplest case, the energy difference between the spin states is given by

$$E_{\mathrm{Z}} = g\mu_{\mathrm{B}}\vec{B}\vec{S},$$

where g is the effective Landé g-factor, μ_{B} the Bohr magneton, and $\vec{S}$ is the spin. In CB spectroscopy, this splitting manifests as a shift of the conductance resonances in source–drain bias or gate voltage that increases linearly with B. As the peaks corresponding to the degenerate levels are separated by the electrostatic charging energy, no direct splitting is observed; rather the two successive resonances separate further with increasing B. The shift for each peak is then given by

$$\Delta V_{\mathrm{G,Z}} = \frac{1}{2}\frac{E_Z}{e\alpha_{\mathrm{G}}}, \tag{2.31}$$

with a factor 1/2 which permits direct extraction of g in gated MoS_2 nanotube devices.

Fock–Darwin Spectrum

Beyond spin splitting, a perpendicular magnetic field also modifies the orbital motion of electrons in a confined QD. This effect can be studied by through the simple model of a disc-shaped QD with harmonic confinement. In the constant-interaction picture augmented by a two-dimensional harmonic confinement,

$$V(r) = \frac{1}{2}m^*\omega_0^2\, r^2,$$

the single-particle levels evolve into the so-called Fock–Darwin spectrum. Introducing the cyclotron frequency for a magnetic field perpendicular to the disc,

$$\omega_c = \frac{eB}{m^*},$$

one finds for each radial quantum number $n = 0, 1, 2, \ldots$ and angular momentum $l = 0, \pm1, \pm2, \ldots$:

$$E_{n,l}(B) = \Big(2n + |l| + 1\Big)\hbar\sqrt{\omega_0^2 + \tfrac{1}{4}\omega_c^2} - \tfrac{1}{2}l\hbar\omega_c. \tag{2.32}$$

At $B = 0$, this reduces to the familiar level spacing $\hbar\omega_0$. As B increases, levels with positive and negative l split apart: the $\sqrt{\omega_0^2 + \omega_c^2/4}$ term shifts all states

upward, while the $-l\,\hbar\omega_c/2$ term produces opposite slopes for $\pm l$. In transport measurements (figure 2.24(a)), these evolving orbital energies manifest as non-monotonic shifts and "kinks" in Coulomb peak positions versus B (b), signalling transitions between orbitals of different angular momentum. This model initially stems from GaAs/AlGaAs QDs with the corresponding device geometry.

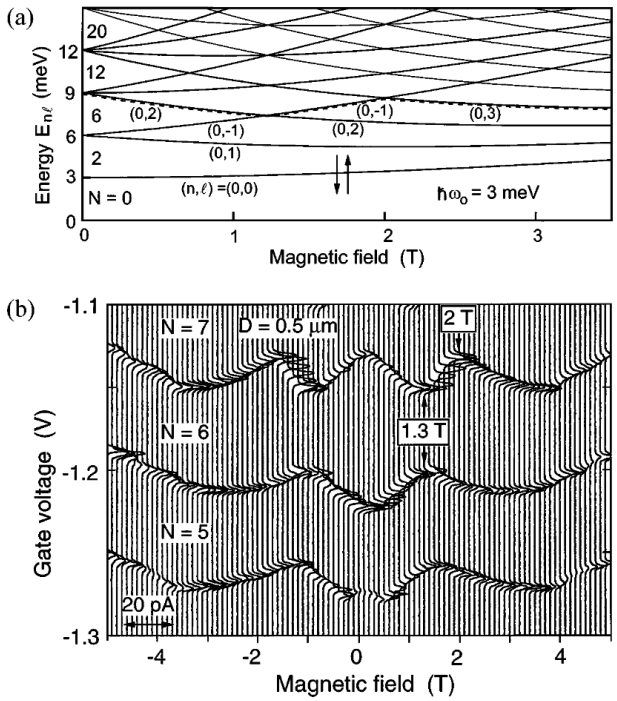


Figure 2.24: Effect of a magnetic field on a circular QD inside GaAs. (a) shows the calculated single-particle energy as a function of magnetic field. (b) Measured gate traces stacked for different B field values of a QD with diameter of 500 nm. From [Tarucha et al., 1996].

For MoS_2 nanotube QDs, the larger effective mass m^* and reduced dielectric screening moderate the orbital dispersion compared to III–V systems, but the qualitative behavior-level crossings, slope changes, and characteristic inflection points-remains a useful framework for interpreting excited-state spectroscopy under magnetic fields.

2.4.5. Disordered Quantum Dots

So far, only perfectly clean systems without any disorder are considered. However, as the QD have to be sufficiently small, requiring nanoscale fabrication, any disorder introduced in a practical application can lead to a variety of effects. For this thesis, a major challenge lays in the formation of multiple QD systems, both through a distorted electrical potential as well as impurities in the studied MoS_2 NTs and their contact interfaces. Additionally, the formation of charge traps is considered.

Multi-Quantum Dots Systems

Previously, a metallic island was considered as the basis of a (classical) QD, defined by its size and by contacts satisfying the constraints from equation (2.14). Two implicit assumptions were made in this context:

- The electric potential of the gate electrode is constant throughout the island.
- The electronic system of the island itself is homogeneous and forms one continues state spanning the entire physically defined QD.

These constraints are not easily met and it took many years of research to enhance fabrication techniques and reduced disorder in material systems similar to MoS_2 such as CNTs and graphene [Kuemmeth et al., 2008, Engels et al., 2013, Banszerus et al., 2018].
If one or both are not met, instead of the desired single QD a system of multiple QDs is most likely to form, with the inhomogeneities forming barriers between adjacent islands. This, in itself, does not alter the underlying principles and multi-dot systems are subject of many research efforts [Hofmann et al., 1995, van der Wiel et al., 2002, Volk et al., 2011]. Compared to the case of a single QD, the number of electrons on each island is still a function of the external capacitance, but this is no longer just a function of gate and contacts. Instead it includes the charges on all other QDs, rendering the system much more complex. If one can influence the charge on each QD separately and the shielding in between the QD is sufficiently strong (which can both be achieved by fabricating gates for each QD individually [van der Wiel et al., 2002, Banszerus et al., 2018]), the system can be analyzed within its full range of parameters.
However, in the case that the formation of multiple QDs is a result of disorder, this is scarcely the case. Rather, all QDs are coupled to a universal gate, with presumably different coupling strengths and coupling between each other. Therefore, a modulation of only this gate corresponds to a slice through the multidimensional space of the induced charge in all QDs. It is actually repetitive but due to the arbitrary (and complexly defined) angle of the slice, the repetition period can be very large (10s to 10000s times the width of 1 CB diamond) or even effectively irregular. Examples of CB calculations of such systems are shown in figure 2.25 with two QDs in series (a) and four QDs (b).

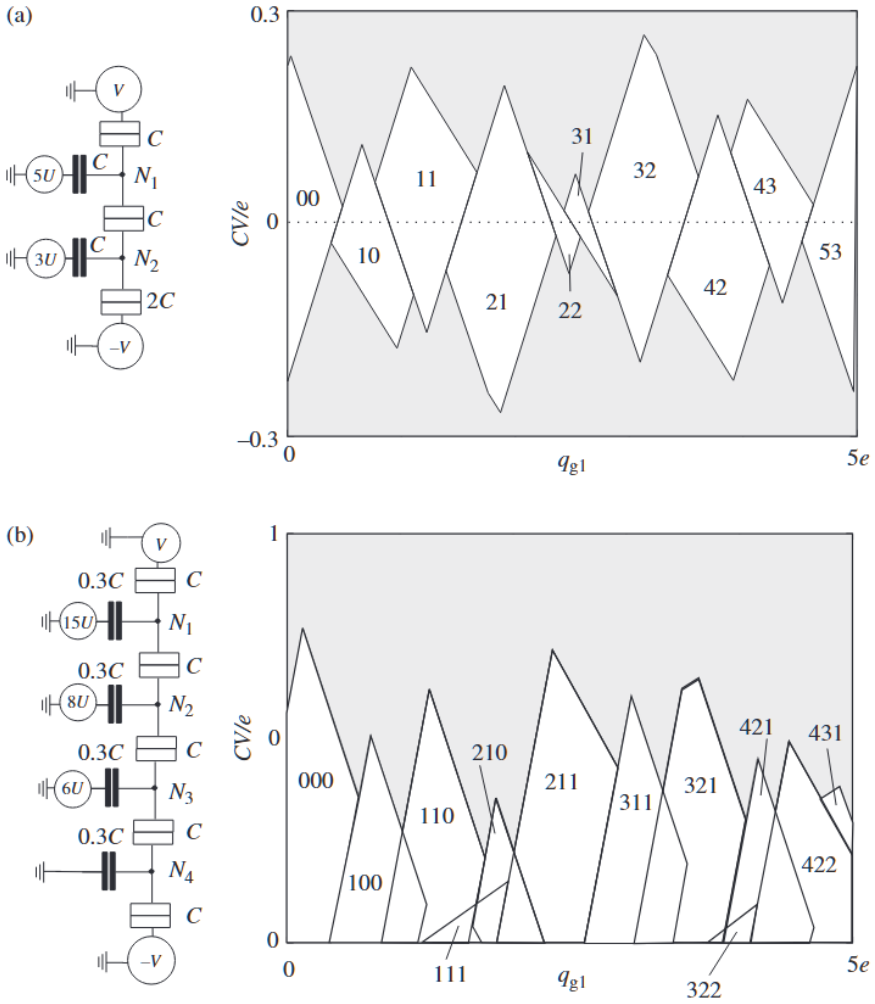


Figure 2.25.: Schematics of a multi QD systems. (a) System of two QDs in succession with different couplings to the backgate. (b) System of four QDs. From [Nazarov and Blanter, 2009].

Trapped Charges

Another source of disorder in QD measurements arises from localized charge traps in the vicinity of the device. These can be impurity states or isolated dopants that are weakly tunnel-coupled but capacitively interact with the QD. When a trap switches between different charge states during a measurement, it abruptly shifts the QD's electrostatic potential, leading to anomalies in the CB spectrum. Specifically, one observes duplicated or distorted CDs, with a characteristic offset between the two configurations corresponding to different trap occupations. The logic is very similar to disordered multiple QD systems, just that the conditions for current flow differ. An

illustrative example is shown in figure 2.26, which depicts simulations of a QD coupled to a charge trap under different capacitive configurations [Hofheinz et al., 2006].

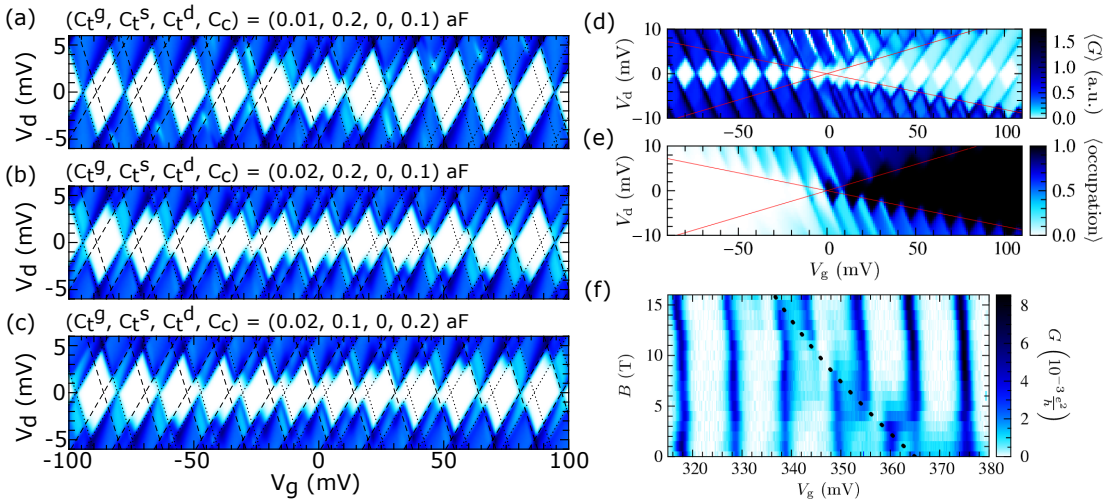


Figure 2.26.: Simulations of a charge trap near a QD for different parameters. (a) A trap located near the source electrode. (b) The capacitance between gate and trap is increased, leading to wider trap signatures. (c) Strong coupling to the QD and reduced coupling to the source electrode. (d) and (e) further simulations with the occupation number of the QD in (e) and red lines marking the change in the QDs state. Adapted from [Hofheinz et al., 2006].

The strength and nature of the observed features depend on the capacitive coupling of the trap to the gate, source, drain, and the QD itself. These couplings define two key parameters: the lever arm of the trap with respect to the gate, $\alpha_\mathrm{t} = \frac{C_\mathrm{G}^\mathrm{t}}{C_\mathrm{t}+C_\mathrm{C}}$, and the electrostatic lever between the trap and the QD, $\beta_\mathrm{t} = \frac{C_\mathrm{C}}{C_\mathrm{t}+C_\mathrm{C}}$. Here, C_C is the capacitive coupling between the trap and the QD, C_t is the capacitance of the QD, and C_G^t is the capacitance between the trap and the gate. The latter determines the shift in gate voltage per change in trap charge and is given by

$$\beta_\mathrm{t} = \frac{\Delta V_\mathrm{G}^\mathrm{t}}{\Delta V_\mathrm{G}^\mathrm{m}} \tag{2.33}$$

where $\Delta V_\mathrm{G}^\mathrm{t}$ is the shift induced by a trap transition and $\Delta V_\mathrm{G}^\mathrm{m}$ is the Coulomb peak spacing of the unperturbed QD. Depending on the relative position of the trap (e. g. near source or drain) and the dominant capacitive coupling, the trap signature appears as characteristic “teeth” structures on either the positive or negative slopes of the CDs, as seen in panels (a)–(e) of figure 2.26. A second approach to determine

β_t can be done via the red slopes in (d) and (e). These lines follow the slope $S_S^t = \frac{C_G^t}{C_t}$ and $S_D^t = -\frac{C_G^t}{C_C}$, which can be used to extract

$$\beta_t = \frac{1}{S_D\left(\frac{1}{S_D} - \frac{1}{S_S}\right)} \quad \text{and} \quad \alpha_t = \frac{1}{\left(\frac{1}{S_S} - \frac{1}{S_D}\right)}. \tag{2.34}$$

In addition to charge sensing, the same trap-induced features can reveal information about spin states. If the trap hosts a single electron, the application of a magnetic field induces a Zeeman shift in its energy level, which translates into a shift of the trap's signature in gate voltage, which is visible as jumps in the Coulomb peak position as a function of the applied field (see figure 2.26(f)). This shift follows

$$\frac{\partial V_G}{\partial B} = \frac{g\mu_B \Delta S_z}{e\alpha_t}, \tag{2.35}$$

where g is the Landé g-factor, μ_B is the Bohr magneton, and $\Delta S_z = \pm\frac{1}{2}$ for single-electron transitions. These Zeeman shifts provide a method to identify singly versus doubly occupied traps and to confirm the spin-$\frac{1}{2}$ nature of isolated donor states in the channel. In the original work by [Hofheinz et al., 2006], the majority of trap-induced shifts under magnetic field were consistent with the filling of a singly occupied spin state, supporting their identification as arsenic donor atoms embedded within the silicon nanowire.

2.4.6. Quantum Dots in Planar MoS_2

A useful reference point for understanding confinement in TMDC systems is provided by simulations of QDs in planar MoS_2, presented by [Kormányos et al., 2014]. Their model focuses on the conduction band, suitable for n-type systems, and includes spin and valley degrees of freedom via an effective Hamiltonian, resulting in a parabolic, isotropic dispersion. Owing to the well-separated conduction-band minima at the K and K', Q valley can be neglected in MoS_2, unlike in other TMDCs where it lies close in energy.

Strong intrinsic SOC and the lack of inversion symmetry cause a small spin splitting of approximately $\Delta_{SO} = 1.5\,\text{meV}$ near the K and K' points (see figure 2.27(a)). This splitting leads to a spin-dependent effective mass, with $m_{\text{eff}}^{K,\uparrow} = 0.49\,m_e$ and $m_{\text{eff}}^{K,\downarrow} = 0.44\,m_e$. At zero magnetic field, states with identical valley index and opposite spins are shifted by $2\Delta_{SO}$, while states from opposite valleys remain degenerate due to time-reversal symmetry.

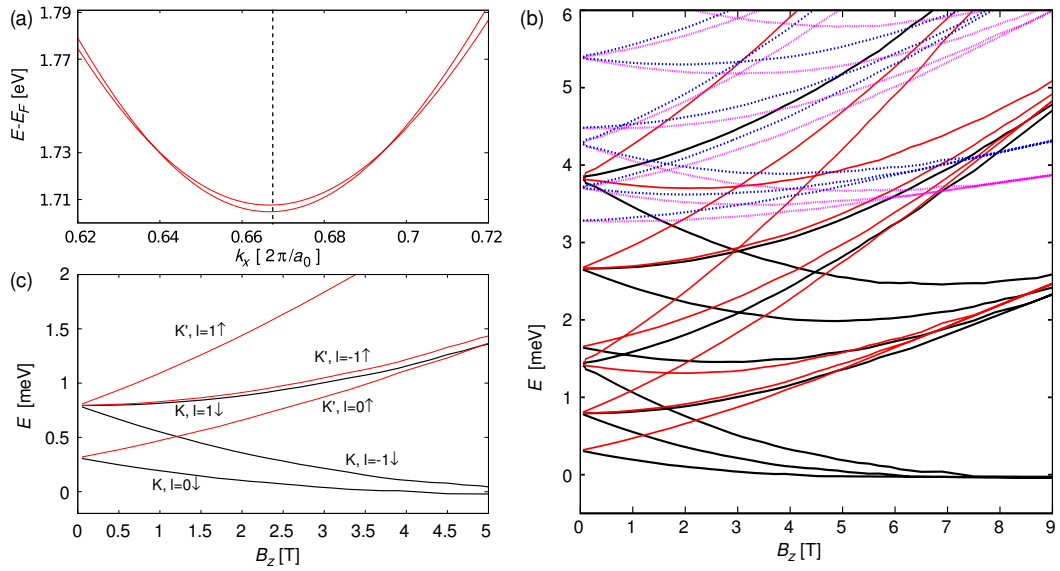


Figure 2.27.: Simulations of a QD in planar MoS_2 and the effect of an magnetic field. (a) Bandstructure of monolayer MoS_2 with a spin-splitting of $\approx 1.5\,\text{meV}$ at the CBM. (b) Simulated effect on out-of-plane magnetic field on the energy levels of a monolayer MoS_2 QD with a radius of $R \approx 40\,\text{nm}$. Black (purple) lines correspond to spin $\downarrow$ ($\uparrow$) in the K- and red (blue) dotted lines $\uparrow$ ($\downarrow$) in the K'-valley. (c) Zoom into (b) showing only orbital states with the orbital quantum number $|l| < 1$ for small magnetic fields. Adapted from [Kormányos et al., 2014].

When a perpendicular magnetic field is applied, this degeneracy is lifted. Both the spin and valley states experience distinct shifts: the spin splitting increases linearly due to an effective out-of-plane g-factor of approximately $g_{\text{sp}}^{\perp} \approx 2$, while the degeneracy between opposite valleys is broken through an additional valley Zeeman term, where the magnetic field couples to the orbital angular momentum of the electrons. The resulting energy level structure is shown in figure 2.27(b), which displays calculated energy levels of a circular QD with radius $R_{\text{QD}} = 40\,\text{nm}$ as a function of magnetic field. As expected, in the absence of a magnetic field, states with opposite angular momentum in the same valley are degenerate due to time-reversal symmetry, while the opposed spin state in the same valley is shifted by $2\Delta_{\text{SO}}$ (black vs. purple and red vs. blue lines). When a perpendicular magnetic field is applied, both the degeneracy in opposing valleys is lifted, and at higher fields the discrete QD states evolve into Landau levels once the magnetic length becomes comparable to the QD radius $l_B \lesssim R_{\text{QD}}$.

A more detailed view of the low-energy spectrum with orbital quantum numbers $|l| \leq 1$ is shown in figure 2.27(c). It reveals that for magnetic fields $B_z \lesssim 2\,\mathrm{T}$ the lowest states are localized in the K and K' valleys. Unlike in gapped monolayer or bilayer graphene, these states are also spin-polarized, reflecting the intrinsic spin–orbit coupling in the MoS_2 conduction band. Consequently, QDs in MoS_2 can act as simultaneous spin and valley filters, allowing selective control over both degrees of freedom [Kormányos et al., 2014].

Liu et al. simulated QDs with varying size to estimate the inter-valley coupling. For all simulated *shapes* (e.g. sizes, boundaries, potential depts, etc.) they found a maximal inter-valley coupling of $\Delta_{KK'} \lesssim 0.1\,\mathrm{meV}$. The precise value varied very strongly with the size, center position (zero mixing for QDs center on Mo-sites), shape, and orientation towards the crystalline axes. Even though a rapid (lattice-constant scale) oscillation of the mixing is observed for varying diameters, the overall trend is an exponential decay with the size [Liu et al., 2014]. This indicates that for QDs with diameters exceeding 20 nm the inter-valley coupling is always much lower than the SOC $\Delta_{KK'} \ll \Delta_{\mathrm{SO}}$. As previously established, the NTs in this thesis almost entirely exceed radii of 10 nm corresponding to a surface area larger then this limit. Consequently, a significant intrinsic inter-valley coupling compared to the SOC is not expected.

Expected Confinement Quantization in Nanotube Based QDs

[Kormányos et al., 2014] estimated the required confinement using $\delta_{\mathrm{S}} = 2\pi\hbar^2/(m_{\mathrm{eff}}A)$ and expected a level spacing of $\delta_{\mathrm{S}} \approx 0.2\,\mathrm{meV}$ for a 40 nm radius QD, corresponding to a thermal energy of $T = 2.3\,\mathrm{K}$. As a dilution refrigerator system (section 3.2.3) with a base temperature of 10 mK is used here, the required radius can be calculated to be smaller than

$$k_{\mathrm{B}}T = \frac{2\pi\hbar^2}{m_{\mathrm{eff}}A} \leftrightarrow r = \sqrt{\frac{2\hbar^2}{k_{\mathrm{B}}T m_{\mathrm{eff}}}}. \tag{2.36}$$

At base temperature, a QD with a radius smaller then 630 nm would be sufficient, whereas for 100 mK the required radius is already reduced to 200 nm. However, this is only a very rough limit, as the temperature which needs to be considered here is the electron temperature in the leads, which can be higher than the nominal base temperature if cable filtering is insufficient.

As the use of a NT naturally confines the system to the nanotube circumference, the required length of a NT hosting a QD in the single level transport regime can be estimated. Then the area A of the QD is given by the surface area of the nanotube, $A = 2\pi r_{\mathrm{NT}} L_{\mathrm{NT}}$. Similarly for a collapsed NR, the surface area is two times that of a 2D QD of given width $w_{\mathrm{NR}} \times L_{\mathrm{NR}}$, neglecting the curved sides for the moment. In table 2.2 the required lengths for different NT radii and different ribbon widths at different temperatures are listed.

Table 2.2.: Required length of a NT L_{NT} or a NR L_{NR} QD for different temperatures in order to exhibit a level spacing of similar size to the thermal energy.

T(mK)	$r_{\mathrm{nt}} = 20\,\mathrm{nm}$	$r_{\mathrm{nt}} = 50\,\mathrm{nm}$	$w_{\mathrm{nr}} = 50\,\mathrm{nm}$	$w_{\mathrm{nr}} = 500\,\mathrm{nm}$
10	9 µm	3.6 µm	12.5 µm	1.3 µm
100	1 µm	400 nm	1.3 µm	125 nm

These values are upper bounds and one should stay well below these limits (at least for 10 mK) in order to observed single level transport. However, the required confinements are within reach of standard electron beam lithography (EBL) procedures, and the use of thin NTs or small NRs already relaxes lithographic constraints for the formation of QDs in TMDC materials. As all NTs investigated in this thesis are multi-walled, a possible QD could extend across multiple layers, thereby further reducing the required NT length.
From section 2.3.2, it is known that multi-walled NTs are likely chiral, with each layer exhibiting a distinct chirality. Since the chiral index determines both the magnitude and type of the band gap [Milivojević et al., 2020], the position of the QD in k-space and its resulting transport characteristics cannot be precisely predicted. Because the SOC is suppressed at the high-symmetry points, an observable effect is expected only if the NT possesses an indirect band gap. This could provide an indication of its chirality; however, due to the vast number of possible chiral indices corresponding to the expected NT radii, the chirality cannot be deduced from this information alone. Based on the findings of [Li and Mason, 2013], a negligible $\Delta_{KK'}$ can at least be expected for the given device dimensions.

3. Fabrication and Measurement Techniques

This chapter will summarize all methods used throughout the this thesis for device fabrication, characterization and measurement.

3.1. Device Fabrication

So far, direct growth of the TMDC NTs on chip and/or contact surfaces is not directly possible using the CVT process describe in section 2.3.2. Therefore, the NTs have to be transferred from the surface of the glass ampoule onto a substrate. This is done using different methods, which will be discussed in the following sections. A detailed description of most of the following methods can also be found in [Schock et al., 2024].

3.1.1. Scotch Tape Transfer

A deceptively simple yet effective approach to incorporate MoS_2 NTs into functional devices is the well-known tape-assisted transfer technique, originally demonstrated for graphene [Novoselov et al., 2004] (see figure 3.1). In the implementation here, a strip of *Nitto Denko ELP BT-150E-CM* adhesive tape is first applied to the as-grown MoS_2 NT ensemble on a fragment of the quartz growth ampoule. Next the tape, now bearing a random assortment of NTs, flakes and other MoS_2 nanostructures, is pressed onto a p-doped (boron) Si wafer capped with a thermally grown 500 nm SiO_2 layer and lithographically defined Cr–Au alignment markers (with a distance of 50 µm, see figure 3.1(b,c)), which where thankfully provided by PD Dr. Jonathan Eroms.

Despite its operational simplicity and compatibility with large substrates, this method invariably transfers a fraction of the adhesive polymer onto the target,

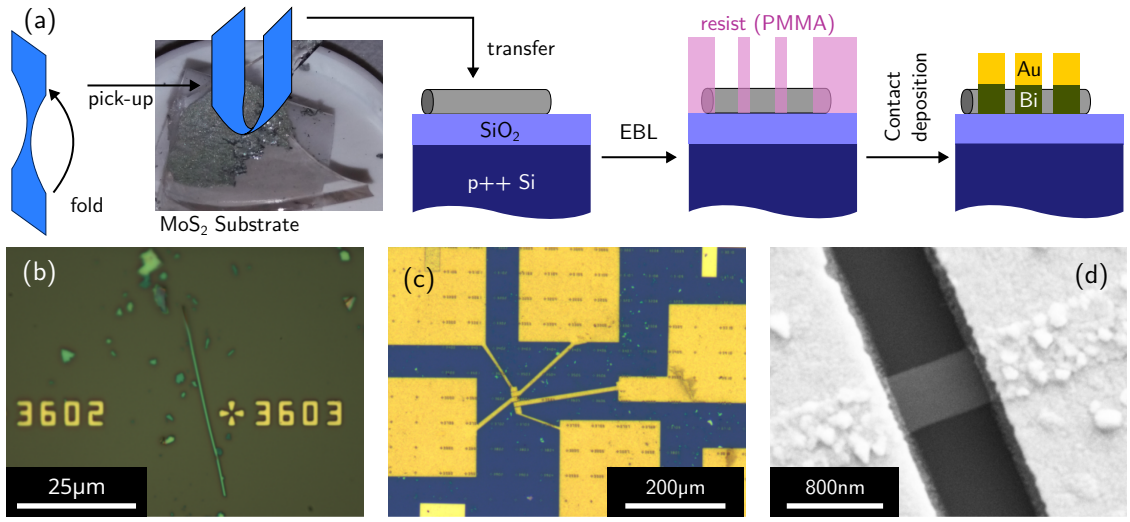


Figure 3.1.: Illustration of the tape-assisted transfer (*Scotch tape*) method used here. (a) Schematics of the transfer process: First a strip of *Nitto Denko ELP BT-150E-CM* tape is cut so that its midsection is narrowed, then folded and gently pressed onto the MoS_2 NT growth substrate (a fragment of the original quartz ampoule), thereby picking up individual NTs. These are subsequently placed onto a p-doped Si–SiO_2 receiving substrate. Finally, contacts are defined on the transferred NTs by electron-beam lithography followed by contact metal deposition and lift-off. (b-d) Optical images of a NR on chip 1 after transfer (b) and after contact deposition (c) as well as a SEM micrograph of the trench between to contacts with the exposed NR (d). From [Schock et al., 2023].

producing patches of residual glue that may compromise device performance. Moreover, the random placement necessitates post-transfer localization and selection of suitable NTs, limiting throughput in large scale applications. The individual NT are localised via optical microscopy, where remarkably it is possible to detect NTs with diameters down to 20 nm, most likely due to their extraordinary optical properties [Kazanov et al., 2018, Remškar et al., 2022].

Once the position on the chip is established, the images are used to design contact geometries for lithography. After spin-coating with a layer of resist, e.g. a 9 % solution of Poly(methyl methacrylate) (PMMA) 200k (molecular weight (MW) of 200 ku) in anisole, and back-out for 5 min at $T = 150\,°C$, a standard EBL process is performed with a *Zeiss Supra™ VP 55* SEM at a beam acceleration voltage of 30 kV. The resist is subsequently developed in a methyl isobutyl ketone (MIBK), isopropyl mixture of ratio 1:3 for 45 s and rinsed in isopropyl for 90 s. This is followed by the contact deposition.

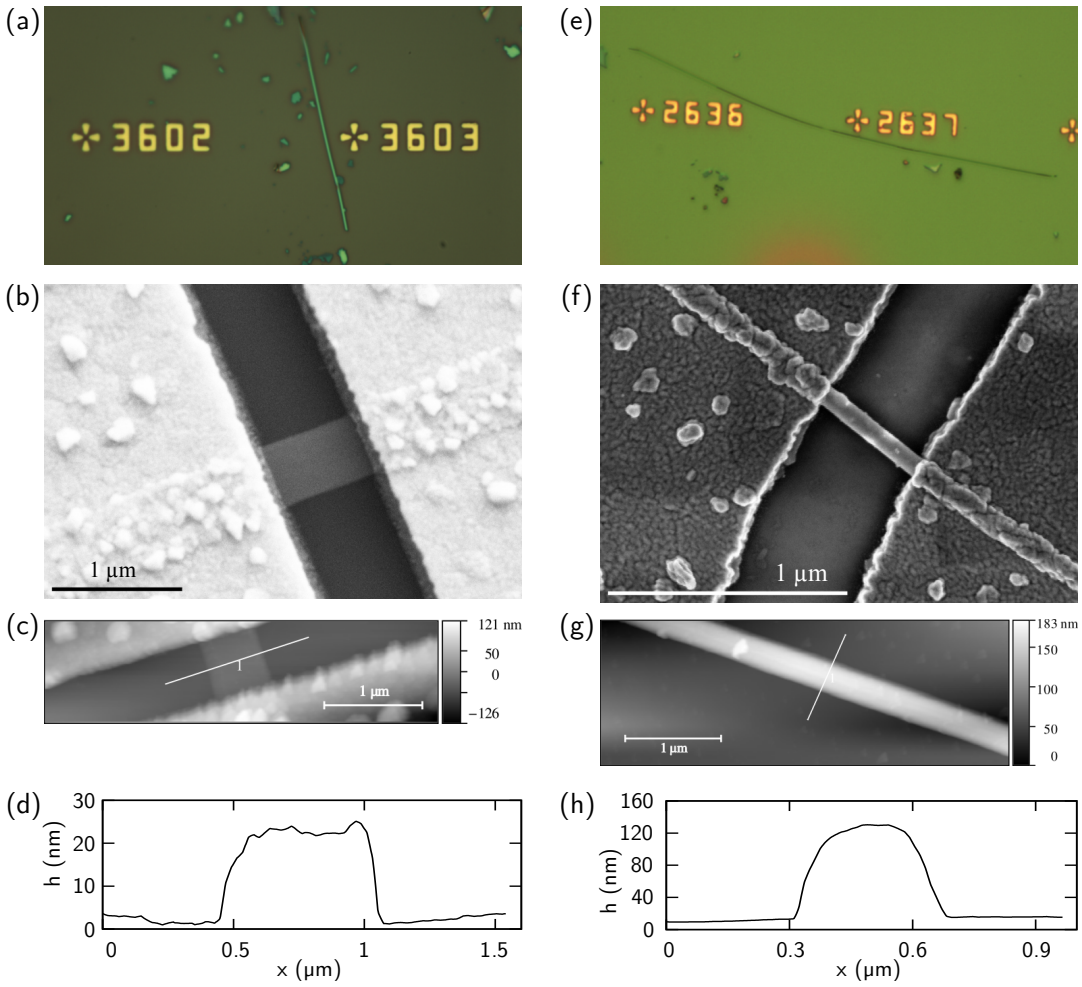


Figure 3.2.: Depicted are micrographs before contact deposition (a, e), SEM images of the finished devices (b, f), and atomic force microscopy (AFM) measurements (e, g) with line traces marked in white and the height along the line trace in (d) and (h), respectively. On the left side a MoS_2 NR on chip 1 (a, b, c, d) and on the right the MoS_2 NT device 2A (e, f, g, h) is depicted. From [Schock et al., 2023].

To distinguish the transferred NTs from NRs, a combination of microscopy techniques can be employed, as illustrated in figure 3.2. After the initial optical image is taken, further SEM and AFM scans are preformed either prior or following the contact deposition. Based on the resulting aspect ratio, the structures can be identified as either NRs or NTs, since the height of a collapsed ribbon is determined by its number of layers. A NT on the other hand might be slightly squashed due to substrate interaction (see figure 2.14), but still has a height in a comparable range to the width. Since the devices investigated here are often comparable in size to, or even

smaller than typical AFM tips, the measured width is overestimated due to the convolution of the device and tip geometries. Therefore, SEM imaging is employed to determine the actual width.

A further distinction becomes possible at larger widths ($w > 50\,\text{nm}$). In this regime, the optical micrograph can already provide an initial indication of whether the device is a nanoribbon or a nanotube. A NR, being essentially flat, can produce thin-film interference with the substrate and thus exhibits colors similar to a 2D flake. By contrast, a NT, owing to its curved cross-section and the absence of extended parallel interfaces with the substrate, predominantly scatters light and appears as a thin dark line (see figure 3.2(a) and (e)).

3.1.2. Contact Deposition

The NT devices were contacted with the following materials: Hf, MgO/Cu, MgO/Au, Cu, Sb, Ti, Bi_2Se_3 and Bi. Deposition of Bi and Ti contacts was performed in an *Orion* ultra high vacuum (UHV) physical vapor deposition system (see figure 3.3), whereas all other metallizations (Hf, MgO/Cu, MgO/Au, Cu, Sb, Bi_2Se_3) were performed in a molecular-beam epitaxy (MBE) system equipped with Knudsen effusion cells at a base pressure below $1 \cdot 10^{-10}\,\text{mbar}$. The MBE depositions were conducted by Dr. Matthias Kronseder. Further details on the individual contact materials are provided in section 5.2.

For material deposition in the *Orion* system, a multiple-crucible linear electron gun (*RCL Series 3 kW Multiple Crucible Linear e-Gun™*, Thermionics Laboratory, Inc.) mounted within the UHV chamber is employed. Typical base pressures lie in the range $5 \cdot 10^{-8}\,\text{mbar}$ to $5 \cdot 10^{-7}\,\text{mbar}$, as measured by an ion gauge. The e-gun provides emission currents up to 600 mA, sufficient to evaporate high-melting-point metals such as tungsten under UHV conditions.

Devices are affixed to mounts using *Marabu fixogum* and loaded upside-down into the load-lock. Pumping for 30 min reduces the pressure below $5 \cdot 10^{-6}\,\text{mbar}$, after which the mount is transferred into the main chamber. An optional *KDC 10 DC Kaufmann ion-beam source* allows in-situ Ar^+ cleaning at variable beam voltages, effectively removing residual adsorbates prior to metal deposition.

Once in the main chamber, the chip temperature can be controlled via a resistive heater of $100\,\Omega$ (monitored by a *THERMA* Type K thermocouple with a *Senseca G1200* thermometer) and a cooling water supply of $10\,^\circ\text{C}$. Additionally, the sample

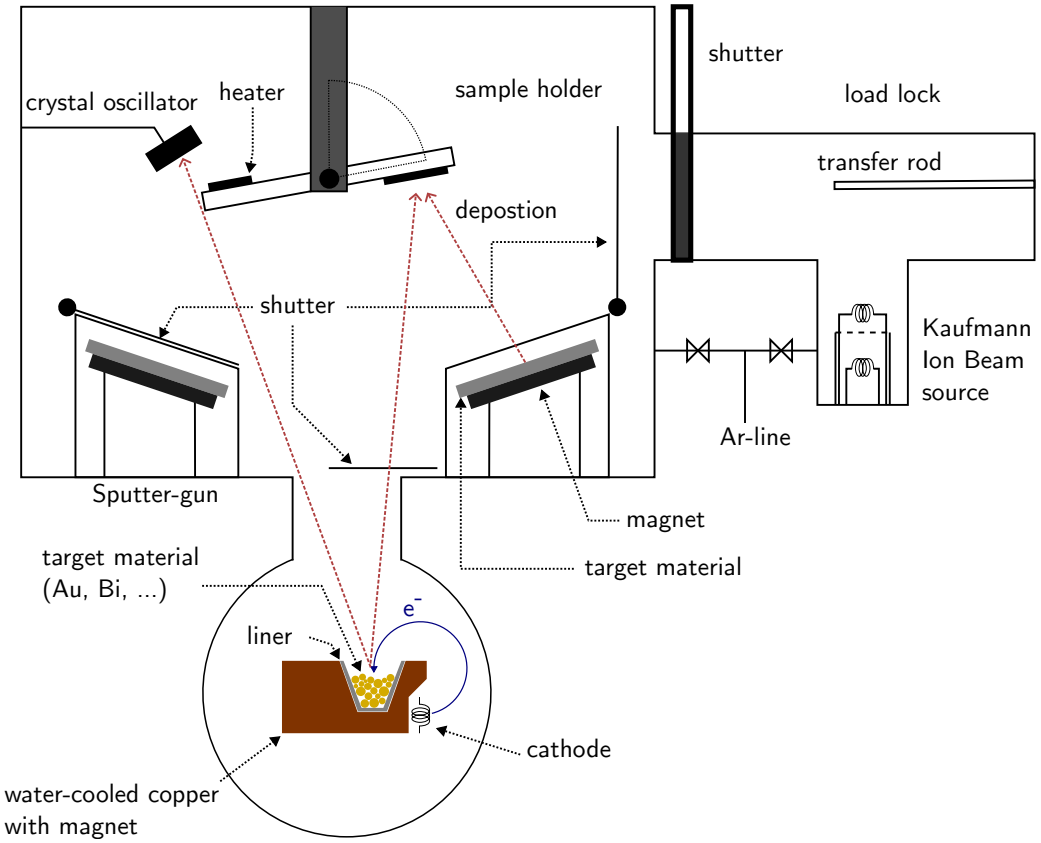


Figure 3.3.: Schematics of the UHV *Orion* metal deposition system. On the right side chips can be transferred into the system through a load lock with a Kaufmann ion beam source for dry Ar^+ pre-etching. At pressures of $1 \cdot 10^{-6}$ mbar the load lock is opened and the chip introduced into the main chamber with the transfer rod. The sample holder in the main chamber can be rotated and heated by applying a current through a mounted resistor. Shutters in front of the electron gun (eGun) and the sputter targets are used to clean the target materials and stabilize deposition rates. A crystal oscillator mounted close to the sample holder is used to monitor the deposition rate.

holder can be rotated in order to change the incident angle of the deposited material. Prior to deposition, titanium (Ti)-gettering can be performed to improve vacuum. Deposition rates are monitored by a quartz-crystal. For bismuth contacts, an emission current of 14 mA is used, which yields a deposition rate of 0.5 Å s^{-1}, for thicknesses in the range of 20 nm to 60 nm. A subsequent gold (Au) cap of 60 nm to 150 nm (rate 0.5 Å s^{-1} to 1 Å s^{-1}) prevents oxidation and provides a low-resistance path to the NT. Deposition angles can be varied between 0°, 10° and 15° to optimise sidewall coverage (full dataset in table A.1). Additionally, the system features a set of sputtering sources, which provide a less directed method of contact deposition compared to electron beam assisted evaporation.
After deposition, the chip is returned to the load-lock, which is then flooded with dry N_2. Lift-off is then performed in hot acetone (1 h to 24 h at just below 60 °C) for PMMA/optical resists, or in Remover PG for lift-off resist (LOR) 3A. Final rinsing in isopropanol and N_2 blow-drying ensures residue-free contacts.

3.1.3. Suspending Nanotubes Between Contacts

The substrate-induced disorder originating from the amorphous SiO_2 surface and surface charges may be reduced by suspending the NT, a procedure well established to improve spectroscopic performance in CNTs [Jarillo-Herrero et al., 2004, Cao et al., 2005]. To achieve this, a first layer of PMMA resist is spin-coated onto the SiO_2 substrate and subsequently cured at $T = 150$ °C prior to the NT transfer. This is then followed, similar to the "normal" *Scotch tape* approach, by gently stamping the NTs with *Nitto* tape onto the baked resist. Compared to the "normal" approach, extra care has to be taken to not scratch the underlying PMMA layer. However, the transfer process is equally effective on the bare oxide and cured PMMA. Subsequently, a second resist layer is applied such that the NTs reside at the interface between both resist films. Following electron-beam lithography and development, the NTs are left suspended at the interlayer height, anchored by the unexposed resist. After deposition of the contact material and lift-off, the NT are freely suspended between the electrodes (figure 3.4).
For the bottom resist, either a 1 % to 4 % solution of PMMA 50k (MW of 50 ku) or 9 % PMMA 200k was used and then spin coated at 8000 rpm. This yielded a thickness of 20 nm to 60 nm, similar to typical NT diameters, and 200 nm for the other resist, respectively. Through the choice of the first resist it was possible to tune the NT–substrate gap. In both cases, the top resist layer was 9 % PMMA 200k.

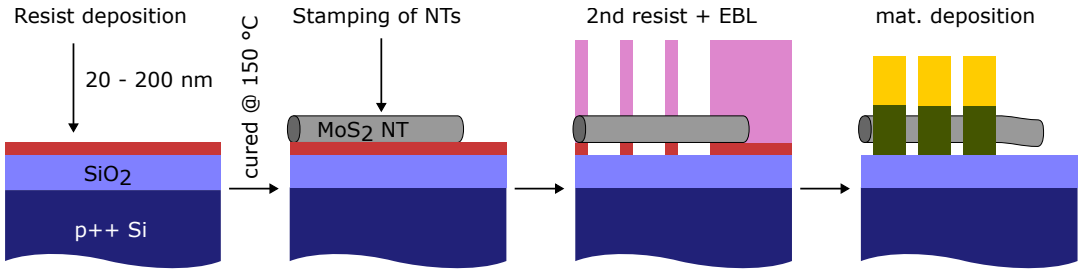


Figure 3.4.: Schematic of the suspension of NTs between contacts. First a thin layer of PMMA is spin-coated onto the SiO_2 substrate and baked at 150 °C. Subsequently, the NT are transferred similar to the *Scotch tape* approach (see figure 3.1) onto the cured PMMA layer, which is followed by a second resist layer, EBL, metallization and lift-off.

A range of metallization schemes were tested for the suspended NTs, including bismuth, antimony, and MgO combined with either copper or gold. The performance of these contact materials is discussed in section 5.2, while the resulting contact morphology and quality are presented in section 5.4. Antimony contacts and those incorporating a thin MgO insulator were deposited in the MBE system using Knudsen cells (see section 3.1.2). This was followed by second evaporation in a different e-Gun system in order to cap the layers with a 80 nm thick gold layer.
For bismuth contacts, initial deposition parameters used 30 nm to 40 nm of bismuth (Bi) and 40 nm to 100 nm of Au. However, after observing the formation of nanogaps (section 5.4), the procedure was modified to employ consistently thicker layers (40 nm Bi and 100 nm to 150 nm Au) together with angled evaporation at ±15° relative to the substrate normal.

3.1.4. Nanotubes on Heterostructures

An alternative approach to reducing substrate-induced disorder, compared to the suspension of NTs between contacts, is the replacement of the amorphous SiO_2 substrate and the p++ doped Si back gate with a material of higher crystallinity. Suspension merely increases the separation from the disordered SiO_2, whereas crystalline substrates can eliminate its influence entirely. A straightforward option would be a gold substrate coated with epitaxially grown Al_2O_3, providing an atomically flat and inert surface [Yang et al., 2017, Li et al., 2019]. However, recent advances in the field of nanomaterials have demonstrated that 2D materials themselves, such as hBN and FLG, can serve as crystalline substrates and dielectric layers

of exceptional quality. Studies on bilayer graphene and related heterostructures have consistently shown that such layered systems suppress substrate-induced disorder and yield highly uniform electric fields [Engels et al., 2013, Li et al., 2017, Banszerus et al., 2018, Eich et al., 2018, Overweg et al., 2018]. Different transfer techniques were developed for both the 2D base stack and the placement of NTs, as described in the following sections.

All heterostructures were assembled on Si/SiO_2 chips pre-patterned with metallic alignment markers and bond pads. Two types of chips were used. The first type featured Cr/Au markers separated by 50 µm, which served as references for the Scotch-tape transfer technique. The second type, fabricated specifically for this work, employed Ti/Au markers and recessed bond pads embedded within the SiO_2 layer. The embedding of the metal structures provided a planar surface that improved adhesion of the subsequently transferred 2D crystals, which tend to delaminate at step edges or surface irregularities.

For fabrication, the bare Si/SiO_2 substrates were spin-coated at 8000 rpm with LOR 3A and the optical resist *S1805*, followed by baking at 120 °C for 4 min and 1 min, respectively. Lithography was carried out using a *Heidelberg Instruments µMLA* maskless aligner, and developed in *MF26A* (*Megaposit*) for 45 s, followed by rinsing in deionized water for 20 s.

Material deposition was performed in the *Orion* UHV system (figure 3.3). Prior to metallization, the substrate surface was dry-etched with Ar^+ ions to a depth of 35 nm in order to recess the gold layer slightly into the SiO_2. This ensured that the final metal surface was level with the surrounding oxide, minimizing topographic steps and facilitating the adhesion of 2D materials. The etching was carried out at $p_{Ar} = 3 \cdot 10^{-3}$ mbar with a beam voltage of 450 V, a beam current of 10 mA, and a duration of 66 s. A 3 nm Ti adhesion layer was then deposited at a rate of $0.3\,\text{Å}\,\text{s}^{-1}$, followed by 32 nm of Au deposited at $1\,\text{Å}\,\text{s}^{-1}$. Liftoff was carried out in hot *remover PG*, followed by rinsing in acetone and isopropanol, and final drying with a N_2 jet.

Polydimethylsiloxane Transfer

Polydimethylsiloxane (PDMS) is a silicon-based polymer extensively employed in two-dimensional material research both as a support and as a transfer medium [Castellanos-Gomez et al., 2014, Dong et al., 2024]. Its pronounced flexibility and viscoelastic response facilitate the deterministic relocation of atomically thin flakes (and NT) between disparate substrates. In the present work, PDMS

served to transfer quasi-2D hBN and FLG onto Si/SiO_2 chips patterned with Ti/Au or Cr/Au features. These flakes function as highly conductive back gates and crystalline gate dielectrics devoid of dangling bonds. As exfoliation of 2D materials with PDMS relies on a strong interaction between the material to be exfoliated and the substrate during the release step, MoS_2 NTs could not be transferred; the soft PDMS engulfs the round shape of the NTs and sticks much stronger to them.

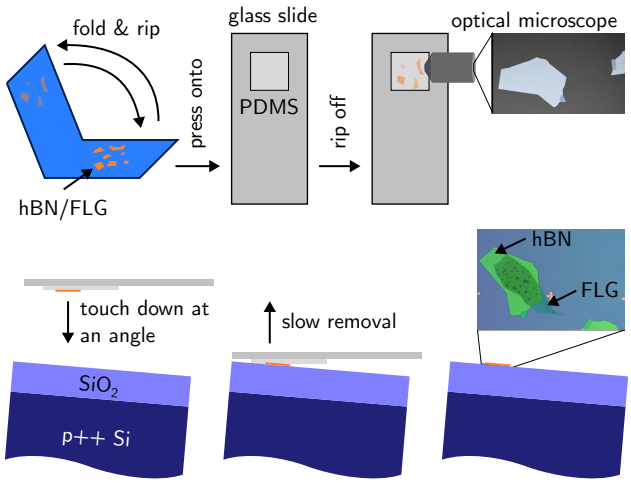


Figure 3.5: Schematic of the PDMS transfer method for deterministic placement of FLG and hBN flakes. A Nitto tape strip is pressed onto the bulk crystal, folded and peeled repeatedly to exfoliate thin flakes. A PDMS stamp of approximately 1 cm × 1 cm is then brought into contact with the tape and lifted to pick up the flakes. Individual flakes are identified by optical microscopy and transferred onto a SiO_2/Si substrate.

Exfoliation begins by pressing a *Nitto* tape strip onto the bulk crystal of interest, thereby transferring a thin lamella of the 2D material (see figure 3.5). The tape is then folded and peeled apart multiple times (typically ≤ 10 cycles) to delaminate thinner stacks and monolayers. A 1 cm × 1 cm PDMS film (*Gelpak Gelfilm*) affixed to a glass slide is pressed onto the tape and rapidly peeled away, capturing selected flakes on its surface. Using optical microscopy, candidate flakes are identified by size and thickness. Finally, the PDMS stamp is aligned over the target SiO_2 substrate, brought into conformal contact, and slowly peeled off, leaving the chosen flakes in a pre-planned position.

Repeating this process twice, first with graphite source material for a FLG back gate and then with hBN for a clean dielectric layer, a heterostructures is created. In the next sections, different methods for transferring NTs onto this stack will be presented.

Polycarbonate transfer

It has been shown, that residues from PDMS contaminate transferred material, which can strongly alter the electronic and optical properties of the transfer nanomaterials [Jain et al., 2018, Schwartz et al., 2019, Otsuka et al., 2021]. Therefore, an enhanced version of the PDMS transfer process introduces a Poly-Carbonate (PC) "buffer" between the PDMS stamp and the target nanostructure, thereby enabling precise placement of MoS_2 NT or 2D flakes while minimizing contamination.

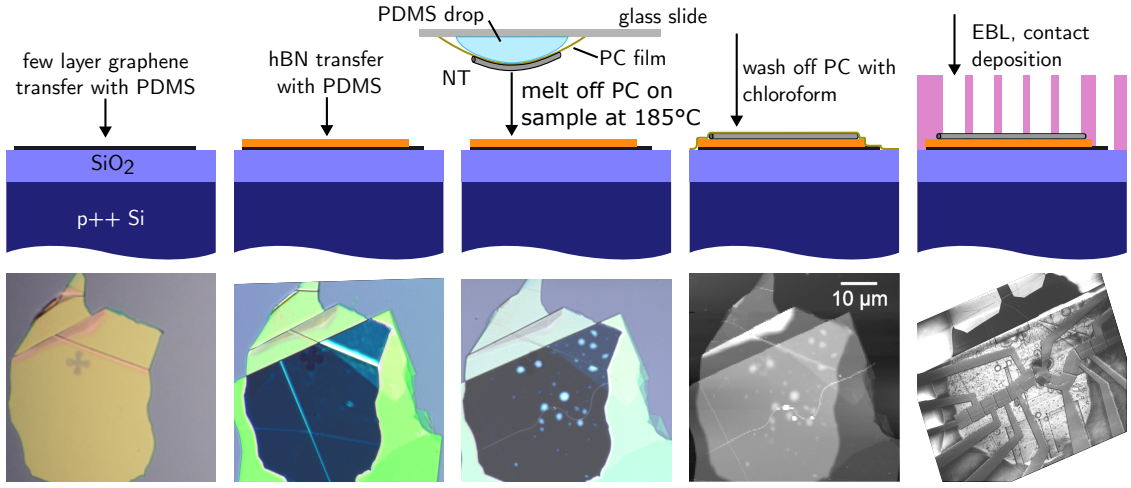


Figure 3.6.: Schematic of the PC–assisted transfer workflow (upper row) with images taken at each step of the process (lower row, first three optical, fourth AFM, and last SEM). First, FLG and hBN flakes are stacked via the PDMS method (see figure 3.5). A thin PC film strip is then laid onto a PDMS droplet mounted on a glass slide. Using an XYZ stage, a NT is picked up from a Si wafer prepared by the *Scotch tape* exfoliation (see figure 3.1) and pressed onto the FLG–hBN heterostructures. The PC layer is melted at 185 °C on the chip surface, thereby fixing the NT on the heterostructure. Finally, the PC layer is dissolved in chloroform, while the NT remains in place due to the van-der-Waals interaction. This is followed up by standard electron-beam lithography and metallization. From [Schock et al., 2024].

In the first step, a 4 % PC solution in chloroform is used to coat a glass slide. It is subsequently air-dried to yield a thin PC film. This film is then peeled off using adhesive tape featuring a central aperture. Next, the PC–tape assembly is stretched over a preformed PDMS droplet on a secondary glass carrier, creating a composite stamp whose exposed PC surface interfaces with the nanodevice. By pressing the PC-coated droplet against a substrate, previously prepared using the

Scotch tape method (see section 3.1.1), a NT (or flake) can be picked up (see figure 3.6). After contact, the setup is heated to 130 °C and the PC/PDMS-stamp is retracted slowly, while the nanomaterial adheres to the PC layer. The entire stack (PDMS/PC/nanomaterial) is then aligned over the target substrate, carefully brought in contact with the predefined heterostructures (see figure 3.5), heated to 185 °C to melt the PC, and lifted away, leaving the PC-encapsulated NT in place. A final 15-minute wash in hot chloroform removes the PC, yielding a clean, uncontaminated transfer.
Compared to PDMS-only stamping, this method (i) succeeds even when the material affinity for PDMS exceeds that for the receiving surface, and (ii) eliminates residual PDMS contamination by dissolving the interfacial PC along with any adhering oligomers.

Anthracene transfer

Unfortunately, even PC was demonstrated to leave behind contamination after the transfer process [Schwartz et al., 2019]. Therefore, an alternative transfer agent, namely anthracene crystal, was also employed. This process enabled measurements of transferred CNT with optical properties comparable to as grown NTs [Otsuka et al., 2021]. This is possible since anthracene, unlike PC, sublimates cleanly under mild heating, eliminating the need for wet chemical removal. Moreover, its crystalline rigidity ensures a stable yet reversible adhesion to both the PDMS carrier and the target nanomaterial, making it particularly advantageous when even trace organic residues could compromise device performance or when subsequent processing steps demand atomically pristine interfaces.
The transfer sequence (figure 3.7) begins with the vapor-phase growth of large, single-crystalline anthracene platelets on glass slides held $\approx 1\,\mathrm{mm}$ above a bed of granular anthracene heated to 80 °C in air. Following Otsuka et al., black masking lines are drawn with a permanent marker of type *STADEDLER permanent Lumocolor S, NR 313-9*, which produced results similar to the permanent marker used by Otsuka et al. *KOKYUO PM-41B* that was not available here. The lines on the slide surface direct crystal nucleation from adjacent unmarked regions into the masked area, yielding platelets $\approx 1\,\mathrm{mm}^2$ in area and only few microns thick (figure 3.7 left images). After $\approx 12\,\mathrm{h}$ of growth, candidate crystals are identified under an optical microscope and lifted intact by gentle contact with a PDMS droplet. The droplet–anthracene composite is then aligned over an isolated NT or flake on SiO_2

substrate, which was previously prepared by the *Scotch tape* method (section 3.1.1). Then the stack is pressed onto the NT and subsequently heated up to $T > 80\,°C$ to strengthen interfacial adhesion between the anthracene crystal and the to be transferred material. Finally, the stack is peeled away in under one second—ensuring preferential binding of anthracene to PDMS over the oxide substrate.

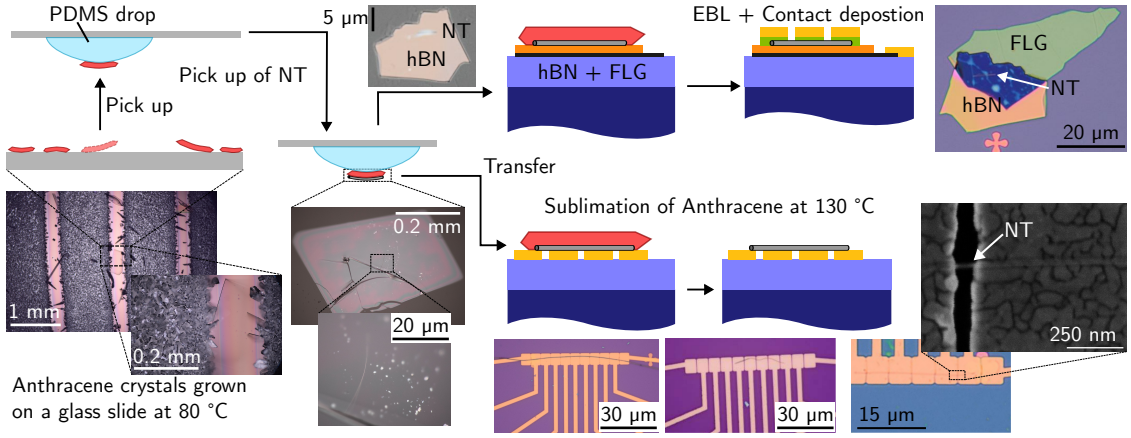


Figure 3.7.: Schematics of the anthracene assisted transfer process. The large anthracene crystals are grown on a glass slide with marker stripes at 80 °C [Otsuka et al., 2021]. Using a PDMS droplet on a glass slide, a large area anthracene crystal is picked up from the marker region. With this anthracene/PDMS stamp a NT or 2Dflake, previously exfoliated with the *Scotch tape* method (see figure 3.1), is picked up. Then, these can either be placed onto a heterostructures (upper part) or placed onto predefined contacts (lower part). The crystal/NT stack is pressed onto the chip, heated to temperature above 90 °C to enhance interfacial adhesion between the anthracene and SiO_2 substrate, and the PDMS stamp is slowly ($\approx 5\,$min) peeled off, leaving the anthracene/NT stack behind. Finally, sample is heated above 130 °C sublimating the anthracene crystal and leaving the NT on the device. From [Schock et al., 2024].

For deposition, the PDMS/anthracene/nanomaterial stack is precisely positioned above the receiving chip and pressed down at T > 90 °C to promote transfer of the anthracene plate and the adhered nanotube/flake onto the target location. The subsequent slow retraction of the PDMS ($\approx 1\,$min) leaves the crystal bearing the nanotube atop the substrate with minimal mechanical disturbance. Finally, a brief anneal at $T > 130\,°C$ induces anthracene sublimation in ambient atmosphere, yielding a clean, residue-free heterostructures ready for contact metallization or encapsulation (figure 3.7 upper part).

This all-dry, solvent-free protocol not only preserves fragile NTs and 2D flakes against capillary forces if placed on trenches [Otsuka et al., 2021] but also integrates seamlessly with prepatterned contacts, provided their surface chemistry does not form an insulating oxide barrier (figure 3.7 lower part).

3.1.5. Enhanced Contact Strategy

Despite the already mentioned advantages of heterostructures in terms of reduced disorder, the methods described above share one major disadvantage compared to the "classical" *Scotch tape* method: Only a single NT can be transferred per process. As discussed later (see section 5.2), even materials exhibiting excellent contact properties are found to show a large variation in resistance per contact pair, including cases with multiple contacts on a single NT. This is especially cumbersome, as an experimentally derived threshold in the order of at most a few MΩ has to be met for devices to still be measurable at cryogenic temperatures.
In section 5.4, it will be shown that most contacts exhibiting very large resistances originate from nanogaps between the contact material covering the NT and the surrounding material. To enhance contacting efficiency and achieve more reliable contacts, the contact definition and deposition techniques were further refined.
As a first step, a prior EBL process is performed before the lithographic step for the contact structure definition shown in figure 3.8. Again a roughly 200 nm thick layer of PMMA 200k 4 % is used, which is overexposed by a factor of ≈ 20 (corresponding to a dose of $50\,\mathrm{mC\,cm^{-2}}$) in small ($\leq 50\,\mathrm{nm}$) circular regions intersecting the NT. This high dose not only breaks the bonds in the polymer chains but also rebuilds a network of covalently bound polymers, a process known as *crosslinking*. With hot acetone (just below 60 °C) the resist is "developed" for 16 h by removing the remaining resist, which was not crosslinked. The result is a "dome" or spot effectively welding the NTs to the substrate surface (figure 3.8(c)) as well as creating a smooth path between any material later deposited on the NT and the substrate.
After a second EBL process, following the description in section 3.1.1, contact deposition is performed. Compared to the processes before, this was adapted in the following way:

- The samples were kept inside the main chamber at elevated temperatures $T = 100\,^{\circ}\mathrm{C}$ for more then 12 h to out-gas the surfaces. Together with a Ti-getter pumping step prior to material deposition this ensured pressures

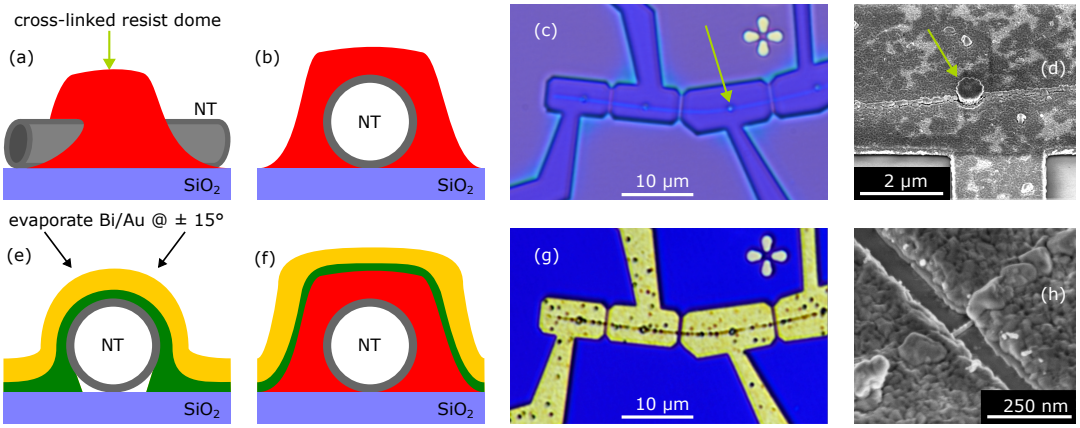


Figure 3.8.: Schematics of the enhanced contact process with *crosslinked* resist. After NT transfer by any of the above techniques (*Scotch tape*, PC-transfer, or anthracene transfer) the resulting NT is spin-coated with PMMA which is exposed to a high dose of $50\,\mathrm{mC\,cm^{-2}}$ to create a crosslinked dome which intersects the nanotube (a), (b), and (c). Contact deposition is additionally performed at elevated temperatures of 100 °C and at two different incident angles (15° and −15°) (e). Together with the crosslinked dome, the resulting contact material spans the gap between material on the substrate and the NT (see figure 5.7), schematically shown in (e) and (f). Device 3A is shown after *crosslinking* and lithography (c), and metallization (d), (g) and (f).

during the actual deposition of $5 \cdot 10^{-8}$ mbar, which is an almost an order of magnitude lower than before. It was shown that Ni-contacts to planar MoS_2 were very sensitive to the pressure, with contacts deposited in UHV conditions performing significantly better then comparable contacts from only high vacuum conditions [Sun et al., 2024]. Sun et al. did not observe a similar effect for Bi contacts, but a reduced pressure and thorough removal of surface moisture might still be beneficial.

- During deposition, the sample holder temperature was kept at 100 °C. This could enhance mobility of the adsorbed Bi atoms leading to better match between crystal structures. On samples produced prior to this enhanced scheme, a very grainy growth of the Bi/Au-layer was always observed (figure 5.7). Therefore, the higher mobility could potentially improve the overall structure of the contact layer. Figure 3.8(h) shows a region where no grain has grown on top of the contacted NT, indicating an improved growth which fully incorporates the tubular geometry.

- As a final addition, both Bi and Au layers were deposited at two angles 15° and −15°, switching after deposition of half the desired layer thickness (figure 3.8(e)). As it is indicated in the schematics, the angled incidence of the deposited material should prevent the formation of nanogaps caused by a top down deposition process.

Finally the chips are left in UHV conditions until cooling down to room temperature before exposure to ambient conditions. This processes is then followed by typical lift-off process in hot acetone for over 1 h.

3.2. Measurement

In this section, a comprehensive overview is provided of the electrical characterization techniques employed to evaluate the MoS_2 NT devices. The discussion begins with room-temperature measurements, where two-terminal resistances are established as indicators of contact quality and overall transport behavior under ambient conditions. Building on these results, device performance is examined at low temperatures using a 1 K dip-stick cryostat to verify contact transparency. Finally, the investigation is extended into the millikelvin regime within a dilution refrigerator, where CB measurements are conducted on QDs confined within the NT devices. All measurements were automated using Perl and *Lab::Measurement* [Reinhardt et al., 2019].

3.2.1. Room Temperature Characterization

As an initial step in evaluating the contact quality of the devices, the two-terminal resistance at room temperature is measured between adjacent contact pads. In the probe station (figure 3.9(a)), the chip is secured by a vacuum pump, and metallic needles mounted on micro-manipulators are brought into electrical contact with the bond pads connected to each nanotube electrode in succession. A constant source–drain bias V_{SD} in the range of 1 mV to 10 mV is applied using a *Yokogawa GS200*, and the resulting current I_{SD} is recorded. Current amplification is performed with an *Ithaco 1211* (gain set from $1 \cdot 10^{-6}\,\mathrm{V\,A^{-1}}$ to $1 \cdot 10^{-9}\,\mathrm{V\,A^{-1}}$, rise time 100 ms), and the amplified voltage is read out using an *Agilent 34401A* multimeter. Where required, the Si back-gate or FLG gate is biased with a *Yokogawa 7651* source as shown in figure 3.9(b).

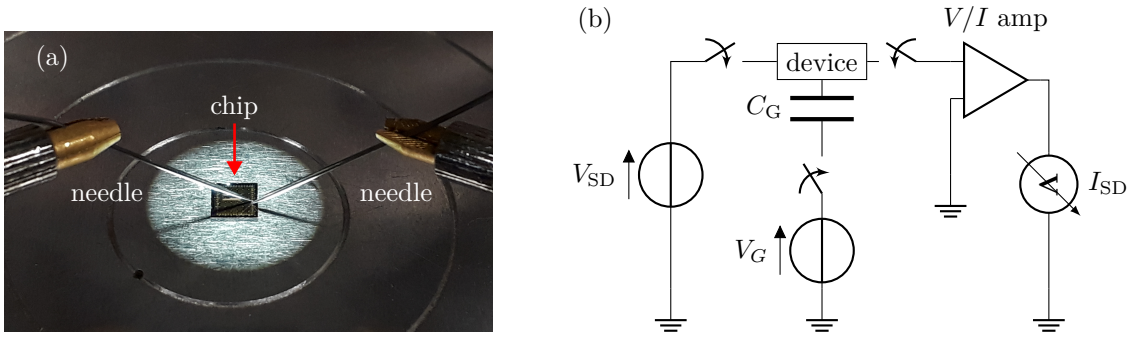


Figure 3.9.: (a) Image of the *point-probe* station used to determine the room temperature resistance. (b) Circuit diagram of a typical two point resistance measurement at room temperature performed with the *point-probe* station. A constant bias voltage $V_{SD} = 1\,\text{mV}$ to $10\,\text{mV}$ is applied, usually with a *Yokogawa GS200* voltage source, through one of the needles (indicated with a switch). The resulting current is then amplified with an *Ithaco 1211* current amplifier with an amplification of $0.1\,\text{V}\,\text{nA}^{-1}$ to $100\,\text{V}\,\text{nA}^{-1}$. The resulting voltage is then measured with a multimeter (*Agilent 34401A*). An optional gate voltage V_G can be applied using a *Yokogawa 7651*.

Because the two-terminal resistance of each device is dominated by the Schottky barrier, in case of high barriers, it serves as a straightforward metric for contact quality. Nevertheless, to more rigorously decouple the contact resistance from the channel resistance, additional four-terminal measurements are performed on devices fabricated using the crosslink scheme (section 3.1.5). In this configuration, the bias is applied to the first contact, the voltage drop across the inner contacts is measured with a second *Agilent 34401A* multimeter, and the current at the fourth contact is determined using the same amplification setup described above. This four-terminal approach allows to determine whether the contact-engineering strategies employed here truly minimize parasitic resistances and to guide future improvements in device fabrication.

If the room temperature resistances are below or in the few MΩ regime, the chips are glued into a twenty pin chip carrier using *Epoxy Technology H20E* conductive silver epoxy. By covering one pin of the chip carrier with the epoxy, the highly doped Si is connected to be used as a back gate. After a bake out for 1 h to 12 h at 50 °C to 100 °C, the glue has hardened and the best contacts of NTs are bonded to the chip carrier with a *West Bond model 5400B* aluminum wire bonder.

3.2.2. 1 K Dip-Stick Cryostat

In order to rapidly screen device functionality before a full dilution-refrigerator cooldown, a 1 K dip-stick cryostat is emplyod. This can be cooled down from room temperature in about two hours via evaporative cooling of liquid ^{4}He (see figure 3.10) opposed to the several hours to days in a full dilution-refrigerator. First, the internal vacuum seal is pumped to high vacuum conditions ($1 \cdot 10^{-4}$ mbar) to ensure thermal decoupling between the 1 K pot and the helium bath and remove excess moisture. The dip-stick is then inserted into a liquid helium can and the 1 K pot pumped to a few millibars to drive evaporation there. Under continuous flow, regulated by a fine needle valve, the pot stabilizes at $T_{\mathrm{pot}} \approx 1.3\,\mathrm{K}$. Alternately, by closing the inlet after letting the pot fill completely, a "single-shot" mode achieves $T_{\mathrm{pot}} \approx 1.2\,\mathrm{K}$ for several hours without active pumping. A thin-film RuO_2 resistor mounted on the pot provides accurate temperature monitoring, and a 50 Ω heater allows controlled heating.

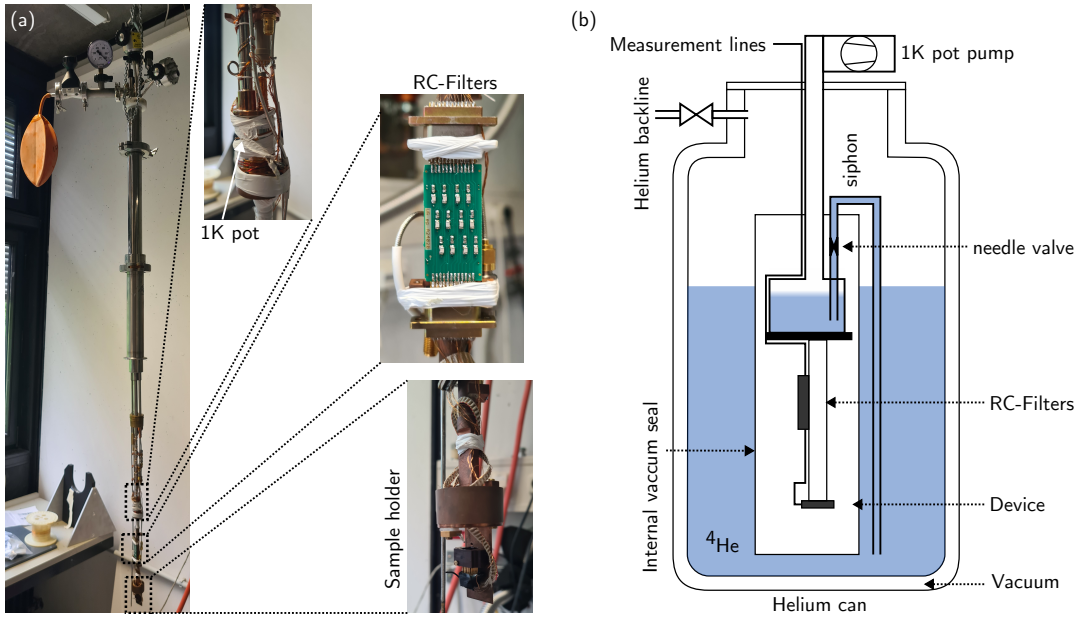


Figure 3.10.: 1 K dip-stick cryostat from *ICE Oxford*. (a) Images of the dipper with zoomed-in views on the 1 K pot itself, the RC-filters, and the direct current (DC) sample holder. (b) Schematics of the dipper, showing the working principle. The dip-stick is lowered into a liquid ^{4}He can, where a siphon is used to suck helium into the 1 K pot. There it evaporates at mbar pressures provided by a rotary pump, reaching temperatures of roughly 1 K.

Thermal anchoring and electrical filtering are critical to maintain low noise and minimize heat leaks. Twenty 100 µm thick copper lines run from the room temperature down the dipper shaft, each thermally anchored at 4 K flange and again at the 1 K pot using RC-filters ($R = 1.2\,\mathrm{k\Omega}, C = 27\,\mathrm{nF}$) with a cutoff frequency of 5 kHz. These ensures low-noise measurements and protect the samples from high frequency noise, which seemingly destroyed several devices in the system prior to installing the filters. At the room temperature side, a setup comparable to the needle station is used to conduct CB measurements (see figure 3.9(b), but with a *Keithley 2400* source-measure-unit as the gate voltage source).

3.2.3. Dilution Refrigerator

In this work all measurements performed at temperature below 1.2 K were performed in a dilution refrigerator *Trition System* from *Oxford Instruments*. A schematic of the system can be seen in figure 3.11 and some photographs of the system can be found in the Appendix (figure A.2).
A dilution refrigerator exploits the quantum statistical properties of ^{3}He/^{4}He mixtures to attain temperatures down to a few mK. At its heart lies a continuous-cycle heat engine based on the endothermic mixing of ^{3}He into a ^{4}He rich phase. Below about 0.87 K, a liquid mixture of ^{3}He and ^{4}He separates into two immiscible phases: a concentrated ^{3}He–rich phase and a dilute phase of mostly ^{4}He with a small ^{3}He fraction. When ^{3}He atoms cross from the concentrated into the dilute phase, they absorb heat, thus providing the refrigerator's cooling power. This endothermic mixing is continuous, as long as one maintains circulation of ^{3}He through the system. The "stil", a volume at around 0.6 K to 0.8 K which contains the liquid surface is pumped to remove ^{3}He preferentially from the dilute phase via evaporation. The extracted ^{3}He gas then passes through the pumps and a series of cold traps (nitrogen and helium) in order to be purified from any gas, that has leaked into the room temperature pipes, to prevent the formation of a blockade. It is then condensed and re-liquefied at the 1 K pot, which is cooled by evaporating the ^{4}He from the helium bath, similar to the 1 K dip-stick (section 3.2.2). The liquid ^{3}He passes a series of counterflow heat exchangers, where it is precooled against the returning cold mixture, and impedances in order to generate a precisely calibrated flow. Finally, the ^{3}He enters the mixing chamber, the coldest point ($\approx 10\,\mathrm{mK}$ for this system), where it rejoins the dilute phase and cooling takes place. A detailed description of the underlying physics can be found in [Enss and Hunklinger, 2005].

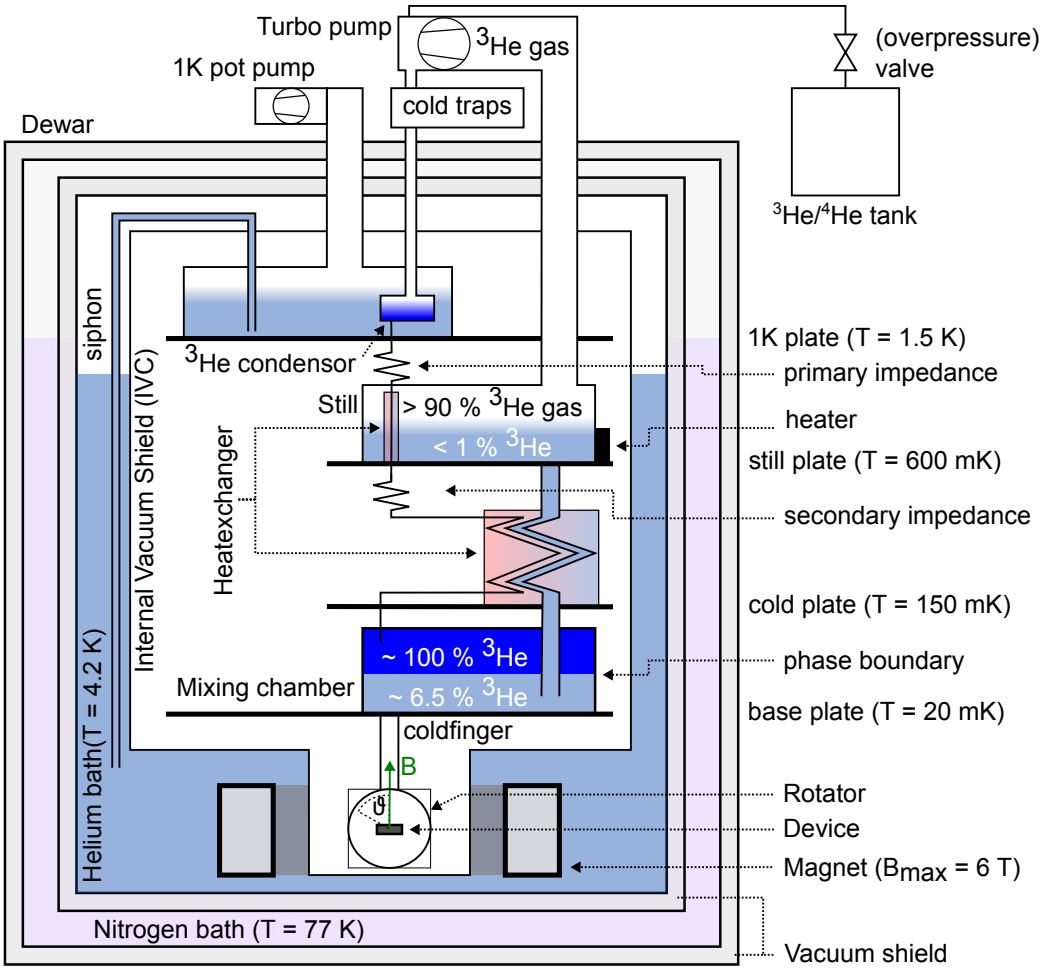


Figure 3.11.: Schematics of a dilution refrigerator similar to the *Oxford Instruments Kelvinox 400HA*, which was used in this work. The dilution system itself is lowered into a cryogenic dewar filled with liquid ^{4}He. Inside the helium bath a superconducting magnet can reach up to 6 T in vertical direction (green arrow). Similar to the 1 K dip-stick (see section 3.2.2), a siphon is used to suck ^{4}He into a evaporation chamber (1 K pot), where helium is pumped in order to achieve temperatures of ≈ 1.5 K. This is used to precool the ^{3}He in the condensor into a liquid, which is then further cooled in additional heat exchangers and slowed down by the two impedances. Inside the mixing chamber the ^{3}He is channeled into the concentrated phase. The actual cooling takes place as ^{3}He transitions into the diluted phase in order to keep a constant concentration; there, ^{3}He is removed from the diluted phase continuously via the under-pressure in the still and recycled through the condensor.

3.2.4. Base Temperature Measurement Setup

Measurements inside the cryostat are performed with the chip attached to the coldfinger, where it resides in the center of the magnet coil and potentially its field (see figure 3.11). It is mounted either to a static holder, with the field perpendicular to the substrate plane, or on an *attocube systems ANRv51* rotator, where the substrate plane is parallel to the field and can be tilted along the normal axis on the plane. The rotator was installed towards the end of this thesis and therefore most measurements with magnetic field were performed in the out-of-plane direction.

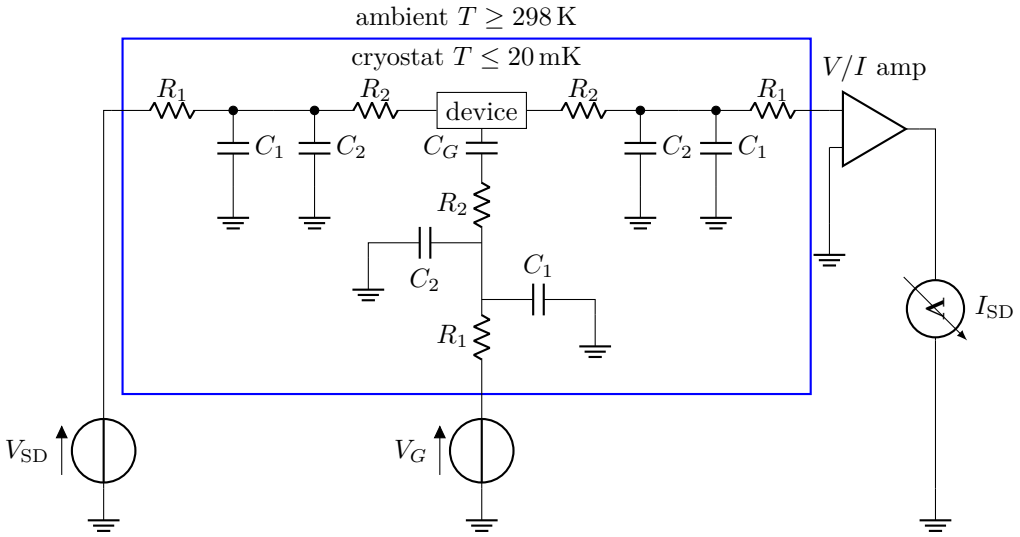


Figure 3.12.: Circuit diagram of the low temperature measurement setups. The blue rectangle marks the part of the circuit which is connected to the base plate of the cryostat. From left a bias voltage V_{SD} is applied through a double RC-filter with $R_1 = 1.21\,\mathrm{k\Omega}, R_2 = 0.825\,\mathrm{k\Omega}, C_1 = C_2 = 27\,\mathrm{nF}, f_{\mathrm{cutoff}} \approx 5\,\mathrm{kHz}$ to the connected NT device. The other other terminal of the NT is similarly connected to a low-pass filter and the current is converted at room temperature by an *Ithaco 1211* current amplifier to a voltage that is read by a *Keysight HP3458A* multimeter. A voltage V_G is applied to the gate of the of the devices through the same set of RC-filters.

The contacts on the chip are connected via twenty DC lines, which are, similar to the setup in the 1 K stick, filtered at the mixing chamber with two RC-filters ($f_{\mathrm{cutoff}} = 3\,\mathrm{kHz}$) in series each (see figure 3.12). Again, these ensure a good thermal anchoring and reduce high frequency noise. After that, the lines are thermalized on each stage of the cryostat through physical contact between the outer isolation and the copper rods attached to each stage. At room temperature the setup is either similar to the one used for the 1 K-dipper (a *Yokogawa GS200* as bias source,

Keithley 2400 as gate source, and a *Keysight HP3458A* as multimeter after an *Ithaco 1211* amplifier) or the voltage sources and multimeters are replaced by a *nanonis Tramea*. This device combines eight voltage sources and eight multimeters and gives a large speed enhancement (2× compared to the previous setup) during measurement owing to the internalized device communication.

4. State of the Art Regarding TMDC Quantum Dots

In section 2.4.6, the fundamental constraints on realizing QDs in TMDCs were established. The large effective carrier masses (table 2.1) demand device dimensions at the nanometer scale, approaching the limits of state-of-the-art lithography. Additionally, the intrinsic semiconducting nature of MoS_2 requires meticulous contact engineering to prevent the formation of excessive Schottky barriers. This chapter gives a review on recent fabrication and measurement breakthroughs in TMDC QDs, identify the prevailing obstacles, and outline the strategies that will be pursued throughout this thesis to overcome them.

4.1. Planar MoS_2 Based QDs

In recent years considerable effort has focused on achieving electrostatic confinement and observing CB in planar TMDC devices. Early work by [Lee et al., 2016] employed the low work function metal zinc as contacts to overcome Schottky barriers, successfully defining a QD between source and drain and measuring classical CB oscillations [Lee et al., 2016]. Similar classical regimes were realized in WSe_2 and WS_2 by [Song et al., 2015a] using palladium/Au contacts, finger gates, and an Al_2O_3 dielectric [Song et al., 2015a, Song et al., 2015b]. [Lau et al., 2022] further reduced the dot size to a radius of 58 nm in bilayer WS_2 by incorporating a high-k HfO_2 layer beneath Au gates, attributing their size reduction to enhanced field penetration [Lau et al., 2022]. More recently, [Tataka et al., 2024] used Au finger gates and the Schottky barrier formed at the Au-MoS_2 interface to create 30 nm-scale QDs in Bi/Au contacted monolayer MoS_2, where disorder-dominated blockade was observed [Tataka et al., 2024].

Alternative confinement has been achieved at defects, enabling transport in the single level regime. [Devidas et al., 2021] performed excited-state spectroscopy on

MoS_2 QDs formed at point defects, extracting a Landé factor $g \approx 1.7$ consistent with vacancy localization [Devidas et al., 2021]. In four-layer WS_2 devices contacted with platinum, [Papadopoulos et al., 2020] measured g-factors of several Coulomb oscillations (3.4 ± 0.9, 15.8 ± 1.8 and 11.0 ± 0.9) and small confinement in the order of 10 nm, concluding that these large Landé factors can only arise if orbital moments dominates. [Krishnan et al., 2023] reported Coulomb peaks from a QD of 1.9 nm to 4.1 nm radius in MoS_2, deducing perpendicular $g_{1,\perp} = 2.2 \pm 0.2$ and $g_{2,\perp} = 8.1 \pm 0.2$ as well as parallel $g_{1,\parallel} = 0.6 \pm 0.1$ and $g_{2,\parallel} = 0.7 \pm 0.2$ for two different Coulomb peaks. Additionally, a sulfur-vacancy confinement was identified from g-factor anisotropy and inter-valley mixing estimates [Krishnan et al., 2023]. Despite these astounding results, the actual confinement in these works is independent of the intended lithographic potential, relies on the existence of defects, and is not reproducible.

Recently, notable exceptions have demonstrated single-level transport in lithographically defined QDs. While this thesis was still in preparation, [Davari et al., 2020] reported reproducible confinement of QDs in mono- and bilayer WSe_2 using platinum contacts and Au/hBN finger gates. The reported QD diameters were in the range of 10 nm to 30 nm, which is of the same order of magnitude as the design diameter of 80 nm to 100 nm close to the lithographic resolution limit. Single-level transport was confirmed, and Landé factors between 0.8 to 2.4 were extracted [Davari et al., 2020]. Around the same time, [Kumar et al., 2023] succeeded in creating QDs not at point defects but most likely at device inhomogeneities in hBN-encapsulated MoS_2. Clear excited-state lines and the temperature dependence of the peak height confirmed single-level transport. Magneto-transport measurements revealed a Landé $g \approx 5.2$ [Kumar et al., 2023]. These results highlight the extreme lithographic precision required to reach the single-level regime in TMDC materials.

4.2. QD in Nanotubes and Etched Nanoribbons

These examples underscore the intrinsic difficulties in achieving clean, controllable confinement in planar TMDC systems. The formation of small enough QDs, required by the large effective masses, is fundamentally constrained by lithographic limitations and weak dielectric screening. As a result, QDs are predominantly confined by defects or sample inhomogeneities, both of which lack reproducibility and tunability. Therefore, different approaches have been explored, such as etched NRs and quasi-one-

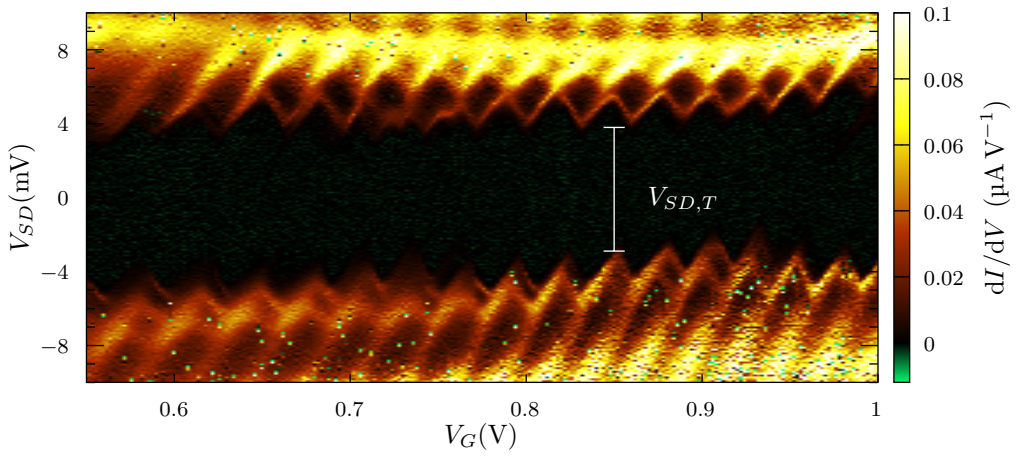


Figure 4.1.: Low temperature transport measurements of a MoS_2 NT contacted with scandium (latter referred to as a *type-I* contact material, see section 5.2). The typical structure of CB are clearly visible and discrete lines indicate single level transport. However, there is a large gap between the upper and the lower part of the CDs marked with $V_{SD,T}$. Adpated from [Reinhardt, 2019].

dimensional structures like NTs, which may offer better-defined boundary conditions and more robust confinement.

NRs-based QDs were realized through etching techniques in multilayer MoS_2, with CB observed in devices of dimensions comparable to the ribbon width [Li and Mason, 2013, Kotekar-Patil et al., 2019]. [Ma et al., 2025] employed Ni/Au to contact grown, rather than etched, MoS_2 NRs and observed disordered CB with active areas corresponding to the physical device size [Ma et al., 2025]. Though promising, these systems remain susceptible to edge disorder introduced by the etching or growth process.

NTs and the similar "squashed tube" NRs shown in section 2.3.2 may circumvent some of these limitations. [Das et al., 2013] performed systematic work optimizing metal contacts for MoS_2, identifying scandium as a suitable material due to its low work function and favorable band alignment. Building on this, [Reinhardt et al., 2019] demonstrated successful low-temperature measurements on NTs contacted with scandium, achieving clean transport characteristics (figure 4.1).

However, despite some indications of transport through excited states, the measurements were limited by a large bias gap ($V_{SD,T}$). This strongly suggest a disordered multi-dot system, where tunneling through the system requires a finite bias voltage in order to span multiple chemical potentials of all QDs (see figure A.3).

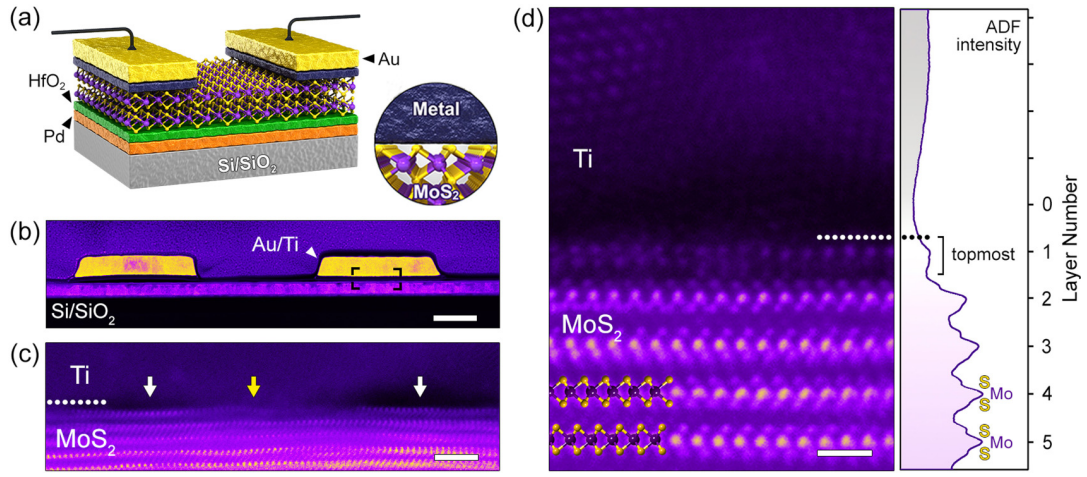


Figure 4.2.: High resolution annular dark-field (ADF)-STEM of the MoS_2 Ti interface. (a) schematic of a FET devices with Ti/Au contacts on a HfO_2/palladium back gate. (b) Large scale ADF-STEM of an interface cross section (scale bar 0.2 µm). (c) High-magnification of the rectangular region in (d) (scale bar 2 nm). Marked with a yellow arrow is a region of intimate contact as well as *gaps* between Ti and MoS_2 marked with white arrows. (d) Atomic-resolution image of the "contact" area together with the horizontal average of the ADF intensity on the right (scale bar 0.6 nm). From [Wu et al., 2019].

[Reinhardt et al., 2019] believe this to be caused by the reactive nature of scandium, which is expected to behave similar to Ti. In scanning transmission electron microscopy (STEM) measurements [Wu et al., 2019] found that Ti reacts with the underlying MoS_2 layer, destroying the crystalline structure and forming covalent bonds, see figure 4.2. The disorder introduced through this process should be able to host QDs directly underneath the contact metal, effectively shielding these from the 500 nm separated back gate.

Taken together, these results point to the need for geometries and contact strategies that preserve the integrity of MoS_2 and other TMDCs. NTs and edge-free NRs (figure 2.14) offer natural confinement and intrinsic boundaries, but only when combined with chemically inert, well-matched contact materials.

5. Transparent and Reproducible Contacts

As the previous chapter showed, the reliable fabrication of QDs in MoS_2 is hindered by fabrication induced defects, lithographic size limits, and, especially for NTs, insufficient contact quality. As NTs with diameters down to 20 nm and a very low defect density [Remškar, 2004] are used here, the first two obstacles are inherently solved and the focus lies on creating transparent and nondestructive contacts. To this end, different contact materials are tested to find a suitable candidate, which yields low resistive contacts with an ohmic character (transparent), while maintaining the structural integrity of MoS_2 (nondestructive).

The following chapter discusses possible strategies to mitigate or avoid the formation of SBs. In addition, it presents a room-temperature analysis of different contact materials and fabrication techniques, as well as a detailed investigation of the enhanced method introduced in section 3.1.5 to improve the reliability of contact fabrication. The work was carried out in collaboration with four M.Sc. students, namely Wolfgang Möckel, Jonathan Neuwald, Stefan Obloh, and Korbinian Fink. Parts of the data have been published in two M.Sc. theses [Neuwald, 2023, Obloh, 2025] and in two manuscripts [Schock et al., 2023, Schock et al., 2024].

5.1. Strategies for Reducing the Schottky Barrier

Section 2.2 showed that a SB between a SC and metal is very difficult to predict and the formation is almost unique to each individual material interface. However, based upon the theoretical models and insights gained over the years, several basic strategies have emerged in order to find a suitable counterpart for a given SC. Here three methods emerging from these insights are presented.

5.1.1. Type-I: Matching Metal Work Function

Probably the most basic strategy to avoid the formation of a SB is to match the work function of the metal with the electron affinity of the SC. The predicted barrier heights are found to follow the Schottky–Mott-rule from equation (2.1). This configuration will here be referred to as *type-I* contacts. For MoS_2 with an electron affinity of $\chi_{SC} = 4.0\,eV$, suitable choices are metals with a low work function, such as Ti or scandium.

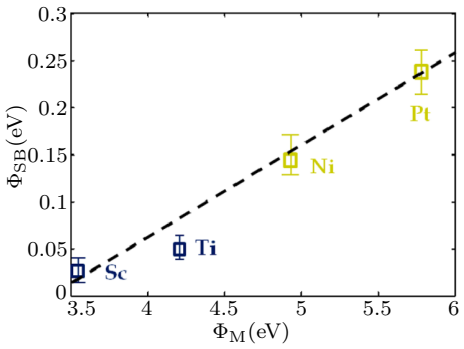


Figure 5.1: Extracted SB height over of the metal work function of different tested *type-I* contact materials. The black dashed line shows a linear fit to the barrier heights. Figure adapted from [Das et al., 2013].

[Das et al., 2013] investigated different metals and extracted the SB heights for each via Arrhenius-type measurements (see figure 5.1). They found a dependence following the linear Schottky-Mott-rule, with both Ti exhibiting the lowest barriers [Das et al., 2013]. Similarly, scandium was also effective for MoS_2 NTs [Reinhardt, 2019]. Unfortunately, the strong chemical reactivity reported by [Wu et al., 2019] (discussed in section 4.2) effectively excludes the use of these metals for contacts to MoS_2 QDs. Additionally, the transition metal Hafnium was also tested, as its work function of 3.9 eV places it in between scandium and Ti.

5.1.2. Type-II: Tunneling Barrier Contacts

Similar to the idea of the *fixed-separation-model* (section 2.2.2), a common technique in semiconductor technology is the insertion of a thin insulating barrier between the SC and the contact material. If this layer is thin enough (a few Å to nms), tunneling through the barrier is still possible while the separating insulator between the materials ensures a nearly unperturbed crystal structure at the interface. Thereby, the formation of MIGS should be prevented and the SB should be reduced. This has been tested with 2D TMDC materials with some success [Chen et al., 2013, Dankert et al., 2014, Farmanbar and Brocks, 2016, Pande et al., 2020]. This contact technique will be called *type-II* contacts.

Two material combinations are tested: a thin layer of insulating MgO topped with either a 20 nm thick layer of Au or copper. For oxidization protection the copper is additionally covered by a few nm Au capping layer. Both these materials were chosen as the conducting metal beyond the tunneling barrier due to their large DOS. These materials were deposited in a MBE system at pressures below $1 \cdot 10^{-9}$ mbar. In order to achieve contact thicknesses similar to the heights of the contacted NTs, an additional 80 nm of gold was deposited following the recipe in section 3.1.2.
Another option would be the use of mono- or few-layer hBN, which was reported to achieve ultra-low SB for planar WSe_2 [Pande et al., 2020]. However, since the curved geometry of the NTs is expected to substantially reduce the physical contact area, materials that grow directly on the NT surface were employed. This approach is intended to establish a larger direct interface between the device and the insulator–metal stack.

5.1.3. Type-III: Semi-Metal Contacts

The recent work by [Shen et al., 2021] first demonstrated that semimetallic bismuth forms true Ohmic (here referred to as *type-III*) contacts to monolayer MoS_2. They achieved a zero SB height through suppression of MIGS and the formation of a degenerate state between the SC and semimetal. Since this first report on semimetal contacts, this result has been confirmed for bismuth [Lee et al., 2024, Sun et al., 2024] and antimony contacts [Li et al., 2023a, Lee et al., 2024].
At the heart of this performance is the near-zero DOS of a semimetal at its Fermi level, which drastically reduces the interfacial MIGS that normally pin the Fermi level and create a Schottky barrier. When Bi's Fermi level lies at or slightly above MoS_2's CBM, only valence-band-derived gap states remain; these are filled completely ("gap-state saturation"), preventing any residual barrier and yielding a degenerate, barrier-free channel in contact with the semimetal. This mechanism contrasts with conventional metal contacts, where high DOS at the Fermi level drives strong MIGS and FLG.
Shen et al. performed first-principles density functional theory, further elucidating how Bi–MoS_2 contacts attain this behavior in a manner akin to the "fixed-separation" model. Simulations show an electrostatic dipole confined almost entirely within a van-der-Waals gap between Bi and MoS_2, with minimal charge transfer and a tunneling barrier only 1.7 Å thick ($\Phi_t = 3.6$ eV) leading to low tunneling resistivity and degenerate MoS_2 beneath the contact.

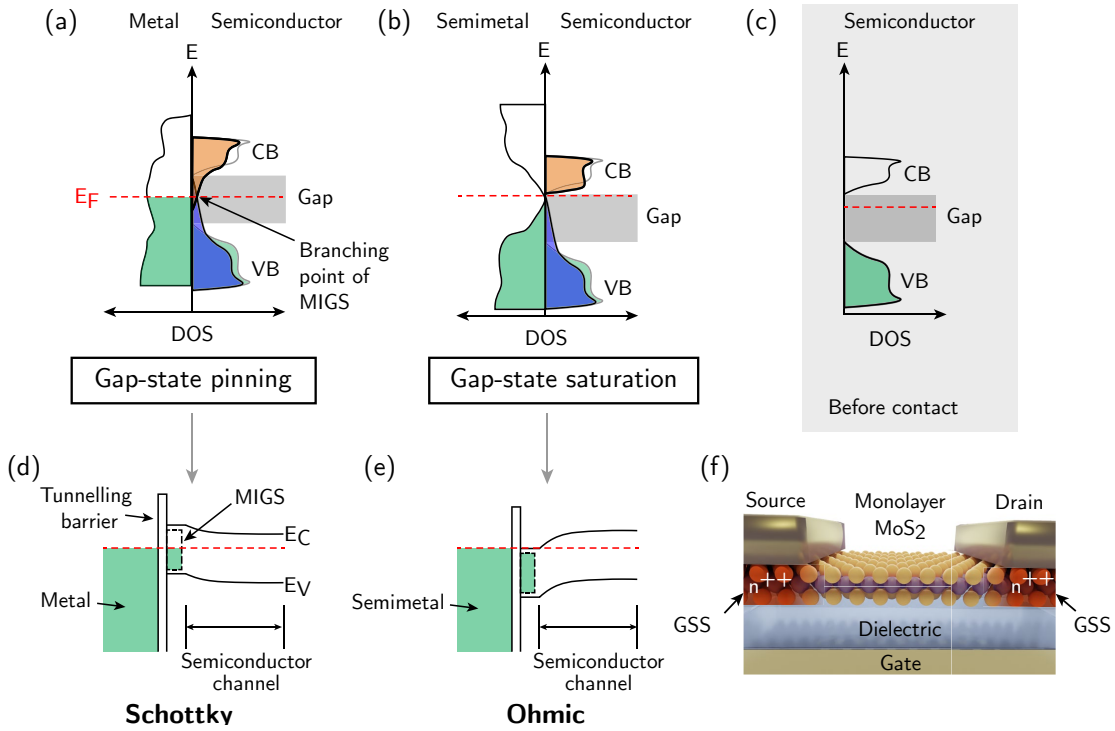


Figure 5.2.: Working principle of semimetal contacts to semiconducting TMDC. (a) DOS at the interface between a metal and a SC with the energy diagram of the resulting barrier in (d). (b) DOS at the interface between a semimetal and a SC with the energy diagram of the resulting barrier in (e). (c) DOS of an unperturbed SC. (f) Schematics of a MoS_2-bismuth devices, showing the gap-state saturation (GSS). From [Shen et al., 2021].

5.1.4. Other Contact Materials

Another common approach in semiconductor physics is the local doping of the SC at the interface [Gao et al., 2020, Jiang et al., 2023]. While this method has produced good results for planar MoS_2, the comparatively small surface area of NTs poses a significant challenge. Achieving sufficient doping coverage would require a higher dopant dose over a larger area to ensure adequate incorporation on the NT surface. Such conditions may introduce irregularities, potentially giving rise to trap states in the contact region, similar to those observed for Sc contacts (see section 4.2) as well as to inhomogeneous Schottky barriers. Nevertheless, copper has been identified as a promising candidate [Liu et al., 2018] and was therefore tested as bulk contact material.

5.2. Evaluating Contact Materials

Based on the strategies presented above, a set of contact materials was chosen and used to fabricate devices following the recipes of section 3.1. After the liftoff, the two-terminal resistance at ambient conditions is measured and yields comparative information on the contact quality (see section 3.2.1). In figure 5.3 the two-terminal resistance of each NT segment is presented as a point in the scatter plot, grouped for each contact material. While the majority of devices were produced via the "simple" *Scotch tape* method (section 3.1.1), the data is here not filtered for a specific transfer method.

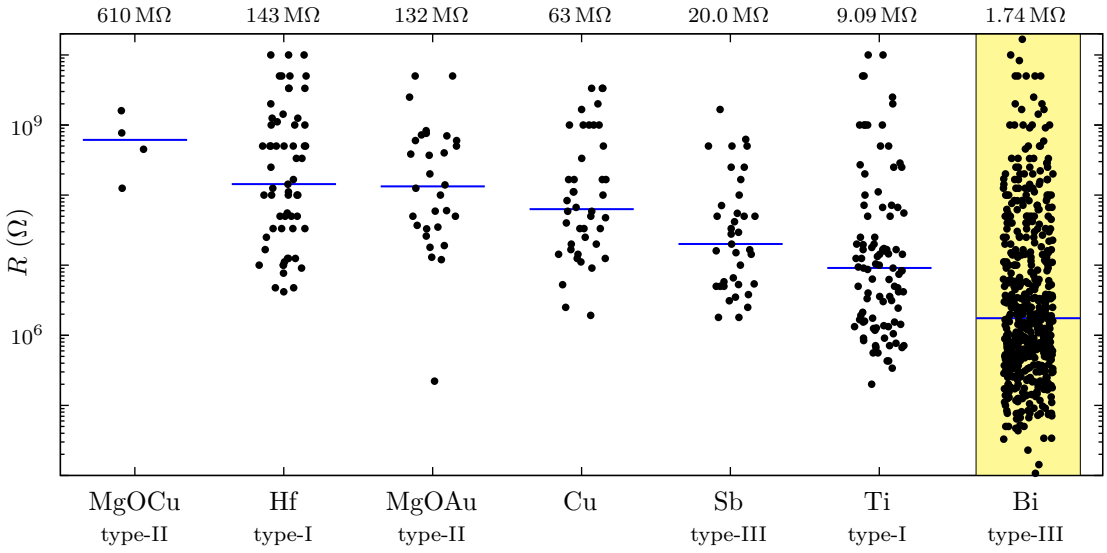


Figure 5.3.: Two-terminal resistances measured for individual MoS_2 NTs segments for different contact materials. Each data point represents one nanotube segment, with different transfer and fabrication methods aggregated. For better visibility, the data points are randomly spread in x-direction. Blue lines denote the median resistance for each contact material (value shown above), and bismuth (highlighted in yellow) exhibits the lowest median resistance. Data partly published in [Schock et al., 2023, Schock et al., 2024]

It is clear from the median resistance (written above the corresponding material) and the percentage of data points below 1 MΩ that bismuth outperforms all other materials. This is in accordance with the results for planar MoS_2 from [Shen et al., 2021] and indicates that the mechanism for the *type-III* contacts works and also applies to MoS_2 NTs.

The material performing second best is the *type-I* material titanium. A fairly good result was expected from previous works on MoS_2 flakes [Das et al., 2013] as well as NTs with scandium contacts [Reinhardt et al., 2019] discussed above. However, as the high reactive nature still poses a challenge for low temperature measurements, further investigations were neglected as the results of bismuth contacts indicate them to be better than Ti and at least similar in quality to Sc.

Opposed to the reported record resistances for planar MoS_2 [Li et al., 2023b], close to the theoretical minimum, antimony was only the third best contact material. Although also a *type-III* material, both the median and lowest resistance remain above the values of Bi and Ti, rendering it unsuitable for low temperature measurements. This was very surprising as its work function should match to the one of MoS_2 even better than Bi, while the fundamental mechanisms are expected to be the same. However, the record contact resistances achieved by [Li et al., 2023b] were obtained using antimony grown specifically in the $(01\bar{1}2)$ direction. This was accomplished by depositing at a temperature of 100 °C as opposed to deposition performed here at ambient temperatures without temperature control. Additionally, the NTs expose a curved surface area instead of a planar topmost layer of 2D MoS_2 which can be matched by the crystal structure of the semi-metal. The curvature may prevent the formation of single crystalline coverage.

While some devices with copper contacts exhibited resistances similar to the lowest values obtained for antimony, the median is much larger. The overall high values indicate that Cu is not a suitable material, at least in bulk configuration, for MoS_2 contacts. For the last *type-I* material Hf a comparably large resistivity was found. This is somewhat surprising, as the work function of Hf is closer to that of MoS_2 than that of Ti. The higher resistances might therefore indicate, that the improved conductance of Ti contacts is also caused by its reactive nature and the formation of a MoSTi-intermediate at the interface.

By far, the worst performing were the *type-II* material combinations MgO/Cu and MgO/Au with median resistances of 130 MΩ and 610 MΩ, respectively. Although the dataset on these materials is relatively small compared to the other materials, their inferiority is still clearly visible. Therefore no further investigations were conducted.

Overall, bismuth is the most promising candidate for transparent contacts at low temperature. Nonetheless, every material exhibited a very large scattering in their two-terminal resistances ($\approx 10^3$); in particular the Bi contacts scatters over almost 5 orders of magnitude. Later analysis will show that this large scattering is at

least partially caused by a shadowing effect of the NT surface (section 5.4) and that the majority of points with high resistances stem from suspended NTs devices. These were fabricated after the first publication [Schock et al., 2023], were a median resistance of 0.5 MΩ was reported, based exclusively on device fabrication following the *Scotch tape* method (section 3.1.1).

5.2.1. Room Temperature Transport Measurements

In order to confirm the quality of the bismuth contacts, further tests on individual devices were conducted. Figure 5.4(a) compares the source drain characteristic of a bismuth to a titanium contacted NT. Already from the difference in the current (see the scaling factor for titanium) a much higher resistance of the titanium contact can be seen. Additionally, a model for two back to back Schottky barriers is fitted to source drain characteristic of the Ti devices [Grillo and Di Bartolomeo, 2021], which describes the data well, yielding a barrier height of about 200 meV. In contrast, the bismuth trace is almost linear and it was not possible to fit the data using the double barrier model. Instead, a slightly larger forward current for negative bias voltages than the reverse current for positive bias is observed. This is consistent with a weak single barrier diode-like behavior [Tian et al., 2014]. As this is evidence for negligible SB at one and a very weak one on the other contact, the devices should meet the requirements for low temperature measurements.
Figure 5.4(b) shows the source drain characteristic as a function of the applied back gate voltage. In the low bias voltage (below 10 mV) regime the devices behaves almost linear for every gate voltage. This indicates that a Schottky barrier is sufficiently suppressed through the use of the Bi contacts. With decreasing V_G the current and therefore the conductance of the NT gets suppressed consistent with a n-type SC. This result is mirrored in the differentially measured conductance in figure 5.4(c), from which a I_{on}/I_{off} ratio of about 1000 can be estimated. This value is lower than that of [Shen et al., 2021], likely due to the thicker dielectric layer (500 nm SiO_2 vs. 100 nm SiN_x) and the resolution limit of the lock-in amplifier below $V_G = -25$ V.
The gate voltage dependence observed in figure 5.4(b) is qualitatively similar to that of several other devices, yet about half of the NTs showed no discernible gate response at all (see section A.4). Theory predicts that only small-radius armchair or multi-wall NTs may become semi-metallic [Seifert et al., 2000, Vadseth et al., 2024], while the majority should remain semiconducting (see section 2.3.2). Since CVT-grown NTs are almost exclusively chiral [Remškar, 2004] and typically have large radii, semi-

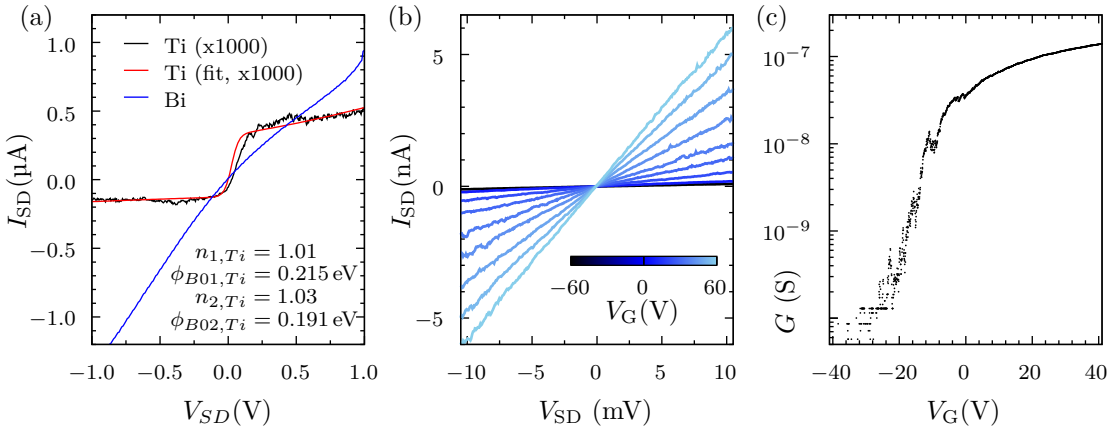


Figure 5.4.: Room temperature characterization of several NT devices contacted with bismuth and titanium. (a) The source drain current $I_{SD}(V_{SD})$ of the bismuth contacted device 4A and the titanium contacted device 5A. The Bi contacts exhibit almost ohmic behavior, while Ti contacts exhibit Schottky barriers. Using a fit model for a double Schottky barrier by [Grillo and Di Bartolomeo, 2021] a barrier height of approximately 200 meV is extracted. Source drain sweeps for varying gate voltage measured on the device 4B (b) confirm the n-type conduction, as well as a linear source drain characteristic for all gate voltages. In (d) the low bias differential conductance measured with a lock-in amplifier as a function of applied gate voltage confirms the semiconducting behavior and shows a I_{on}/I_{off} ratio of about 10^3 of device 6A.

metallic behavior is not expected. For NRs, no systematic predictions exist, though a semi-metallic state of the highly bent edges has been reported [Malok et al., 2025]. One might therefore anticipate that NRs lack a clear gate response, whereas NTs exhibit a cutoff. However, this interpretation does not match the measurements, as device 6A (figure 5.4(c)) is a NR.

A more consistent explanation is that different cutoff voltages of the multi-layer devices account for the observed variations. Table A.2 summarizes the estimated cutoff voltages for all investigated devices, derived from room-temperature and cryogenic measurements as well as the devices type. The cutoff values vary strongly, most likely due to different intrinsic doping from contamination, effects caused by the multi-wall nature and varying gate coupling determined by device geometry. Additionally, both NTs and NRs with and without band gap transitions were measured. Therefore, the cutoff of devices without clear indications of a band gap may simply lie outside the accessible measurement range.

5.2.2. Bismuth Contact Optimization

In figure 5.5(a), the two-terminal resistance is shown as a function of channel length. The data exhibit substantial scattering, which obscures any systematic dependence on the device length. Both high resistance values and devices with comparatively low resistivity are observed across the entire range of lengths. Consequently, the channel length does not appear to play a significant role in determining the overall resistance, suggesting instead that the resistance is predominantly governed by the contacts themselves.

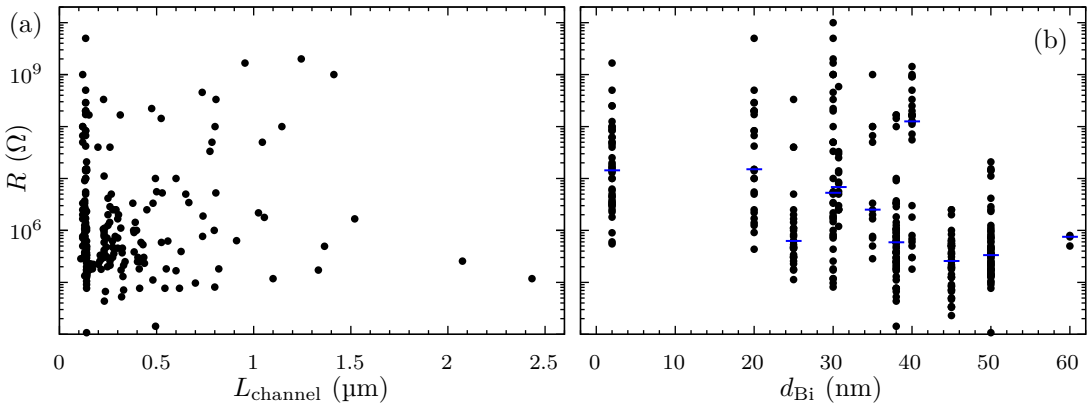


Figure 5.5.: Room temperature two terminal resistance of only bismuth contacted devices independent of the fabrication method as a function of (q) the channel length and (b) the bismuth thickness. In (b) the median resistance of each layer thickness is marked with blue bars at the appropriate resistance.

In an ideal case, the resistance of a device is at room temperature expected to increase linearly with channel length. This behavior arises from the fact that a wire exhibits a specific resistance per unit length, such that the total resistance scales proportionally with its length. This relation forms the basis of the transfer length method, in which the contact resistance can be estimated by extrapolating the linear trend to zero channel length. In the present data, however, only a slight increase in the lowest resistance values with channel length is discernible, and no clear linear dependence is observed at the lithographic scale. A quantitative determination of the contact resistance would therefore require devices with uniform contact properties, enabling a reliable separation of contact contributions from the intrinsic device resistance.

As illustrated in figure 5.5(b), the resistance of devices contacted with varying heights of bismuth appears to exhibit a preferential thickness of approximately 40 nm. As in figure 5.3, no distinction is made between different fabrication methods here. Thicknesses below 25 nm seem to be produce a lot more high resistance devices and only a few devices below 1 MΩ, much less compared to nearly every thickness between 25 nm to 50 nm. Despite the limited number of functional devices, thickness exceeding 50 nm also lead to increased contact resistances. An optimal layer thickness is possible, as two competing mechanism could prevail here.
First, a minimal amount of bismuth might be needed to form a continuous layer, an assumption which is collaborated by the observed growth predominantly generating grains (see figure 5.7(b-f)). Second, the high resistance of devices with thicker bismuth layers could be caused by the larger layer itself. As a semi-metal its resistance is much larger than that of Au, about 50 times at room temperature [Thompson, 1936]. However, this would only lead to a resistance of about 5 Ω for a 50 nm × 50 nm contact on a NT at 100 nm height and can therefore not explain the one to two orders of magnitude increase. Another possible mechanism could be a difference in heat capacitance of the resulting bismuth layer. Similar to heated growth of antimony, the thermal energy carried by the deposited Au particles could cause a recrystallization of the underlying bismuth layer into a more favorable configuration. Then increased thickness of bismuth could prevent this process as not enough thermal energy is provided by the Au in order to overcome the activation energy.
However, as the median resistances of each thickness are widely scattered and no further attempt was made here to compensate the nanogap formation explained in section 5.4 a clear trend cannot be expected here. Apart from settling on a reasonable thickness of around 40 nm to 50 nm no further evaluation or analysis can be performed without testing different thicknesses with the advanced fabrication technique discussed in section 3.1.5.

5.3. Investigation of High Resistance Scatter

Although the use of bismuth contacts allows the fabrication of nearly ohmic devices, the resistance values obtained across nominally similar samples still show considerable scatter. This issue becomes even more critical when device geometries increase in complexity, for example when FLG back-gates or hBN dielectrics are integrated, since

the number of available NTs per chip is thereby strongly reduced. To address this challenge, the following sections examine the impact of different transfer methods, the formation of nanogaps at the contacts, and additional factors that may degrade contact quality.

5.3.1. Impact of the Transfer Technique

In figure 5.6, the distributions of two-terminal resistances are shown for devices fabricated by the different methods described in section 3.1 and contacted with bismuth. The data clearly indicates that the classical *Scotch tape* method yields the largest fraction of devices with resistances below 1 MΩ, with a median resistance also below this value. In contrast, both the *suspended* and PC transfer methods exhibit higher median resistances and substantially fewer devices with resistances below 1 MΩ, even when the smaller overall sample size is taken into account. Furthermore, a comparatively larger fraction of these devices shows resistances exceeding 100 MΩ.

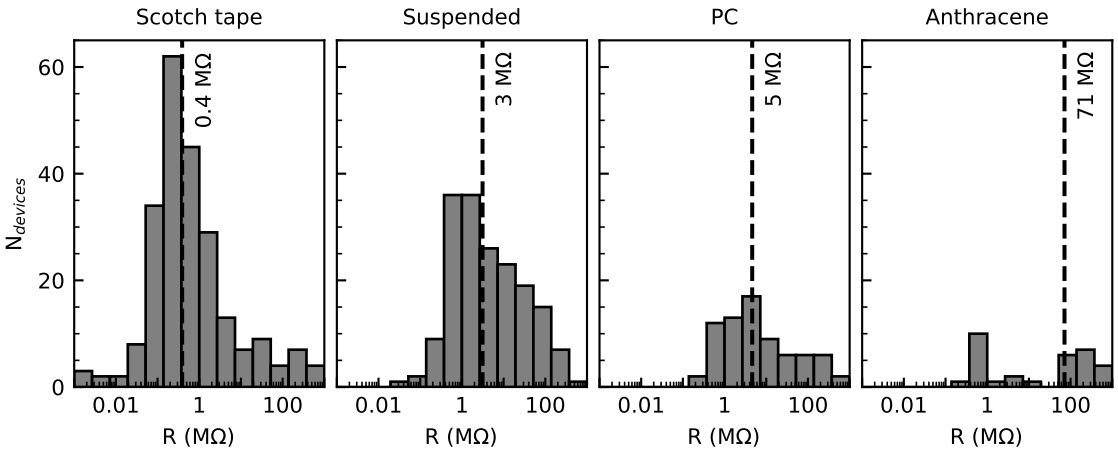


Figure 5.6.: Distributions of two-terminal resistance measured in bismuth-contacted NT devices, fabricated via the four distinct material transfer techniques: *Scotch tape* exfoliation (section 3.1.1), suspended NTs (section 3.1.3), PC-assisted (section 3.1.4), and anthracene-assisted transfer (section 3.1.4). The median of each distribution is marked with the black dashed line with the value next to the line.

The PC method introduces additional chemicals and transfer agents, like PC, PDMS, and chloroform, which have been shown to increase surface contamination [Otsuka et al., 2021, Schwartz et al., 2019, Jain et al., 2018]. Such contamination could in turn lead to a higher device resistance as these would sit right at the SC-metal interface. In contrast, this effect is not expected for *suspended* NTs, where

essentially the same chemicals and procedures as in the *Scotch tape* method are employed, with the only difference being that the NTs are transferred onto a resist layer instead of directly onto a SiO_2 substrate. A possible explanation could be a modified substrate interaction, which might shift the threshold voltage beyond the range of a grounded back gate. However, no significant conductance increase was observed at higher gate voltages. The elevated resistance is therefore more likely related to the same mechanisms that cause the large resistance scatter found for the *Scotch tape* transfer. This is further analyzed in the next section.

For devices fabricated with anthracene transfer, a split distribution of resistances was observed, with a median value of 71 MΩ. This spread arises from two different contact definition methods used during fabrication. Devices with resistances above 100 MΩ were transferred onto 50 nm gold contacts and subsequently covered with 25 nm bismuth and 30 nm gold, evaporated under a ±5° angle (figure 5.7(d)). In contrast, devices with resistances well below 1 MΩ predominantly stem from 2D heterostructure stacks contacted using the enhanced fabrication technique described in section 5.5 (e.g., 7A). In this approach, thicker layers of bismuth and gold were employed (50 nm and 100 nm, respectively). The broad resistance distribution is therefore most likely due to shortcomings in the earlier contact definition process, which are resolved by the enhanced technique. A degradation of the contacts caused by anthracene residues can thus be excluded.

Initially, it could not be ruled out that the increased median resistance observed for the more advanced fabrication methods was caused by a change in the MoS_2 source material [Schock et al., 2024]. For planar, CVD-grown MoS_2, several studies reported oxidization after long-term ambient storage [Pető et al., 2018, Spychalski et al., 2017]. As the NTs used at that stage had been stored under ambient conditions for an extended period, oxidization appeared possible. To exclude this scenario, newly synthesized MoS_2 NTs, kindly provided by Matjaž Malok and Prof. Maja Remškar, were employed for device fabrication. Since this did not lead to a significant improvement, a storage-related effect seems unlikely. However, because the newer material exhibited a different distribution of lengths and thicknesses, an intrinsic degradation of these NTs remained a potential concern. This explanation can be dismissed as well, as the last fabrication run (such as the low-resistance anthracene-assisted devices) demonstrated that the quality of the newer batches matched that of the earlier ones.

5.4. Formation of Nanogaps

The pronounced scatter of the resistance values in figure 5.6(a) suggests that, even for nominally identical device fabrication, fundamental limitations of the process remain. To investigate possible causes, several devices were examined in detail using scanning electron microscopy, with representative results shown in figure 5.7.

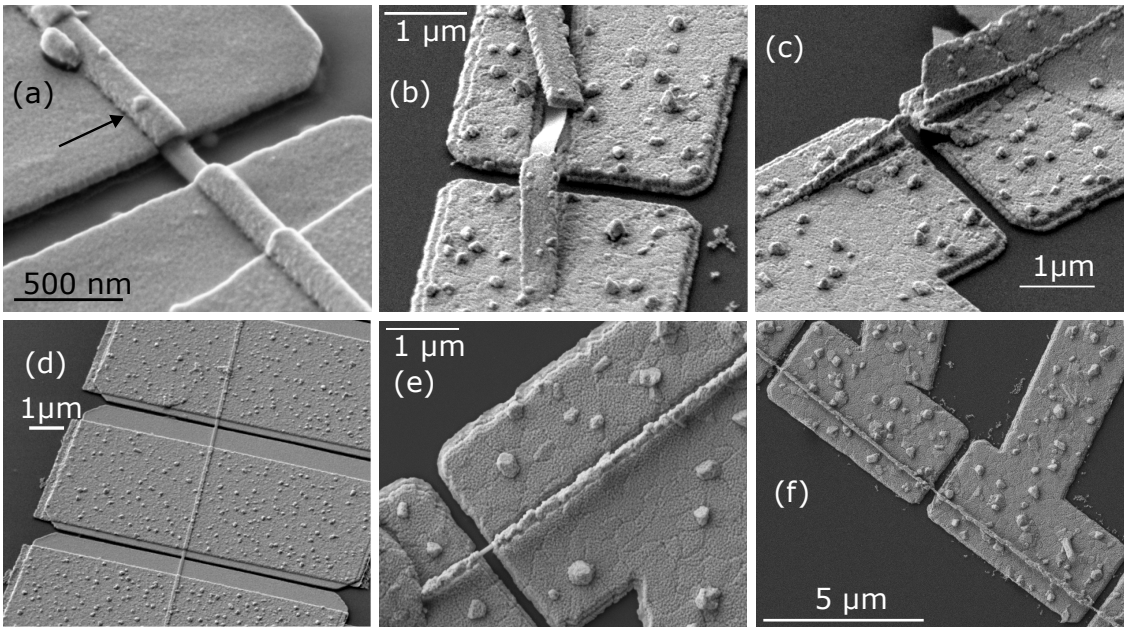


Figure 5.7.: SEM micrographs of NTs and NRs after contact deposition and room temperature testing. (a) NT with 40 nm Bi and 50 nm Au contacts (device 8A). The black arrow points to a possible gap. (b) NR with 50 nm Bi and 100 nm Au contacts (device 9A) (c) NT on the same device as (b). (d) NT transferred on predefined 100 nm Au contacts with anthracene (see figure 3.7) followed by a dual angle deposition of 25 nm Bi and 30 nm of Au (device 10A). Teared-out NT devices (e) 11A and (f) 12A. Further images can be found in figure A.9. (a-d) published in [Schock et al., 2024].

One factor that can limit the effectiveness of the contacts is the appearance of discontinuities between the metal deposited on the nanotube surface and the film covering the surrounding substrate. Such a gap is visible in figure 5.7(a), marked by the arrow. The effect originates from the geometric height of the nanotube in combination with the strongly directional character of thermal evaporation. As material accumulates on the upper side of the NT, a metallic cap develops that gradually shades the adjacent regions. With increasing thickness, this shadow extends further away from the nanotube, leaving parts of the sidewalls insufficiently

covered. A sketch of this shadowing process is given in figure 5.8. In contrast to CNTs, whose much smaller diameters prevent the formation of such gaps, this behavior is well known for larger nanostructures such as semiconductor nanowires. In ideal growth conditions, where the metal grows layer by layer and the atoms travel perpendicular to the surface, this gaps could extend for infinite thicknesses.

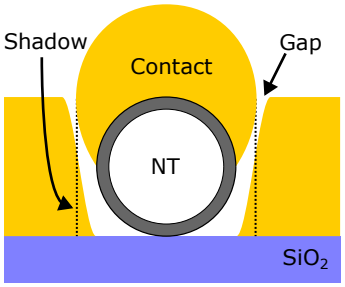


Figure 5.8: A schematic of the formation of a nanogap between the contact material deposited on the NT and the surrounding substrate, if the deposition is directed 90° to the nanodevice surface. As the material growing on top of the nanotube extends further, the shadowed region underneath the NT extends as well and based on the height difference contact will not be reached.

However, the images in figure 5.7 suggest a rather grain-based growth of the metal layers. In particular on top of the NTs the layers are formed out of individual grains instead of a uniform film. This leads to a fluctuations in the layer thicknesses, width of the metal cap, and therefore the potential size of the gap. Due to these variations, the gap can be bridged locally even if it should be present independent of the deposited metal thickness. As these bridges form spontaneously, the resulting quality of the contact would be expected to vary depending on the presence of any and the properties of them. However, the chance of a formation of such bridges should increase with larger layer thickness, as the grains can extend further with a larger supply of growth material.

The dependence of resistance on bismuth thickness, shown in figure 5.5(b), supports this interpretation. There, an optimum electronic performance was identified for contact layers of about 40 nm to 50 nm. This value is consistent with the idea that sufficiently thick films are required to bridge the shadowed region and connect the metal cap on top of the nanotube with the electrode on the substrate. If the deposited layer remains thinner, incomplete merging of the films can occur, producing interruptions such as those visible in figure 5.7(a). The high resistivity of the anthracene devices (figure 5.7(d) and figure 5.6) also indicates an insufficient layer thickness despite the angled evaporation used there.

Furthermore, the SEM images (b), (c), and (e) in figure 5.7 shows NTs that were *ripped out* of the contact material. All these devices were fabricated using the *suspended* method (section 3.1.3). These *tear-outs* most likely happened during the lift-off. As all the resist is dissolved, including the resist underneath the NT, there

should be no direct contact between the NTs and the substrate surface. Therefore the only connection that keeps them in place is the contact material. Assuming the presence of a nanogap, the NTs would be either immediately washed away or the bridges that formed might break at some sections. This is consistent with observations that some NTs were completely missing and for other (as in the figure) the *tear-out* only happened on some contact pads. Even though some of the devices depicted here were already fabricated with a angled deposition, the *tear-out* was still observed. Most likely the overall film thickness was too small to create a continuous layer for the highly suspended NTs. By further increasing the layer thickness, the contact effectiveness was increased for the final devices.

These observations highlight the importance of ensuring robust metallization in order to achieve reliable electrical coupling. In order to prevent the formation of these nanogaps, the contact deposition process was optimized to avoid the shadowing effect. Additionally, a crosslinked resist dome is utilized to "weld" the NTs to the chip surface and provide a smooth transition between NT and chip surface (see section 3.1.5).

5.5. Reliable Contacts via an Enhanced Process

In figure 5.9 the two terminal resistances from the enhanced fabrication method (see figure 3.8) are compared to those from the "classical" methods. The figure shows a strong decrease in the median resistance for all substrates and a reduced number of high resistive devices. Most notably, every pair of contacts to a single NT or NR exhibit similar resistances values, as opposed to a large variety of resistances on different contacts to the same nanotube before. This opens the possibility to perform four-terminal measurements on the same devices, determining the resistance of these NTs themselves (see table 5.1).

Particularly for hBN, the median resistance has decreased by about one order of magnitude. Almost all devices lie below the limit of 1 MΩ, which indicates a contact useful at cryogenic temperatures. This was previously a critical point, as devices with 2D heterostructures are much time consuming to prepare and all prior attempts of measurements at cryogenic temperatures of devices fabricated with the standard PC recipe failed.

The four-terminal measurements show that $R_{4\text{-term}}$ is consistently very close to $R_{2,3}$, the two-terminal resistance of the middle contacts. This indicates that the contacts

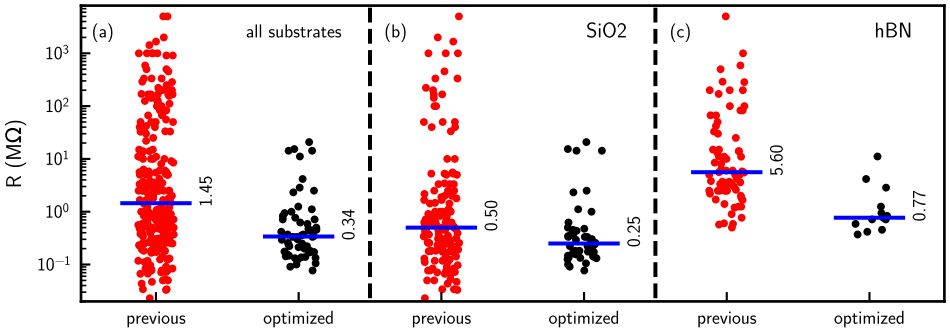


Figure 5.9.: Comparison of the two-terminal resistances of devices fabricated after the *Scotch tape*- and PC-methods and the enhanced method (section 3.1.5). Each panel shows the resistance with the previous fabrication techniques against the optimized method. (a) Two terminal resistances for all substrates, (b) only SiO_2 and (c) only hBN as a dielectric. For all substrates, especially the hBN devices, a drastic decrease of the median resistance and less high resistive NT segments is observed.

Table 5.1.: Four-terminal resistances of three NTs contacted with the enhanced fabrication method (section 3.1.5) on chip 13.

Device	13A	13B	13C
$R_{1,2}$	$(0.20 \pm 0.01)\,\mathrm{M\Omega}$	$(0.37 \pm 0.02)\,\mathrm{M\Omega}$	$(14 \pm 1)\,\mathrm{M\Omega}$
$R_{2,3}$	$(0.14 \pm 0.01)\,\mathrm{M\Omega}$	$(0.29 \pm 0.02)\,\mathrm{M\Omega}$	$(14 \pm 1)\,\mathrm{M\Omega}$
$R_{3,4}$	$(0.18 \pm 0.01)\,\mathrm{M\Omega}$	$(0.13 \pm 0.01)\,\mathrm{M\Omega}$	$(2.3 \pm 0.1)\,\mathrm{M\Omega}$
$R_{4\text{-term}}$	$(0.13 \pm 0.01)\,\mathrm{M\Omega}$	$(0.26 \pm 0.01)\,\mathrm{M\Omega}$	$(2.3 \pm 0.1)\,\mathrm{M\Omega}$

are of such a high quality, that the resistance is no longer dominated by the contact resistance. Instead, the main contribution seems to be the electric properties of the MoS_2 NTs.

The exception is devices 13C, where the four-terminal resistance is much lower then the two-terminal resistance of the middle contacts $R_{2,3}$. In fact, $R_{4\text{-term}}$ is similar to the lowest two-terminal resistance found on this NT ($R_{3,4}$). As the resistance between the other adjacent contacts are much larger, it seems that theses contacts are of a much poorer quality (contacts 1 and 2). However, the four-terminal measurements is independent of the contact quality and should therefore give the resistance of the NT itself. Compared to the other two NTs, this particular device seems to exhibit a much larger resistance.

To assess whether the investigated NT exhibit transport characteristics comparable to planar MoS_2 structures, a rough estimate of the sheet resistance was performed for device 13A. Assuming a simple diffusive model, the sheet resistance was approximated from the measured device resistance and an estimated geometry of diameter $d = (50 \pm 20)\,\mathrm{nm}$ and a channel length $L_{\mathrm{channel}} = (200 \pm 40)\,\mathrm{nm}$ taking the NT circumference as the effective width. In addition to the channel length, the mean free path within MoS_2 was considered, using a literature value of 75 nm [Pisoni et al., 2018]. Only a single conducting shell was assumed to contribute to transport; inner shells were neglected. Consequently, the resistance attributed to a single shell may be overestimated, and it would increase if intershell coupling were taken into account. For example inclusion of a second shell with an interlayer resistance of $2.4\,\mathrm{k\Omega\,\mu m}$ [Das and Appenzeller, 2013] would raise the effective resistance by roughly a factor of two. From these parameters, a sheet resistance of $R_{\mathrm{sh}} = (0.03 \pm 0.02)\,\mathrm{M\Omega}$ is obtained, which lies within the same order of magnitude as the value of approximately $15.6\,\mathrm{k\Omega}$ reported by [Shen et al., 2021]. Although the exact device geometry, layer thickness, and carrier density could not be determined, this estimate suggests that the investigated MoS_2 NTs exhibit transport properties consistent with those expected for CVD-grown planar MoS_2 devices.
With the successfully implementation of a method which ensures good contact quality of all contacts to a NTs, it was possible to perform cryogenic measurements on 2D heterostructure devices (see chapter 8 and section A.6).

6. QDs in Nanotubes on SiO_2

This chapter focuses on low temperature measurements of QDs confined in MoS_2 devices on the SiO_2 substrate surface. All MoS_2 nanomaterials were transferred following the *Scotch tape*-method (section 3.1.1) and contacted with bismuth and gold (see table A.1 for each sample). Most data in this chapter has been published in [Schock et al., 2023]. Device fabrication and measurement were performed together with M. Sc. Jonathan Neuwald.

6.1. Estimating Device Capacitance and QD Size

In chapter 4 it was shown that most QDs formed in TMDC devices correspond to impurities below the lithographically designed size. Therefore, a central aim of this thesis was the creation of QDs spanning the full active device area. However, in order to evaluate this for each measured QD, the size has to be estimated from the extracted charging energies and (gate) capacitances.

A very simple approach is to model the device as a plate capacitor. Then the device is assumed to be one side of two parallel planes, while the other side is the conducting Si backgate. From this the gate capacitance can be estimated and compared to the extracted value from the measurement. The nanodevice is then approximated as a metal plate of $A = w \times L_{\text{channel}}$ given by its width or diameter w and the distance between the contacts L. The classical capacitance of a plate capacitor can be used

$$C = \frac{\varepsilon_0 \epsilon_r A}{h} \tag{6.1}$$

with SiO_2 as a dielectric of thickness $h = 500\,\text{nm}$ and $\varepsilon_r = 3.9$ [Wunnicke, 2006, Robertson, 2004].

While this assumption fits the configuration of NR devices, the model is ill adapted to describe the curved structure of NT devices. Therefore a second model is used, which gives the capacitance per unit length C/L for a metal cylinder above an infinite metal plate. This is the "wire-over-ground" model [Ramo et al., 1994] where

$$\frac{C}{L} = \frac{2\pi\varepsilon_0\varepsilon_r}{\operatorname{arccosh}(t/R)}, \tag{6.2}$$

with t being the distance between the ground plane and the wire center and R the wire or NT radius. This model assumes that the dielectric layer thickness $h = t - R$ is much smaller then the length L of the wire $L \gg h$. As the channel lengths L_{Channel} of the devices used here are in to range of 80 nm to 500 nm and the silicon wafers have oxide thickness of 500 nm, this condition is rarely met. However, equation (6.2) can still be used as a rough estimation of the gate capacitance.

Additionally, the model also assumes the wire to be submerged in the dielectric, which is not the case for NT devices on top of the substrate or even suspended above it. However, this can be accounted for through the use of an effective dielectric constant. Using finite element simulations [Wunnicke, 2006] found $\varepsilon_{r,\text{eff}} = 2.2$ to be a suitable approximation to their simulated results, and it should similarly suit the configuration of the devices here.

An alternative approach for estimating the QD size is based on the extracted total capacitance C_Σ. In this method, the effective QD radius is obtained by calculating the size of a conducting disc in free space whose self-capacitance equals the measured total capacitance of the QD [Kouwenhoven et al., 2001, Hamer et al., 2018, Pisoni et al., 2018]. The corresponding radius r can then be determined by solving the equation for the self-capacitance of such a disc

$$C = 8\varepsilon_0\varepsilon_r r. \tag{6.3}$$

The value of ε_r used varies between different studies. Some use a value of the encapsulating hBN [Pisoni et al., 2018], or the material on which the QD is based [Hamer et al., 2018, Lau et al., 2022]. As the NTs here are on the SiO_2 surface, the same effective dielectric constant of 2.2 is assumed to match the configuration. The model of a flat disc in free space might be applicable in a 2D mono- or few-layer system, however, it does not match the shape of NT devices. Nevertheless, it can still be used for a very rough estimation of the QD size (especially for NR devices) in order to distinguish between features originating from a defect (which should not exceed radii of a few nanometers) and the entire device geometry.

A better estimation, at least for a tubular nanodevice and not a flattend ribbon, is the self capacitance of a cylinder or actual NT. A good approximation for this is

$$C = \frac{L}{8\pi\varepsilon_0\varepsilon_r} \times \frac{1}{\ln\left(\frac{2L}{r}\right) - 1} \tag{6.4}$$

the capacitance of a thin conducting cylinder, which is very close to the result found by numerical analysis for a conducting hollow tube, if the ratio between radius and length is small ($\frac{r}{L} \leq 0.1$) [Maxwell, 1877, Romashets et al., 2023].
A critical aspect is the capacitive coupling between the QD and the contacts. In encapsulated flakes, the QDs are typically confined by gates separated from the TMDCs by a few to several tens of nanometers of hBN. The actual contacts are well separated from the QD, rendering their contribution to the total capacitance negligible. Thus, approximating a conducting object far from any metallic material may be valid for gate-defined QDs. In contrast, the dots inside the NTs are confined by a barrier at the metal–semiconductor interface, where the close proximity to the contacts should add a non-negligible contribution to the total capacitance. A rough estimate can be obtained from a concentric-cylinder model, where the inner cylinder corresponds to the NT and the outer to the contact. Similar to the tunneling barrier between Bi contacts and planar MoS_2 reported by [Shen et al., 2021], a separation of $\Delta R = 1.66\,\text{Å}$ is assumed, resulting in a source (or drain) capacitance of

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{\ln\left(\frac{R+\Delta R}{R}\right)} \approxeq 1\,\text{fF} \tag{6.5}$$

for a NT of radius $R = 42\,\text{nm}$, and length $L = 75\,\text{nm}$ (half the mean free path length reported by [Pisoni et al., 2018]), and a vacuum permeability of $\varepsilon_r = 1$. This value is much larger then the experimentally determined source and drain capacitance of about 5 aF to 100 aF for gate defined QDs in planar MoS_2 [Pisoni et al., 2018, Tataka et al., 2024].

6.2. Inside the Band Gap

Figure 6.1 shows CB measurements performed in a dilution refrigerator (section 3.2.3) at a base temperature of $T \approxeq 20\,\text{mK}$. The absolute source-drain dc current $|I_{SD}(V_G, V_{SD})|$ is measured as a function of the back gate and source-drain voltage and plotted with a logarithmic scale. The measurements were performed on a NR with a width of $(500 \pm 10)\,\text{nm}$, a height of about $(18 \pm 1)\,\text{nm}$, and a channel length of $(270 \pm 10)\,\text{nm}$ (device 1A).

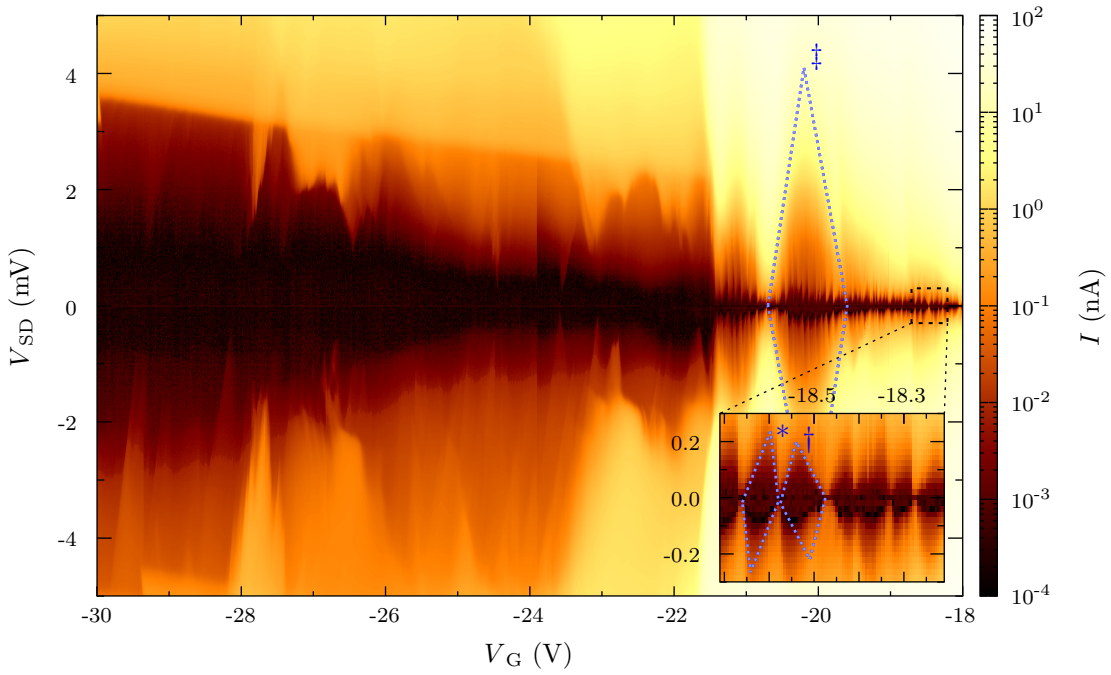


Figure 6.1.: Large scale CB measurements of the NR device 1A measured at $T \approxeq 20\,\mathrm{mK}$, the device current $|I_{SD}(V_G, V_{SD})|$ is color coded in a logarithmic scale. A transition into the band gap of the device can be observed at $V_G \approx -21.5\,\mathrm{V}$, with features corresponding to CB of different characteristic energy scales above. The inset shows a detailed zoom on the low-bias region at the highest back gate voltages.

In the measurements, a clear transition from a region with high transparency $V_G \geq -19\,\mathrm{V}$ to a region dominated by larger features of current suppression is observed. In the transparent part, CB with diamonds of two different sizes can be observed. In contrast to the previous measurements performed on the scandium contacted NTs (section 4.2) the tips of these mostly touch, which indicates that there a no charge traps in series to the central QD. This transparency is further evidence of the enhanced quality of bismuth as a contact material. The smaller CD ($*$ and † in the inset of figure 6.1 inset) correspond to a characteristic charging energy of about $E_C = (0.25 \pm 0.06)\,\mathrm{meV}$ and a gate conversion factor $\alpha = 0.0031 \pm 0.0004$ for the right and $E_C = (0.20 \pm 0.04)\,\mathrm{meV}$ and $\alpha = 0.0020 \pm 0.0004$ for the left diamond. Based upon the charging energy, the gate capacitance can be estimated to be $C_G = (2.0 \pm 0.2)\,\mathrm{aF}$ and $(1.6 \pm 0.3)\,\mathrm{aF}$ respectively. This is of the same order of magnitude as values obtained through plate capacitor (equation (6.1)) or wire-over-ground model (equation (6.2)), with $(9.3 \pm 0.5)\,\mathrm{aF}$ and $(18.4 \pm 1.3)\,\mathrm{aF}$ (assuming a

250 nm radius) respectively. That both capacitor models give larger values might indicate that the QD is not defined over the entire length of the NR. However, the estimated radii of a disk shaped system (equation (6.3)) with $r = (2.3 \pm 0.6)\,\mu m$, corresponding to a area of about $(16.6 \pm 1.2)\,\mu m^2$, are much larger then previously reported values (see chapter 4). As it was already mentioned, this can only hold as a very rough estimation of the QD size as the geometry of the system is much more complex. Additionally the small α indicates a comparatively large capacitive coupling of the leads to the QD, which are not taken into account. Nonetheless, this is much larger than what one would expect from a point like defect of a vacancy or defects inside the sample. Therefore it can be conclude that the QD is of a similar size as the active device area.

Below $-19\,V$ large CD are visible, which are much less regular and overlay the pattern of the small diamonds. These have an estimated charging energy of $E_C \approx (4 \pm 1)\,meV$ and a similar gate conversion factor $\alpha = 0.0037 \pm 0.0006$ based on the dotted lines labeled with ‡ in figure 6.1. From this, the size of the QD can be estimated to be $r_{2D} \approx (140 \pm 50)\,nm$, a much smaller value then for the other features so far. As the α is similar for all features the ratio between gate and contact capacitance remains unchanged, implying that the CDs originate from QDs of comparable geometry but with reduced size. The large difference in estimated radius indicates that it can only be a fraction of the active device area. Considering that the diamond is not tilted to one side and both source and drain slopes are almost equal, a position in the vicinity of the contacts can be excluded. This would cause a large capacitance of the closer contact dominating the sum capacitance and lead to a strong overestimation of the size. Therefore a point like defect seems to be unlikely to host this QD based upon the size. Most probable, another type of disorder causes a fractionation of the system into multiple QDs. This is consistent with the fact, that larger CB patterns reduce in size and are almost not observable at gate voltages $V_G \geq -19\,V$. At these voltages, the barriers dividing the system are overcome and a single QD is formed. Such barriers could be the result of a Moiré lattice, grain boundaries inside the NR, surface contaminations, or an uneven potential profile caused by the amorphous SiO_2 substrate.

At gate voltages below $-21.5\,V$ both the small and large diamonds are replaced by a large region of complete current blockage. This is consistent with reaching the band gap of the material, as it was previously shown in figure 2.22. No clear and regular pattern of CB is observed any longer, although some features at higher bias voltages

remain. After the sharp transition from the high conductance region at −21.5 V, the current for $|V_{SD}| > 1$ mV drops by about one order of magnitude. Together with the large bias offset, irregular patterns reminiscent of CB are still present with a size comparable to the larger diamonds observed at higher gate voltages. These could be caused by subset of smaller QDs of the system, which haven't entered the band gap at gate voltages. Then an electron would need to tunnel sequentially through multiple QDs, similar to the case of extra QDs under the contacts (see figure A.3). Therefore, a bias threshold could arise below which no current is measurable. This is also consistent with the increasing bias gap with decreasing gate voltage.
Another possible cause could be S-vacancies, as these would create in gap states inside of MoS_2 [Li and Zhu, 2015]. However, this is not very likely due to the already discussed feature size.

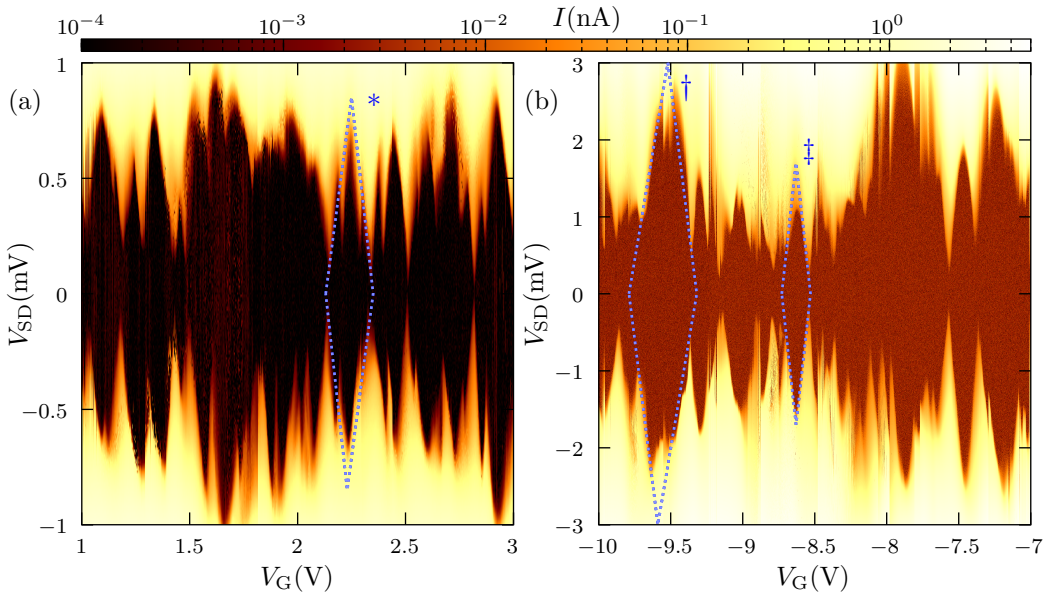


Figure 6.2.: Representative transport measurements performed at base temperature on (a) the NT device 2A and (b) the NR device 14A. The absolute current $|I_{SD}(V_{SD}, V_G)|$ is logarithmically color coded as a function of bias and gate voltage. Both devices show disordered CB with CDs of different characteristic charging energies. Blue dotted lines mark features of CB of different size and slope.

In order to further establish the reproducibility of the transparent contact more devices were measured. Figure 6.2 shows transport measurements of two other devices, a NT in (a) and a NR in (b). Both devices show clear patterns of CB with different characteristic charging energies, indicating a disorder-caused multi-

dot system. Nonetheless, the single electron tunneling regions of finite current almost reach the zero bias line ($V_{SD} = 0\,V$), again evidence that there is no major external voltage drop besides the main QD due to the transparency of the bismuth contacts. Compared to the NR in figure 6.1, the NT in figure 6.2(a) exhibits a much larger charging energy of about $E_C = (0.85 \pm 0.08)\,meV$ observed in the measured gate range. This is consistent with the smaller dimensions of the device ($L = (150 \pm 20)\,nm, w = (90 \pm 20)\,nm, h = (115 \pm 7)\,nm$). However, the device in (b) has again larger charging energy $E_C \approx (1.7 \pm 0.2)\,meV$ as opposed to its larger dimensions ($L = (200 \pm 20)\,nm, w = (155 \pm 30)\,nm, h = (20 \pm 10)\,nm$). Based on the larger α of this devices, a stronger confinement and a reduced capacitive coupling to the contacts might lead to a smaller QD despite the larger geometry.

Unlike figure 6.1, both devices did not show any indication of a band gap. For the NR device 14A the gate range for which transport measurements were performed was rather small and even below the gate offset voltage of the device 1A ($|V_G| \leq 10\,V < |V_{G,gap}| = 21.5\,V$). Therefore, the absence of a band gap is suspected to be a result of the limited gate range. Unfortunately, the device was destroyed by a gate leak, causing a large current through the NT, before higher (and lower) gate voltages could be measured.

For device 2A (figure 6.2(a)), the situation is very different. A much larger gate voltage range was tested ($-80\,V$ to $24\,V$) and no clear sign of a band gap was observed, rather closing CDs were found in the whole range. From table A.2, it can be seen that the gate values associated with a suspected band gap of the measured devices vary. This could be caused by some intrinsic doping either from contaminations on the NT's surface, defects already present after the growth, or interaction between the amorphous SiO_2 and the NT. Therefore, the gate value at which the band gap appears might also here be beyond the measurement range. Another possible explanation for the absence of a band gap would be a different band gap value of the NT compared to the NR. Theoretical calculations (section 2.3.2) indicate that, in the case of a single-wall NT, a very small diameter might suppress a band gap altogether [Seifert et al., 2000, Milivojević et al., 2020]. For multi-wall NTs, a similar effect was observed, with the inner shell being effectively "squeezed", reducing the band gap beyond the size of the gap of the outer wall [Vadseth et al., 2024]. Though the NT device 2A had a much larger diameter then the simulated ones, an alteration of the gap is still possible. The absence of a band gap can not be caused by in-gap states of S-vacancies, as the feature size only slightly varies over

the measured gate range with similar charging energies and gate lever arms values (see figure A.5).

To check for signs of single-level transport, the numerically derived conductance of each CB measurement was analyzed. Two typical results are displayed in figure 6.3. Panel (a) depicts another measurements of the device 14A, while (b) shows a different ribbon device 6B (see table A.2). While both have regions of almost touching CDs, no distinct lines are visible, which would indicate transport through a single level. Rather both stability diagrams are dominated by disorder causing the disordered CB and jumps in the gate voltage.

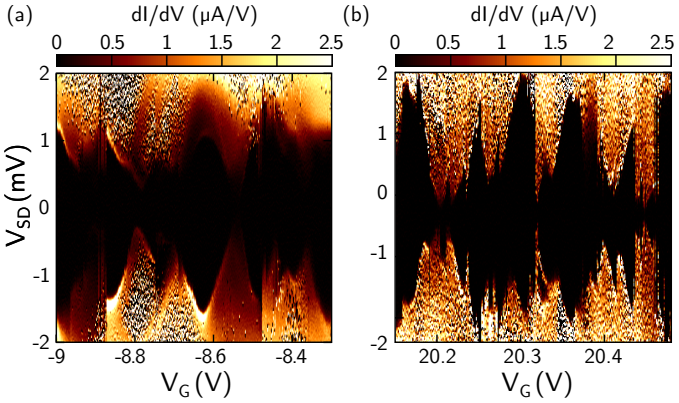


Figure 6.3: Stability diagrams of (a) device 14A and (b) device 6B. The current is numerically derived and plotted against bias V_{SD} and gate voltage V_G. CB is visible, but disordered for both devices. In the low bias region, the CDs almost touch.

From the disordered CB visible in figure 6.3(b), a charging energy in the range of 0.2 meV to 2.0 meV can be estimated, which is similar to the values observed so far. However, the disorder in the device was by far the largest, which makes a more accurate estimation of charging energy impossible. It is unlikely that the cause of this disorder is only the amorphous SiO_2; rather, a large contribution from the fabrication processes is suspected. As this was the only device measured at low temperatures with such a high degree of disorder, the observed effects are not attributed entirely to the intrinsic NR. Defects present after growth could also contribute to the disorder observed in all devices.

6.3. Single Level Transport

As the features visible in the inset of figure 6.1 were comparatively regular, temperature dependent measurements of the CB peaks at small bias voltages were performed. The results are shown in figure 6.4, where two exemplary gate traces at 20 mK and 100 mK, exhibiting five distinct peaks, are displayed. Based upon the peak shapes discussed in section 2.4.3, a

$$I_{\max} \cosh^{-2}((V_G - V_G^0)/\sigma)$$

fit was used extract the FWHM and maximum current of each peak together with a constant background.

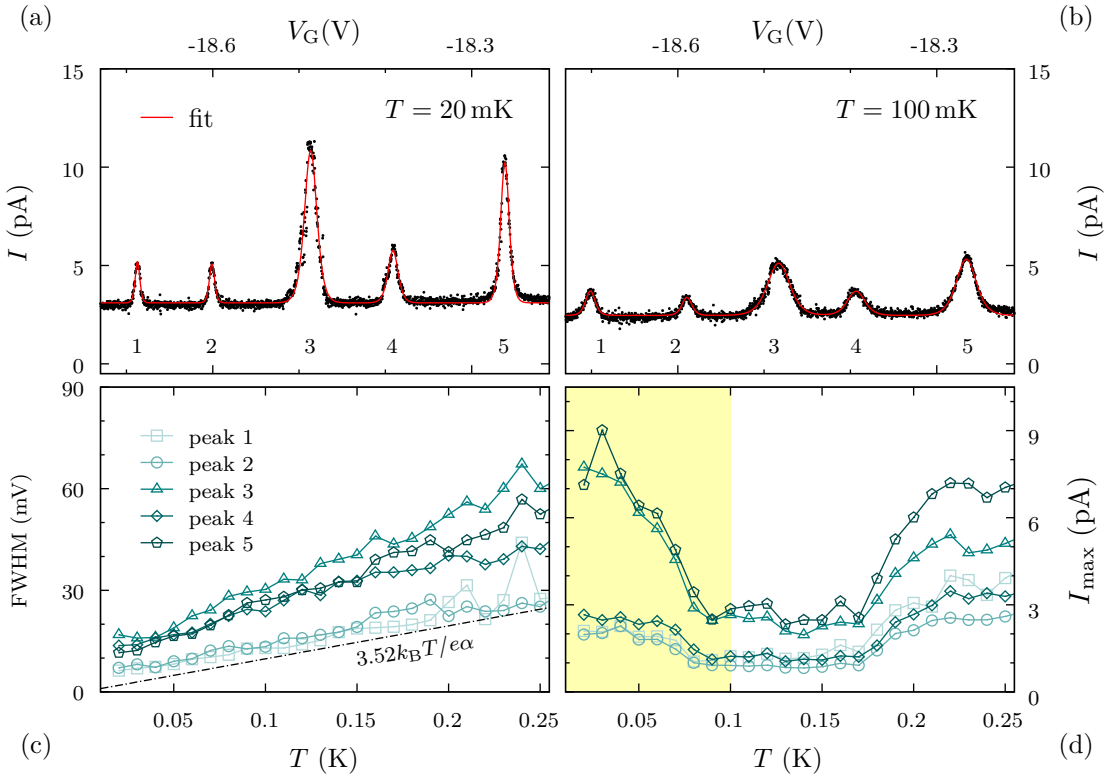


Figure 6.4.: Temperature dependence of the Coulomb peaks of device 1A measured in figure 6.1 at small bias voltage $V_{SD} \leq 0.01$ mV. (a) and (b) shows the Coulomb peaks at base temperature and 100 mK respectively together with a $I_{\max} \cosh^{-2}((V_G - V_G^0)/\sigma) + c$ fit as an example. In (c) the FWHM of the individual peaks is plotted as a function of temperature. The dotted black line marks the thermal broadening inside the leads. (d) Depicts the peak height as a function of temperature. The yellow area marks the region where $I_{\max}$ with decreasing T up to 100 mK.

The FWHM of all peaks, as can be see in figure 6.4(c), decreases with decreasing temperature and follows the line given by equation (2.28). The tunneling energy $\hbar\Gamma$ can be extracted and a value of (3.4 ± 0.6) meV for the two peaks 1 and 2, which follow the trend most clearly, was determined.

A clear indication that transport through a single level is reached can be seen from the temperature dependence of the peak height (figure 6.4 **d**). Inside the highlighted area, corresponding to temperatures below 100 mK, the peak height of all peaks decreases with increasing temperature. This is consistent with the maximum current dependence $I_{\max} \propto 1/T$ in equation (2.25) that describes the thermal broadened single level transport [Beenakker, 1991]. Above a temperature of ≈ 100 mK the peak height becomes independent of temperature and indicating that thermal energy (of about 8.6 µeV) gets closer to the level spacing δ_S and the condition for single level transport $k_B T \ll \delta_S$ is no longer fulfilled. Conversely, in the low temperature limit the peak height does not increase further, implying that the electronic temperature in the device saturates above the mixing-chamber temperature. Such a saturation could be caused by residual noise reaching the device via the measurement leads, which limits the achievable electron temperature.

Table 6.1.: Estimated charging energies, gate lever arm, gate capacitance, total capacitance and radius of a disk shaped QD (equation (6.3)) for the CDs marked in figure 6.1, figure 6.5, and figure 6.2, extracted from CB measurements.

device	CD	α	E_c(meV)	C_G(aF)	C_Σ(fF)	r_{disc}(µm)
1A	∗	$3.1(4)\cdot10^{-3}$	0.25(6)	2.0(2)	0.6(2)	2.3(6)
	†	$2.0(4)\cdot10^{-3}$	0.20(6)	1.6(2)	0.8(2)	2.9(8)
	‡	$3.7(7)\cdot10^{-3}$	4(1)	0.15(2)	0.04(1)	0.14(5)
	▷	$1.9(1)\cdot10^{-3}$	0.37(4)	0.80(2)	0.43(4)	1.6(2)
2A	∗	$3.9(2)\cdot10^{-3}$	0.85(8)	0.73(3)	0.19(2)	0.68(7)
14A	†	$6.4(3)\cdot10^{-3}$	3.0(2)	0.341(7)	0.053(4)	0.19(1)
	‡	$8.5(7)\cdot10^{-3}$	1.7(2)	0.80(4)	0.09(1)	0.34(4)

The size of the devices can be compared to the dimensions at which the level spacing is expected to become similar to the thermal energy (see table 2.2). As the NR had a width of approximately 500 nm and a design length of about 270 nm, the surface area is close to the estimated requirements for a QD at 100 mK. This also indicates that observed features correspond to a QD spanning the entire active area of the device.

The numerical derivative of the current in the inset of figure 6.1 with respect to the bias voltage V_{SD}, is shown in figure 6.5. There several features that appear to be

discrete lines are identified with white arrows. Based upon the large diamond with clear conductance lines at about −18.5 V, the CD spanning between peak 3 and 5 of figure 6.4 can be used to estimated the size of the QD separated energy level limit. The corresponding values are listed in table 6.1 and are comparable to the estimates obtained from the other small CD.

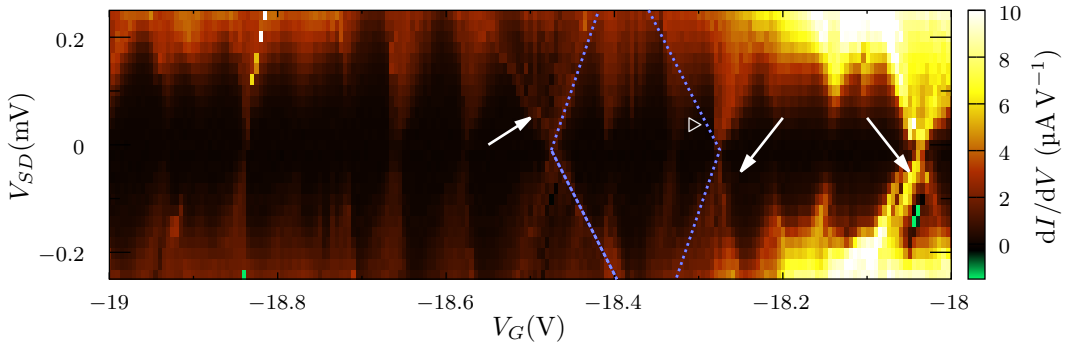


Figure 6.5.: Numerical derivative of the current in the low bias regime of figure 6.1. The conductance is color coded as a function of both bias V_{SD} and gate voltage V_G. White arrows mark discrete lines in the stability diagram and the blue dotted lines mark a potential CD.

Despite the disorder leading to multi-dot behavior, QDs with charging energies consistent with confinement sizes similar to those of the devices were successfully measured. Evidence of single-level transport was observed in the NR device 1A. Taken together with the largely reduced bias gap observed in all devices, these results indicate that bismuth forms non-destructive and transparent contacts to the MoS_2 NTs.

6.4. Conclusion: Reduction of Disorder

A very common challenge of the creation of QDs in any system is eliminating the causes of disorder. As all measurements of this chapter show, creating a clean system by chance is clearly impossible. For CNTs, a major improvement was the suspension of the NTs above the gate electrode between the contacts in order to eliminate the uneven potential of the SiO_2 substrate [Kuemmeth et al., 2008]. Another option is the use of a different dielectric with a crystalline structure and reduced thickness, like Al_2O_3 or hBN [Banszerus et al., 2018]. Together with a back gate of enhanced

crystallinity, such as FLG, the disorder could be reduced drastically by providing a uniform potential and screening of potential fluctuations from the SiO_2 substrate. As the largest contribution to the disorder is suspected to originate in the substrate interactions, further optimized fabrication techniques are used to reduce these by either suspending or the use of enhanced substrates. In the next chapters, low temperature measurements of devices suspended between contacts and on top of a hBN/FLG heterostructure are presented.

7. QDs in Suspended Nanotubes

Suspending nanostructures has been established as an effective method to reduce substrate-induced disorder and contamination. In the case of CNTs, growth on predefined gate and contact electrodes results in suspended NTs and additionally avoids residues from wet chemical processing [Cao et al., 2005]. This approach cannot be applied to the current MoS_2 growth process. However, suspension during contact definition is expected to reduce disorder arising from interactions with the amorphous dielectric SiO_2 layer. The devices investigated in this chapter were fabricated according to the procedure described in section 3.1.3. Fabrication of devices and measurements were performed in collaboration with M. Sc. Jonathan Neuwald and M. Sc. Stefan B. Obloh and have already been discussed in [Neuwald, 2023] and [Obloh, 2025], respectively.

7.1. Shallow Suspension

During the first tests, a thin layer of 2 % PMMA 50 k was spin coated at 8000 rpm on the Si/SiO_2 marker chips. This procedure yielded a thickness of approximately 50 nm (section 3.1.3). If suspending is successful, this distance should already suffice to reduce disorder from the amorphous SiO_2 substrate. Figure 7.1 shows a low temperature transport measurement of device 15A fabricated with this recipe and contacted with 40 nm of bismuth and 80 nm of gold. On a first glance, features corresponding to CB with different characteristic charging energies can be identified.

7.1.1. Transport Measurements

The transparency of the bismuth contacts is confirmed by the observation of a nearly vanishing gap at the regions where conductive diamonds touch (figure 7.1). Multiple diamonds with different charging energies are identified; a set of three is outlined in the figure, and the corresponding characteristics are listed in table 7.1.

As the gate voltage is increased, the large CB features observed at low voltage gradually vanish, reflecting a simplification of the multi-dot system. This likely results from a merging of smaller QDs into larger ones, reducing the number of active QDs and leaving predominantly small CD. The small oscillations (†) that persist over a wide gate range remain roughly constant in size, indicating that they originate from single, well-defined dots. Merging of very small QDs with these larger ones produces only minor increases in the QD size. This would only cause negligible changes to the observed features, consistent with the constant size of the small features. From the smallest structures (∗) visible in the inset in figure 7.1 a charging energy of (0.07 ± 0.04) meV, an α of about $(0.9 \pm 0.3) \cdot 10^{-3}$, and a gate capacitance of (2.0 ± 0.5) aF can be deduced. The charging energy is about an order of magnitude smaller than for the devices in the previous chapter, while the gate capacitance was similar. This is most likely caused by the extremely small α.

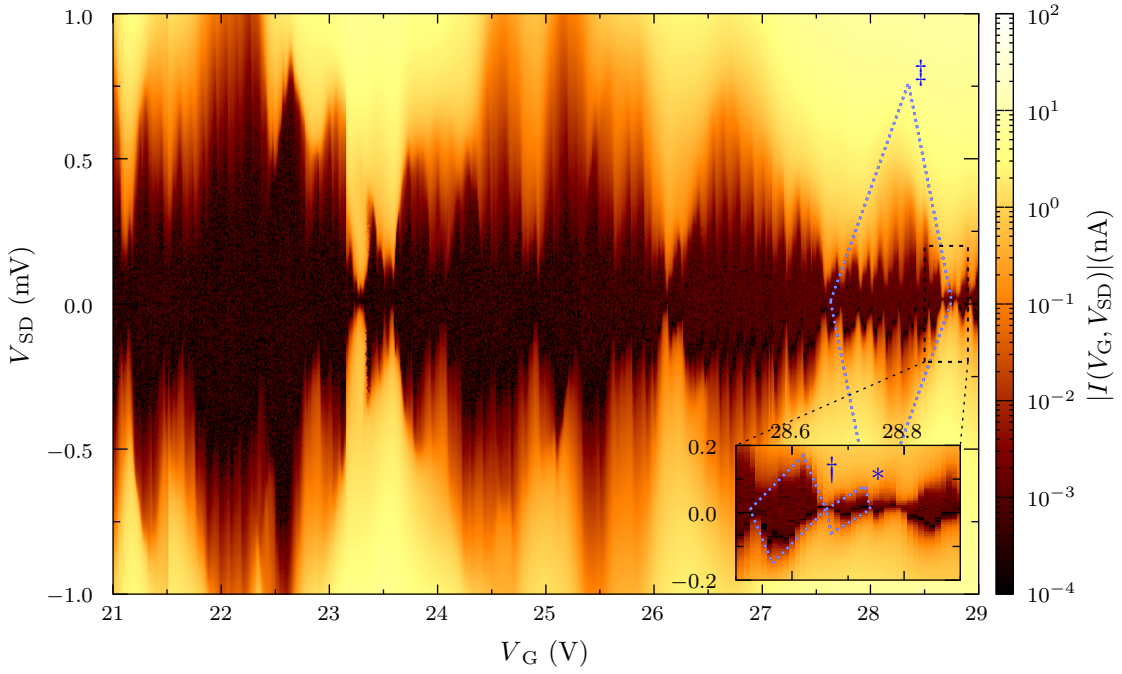


Figure 7.1.: Transport measurement of device 15A at base temperature ($T \approx 20$ mK). The absolute source-drain current $|I_{SD}(V_G, V_{SD})|$ is shown as a function of bias V_{SD} and gate voltage V_G with a logarithmic color scale. CB with features corresponding to different characteristic charging energies can be observed. At several points the tips of the SET region meet, confirming the absence of a voltage drop at charge traps inside the contacts. This is highlighted in the inset with a zoom at the region of almost completely vanishing bias gap.

As the goal here was a suspension of the NTs above the chip surface, thereby increasing the distance between the back gate and the NT further than before, a decrease of α was expected. This can be take as a first indication of a successful suspension. In order to evaluate this, the expected capacitance (section 6.1) for the measured devices was calculated, including the suspension height between the devices and the substrate of about 50 nm. The dimensions of measured NT segment can be estimated from figure 7.2, which was destroyed at the end of the measurement session, to be $d \approx (38 \pm 7)$ nm and $L \approx (140 \pm 10)$ nm. For the plate capacitor model, the distance to the substrate is included as an effective series capacitor with

$$C = \frac{\varepsilon_0 \varepsilon_1 \varepsilon_2 A}{\varepsilon_1 h_1 + \varepsilon_2 h_2}.$$

This results in a value of (0.09 ± 0.01) aF compared to the value of a non-suspended capacitor of (0.37 ± 0.09) aF. In the case of the wire-over-ground model, the calculation of an accurate capacitance is not trivial, as an effective ε_r was already used to approximate the effect of a wire on the surface of the SiO_2 instead of being submerged in it. However, a lower bound can be estimated with a NT in vacuum without any dielectric. This yields about (1.9 ± 0.5) aF, while the upper boundary of a NT directly on SiO_2 surface is (4.3 ± 1.1) aF. The actual value is expected to be between these two boundaries. The value found for the smallest CD is remarkably close to that of an in-vacuum NT. This could be an indication, that the smallest CDs originate from a QD of similar size as the active region of NT device.

Table 7.1.: Values of the gate lever arm α, the charging energy E_C, the gate C_G and sum capacitance C_Σ, and the estimated size of a metal disk in free space r_{disc} (from equation (6.3)) extracted from the CD marked in figure 7.1.

device	CD	α	E_C(meV)	C_G(aF)	C_Σ(fF)	r_{disc}(µm)
15A	‡	$7(1) \cdot 10^{-4}$	0.8(3)	0.14(3)	0.21(8)	0.8(3)
	†	$1.2(2) \cdot 10^{-3}$	0.16(5)	1.2(2)	1.0(3)	4(1)
	∗	$9(3) \cdot 10^{-4}$	0.07(4)	2.0(5)	2(1)	8(4)

The extremely small charging energy and the correspondingly large total capacitance are beyond the expected values of a NT of this size. In particular as this device is smaller than the ones measured in the previous chapter, a larger charging energy would have been expected. A possible explanation might be that the comparatively

large confinement region of the QD has now reached the contacts. As discussed in section 6.1, gate defined QDs in planar MoS_2, with tunnel barriers created between the contacted MoS_2 and the confinement region, have reported capacitance of about 5 aF to 100 aF [Pisoni et al., 2018, Tataka et al., 2024]. With the NT self capacitances (equation (6.4)) of about (20 ± 10) aF, a $C_\Sigma \ll 1$ fF would be expected, even with contacts closer than in gate defined QDs. As this is not the case, one contribution to the sum capacitance must be dominating. While it is also plausible that the inner walls of the nanotube could act as a capacitor, their impact should have been seen in the prior measurements without suspension. Therefore, this is ruled out as possible source of increased capacitance, leaving the contacts as the main suspect. If the QD expands into the NT regions below the contacts, a capacitive coupling between the QD and contacts should reach the values estimated previously for a tubular capacitor of about 1 fF (section 6.1). This value is much closer to C_Σ determined through the CB measurements and therefore a QD expanding underneath the contacts seems likely.

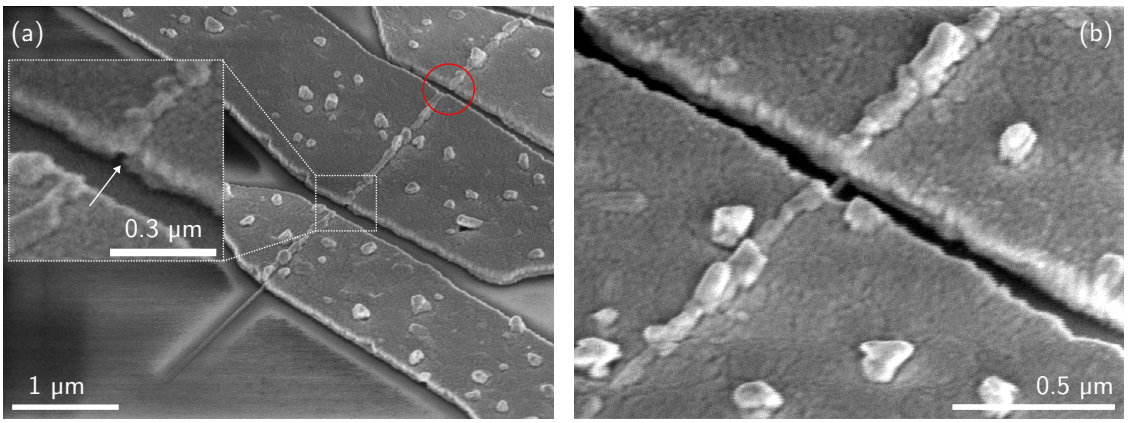


Figure 7.2.: SEM images of the device 15A. (a) Overview of contacts. The red circle marks the measured NT segment, which was destroyed during the measurement. The white rectangle marks the position of the enlarged inset, which shows a channel were the segment is also gone. Underneath the hole, where the NT extended into the contact, some material seems to protrude even below the no longer existing NT. (b) Zoom on the same NT at contacts outside of the displayed area in (a).

Further investigation of the SEM micrographs in figure 7.2 reveals material could be underneath the NT (white arrow in inset of (a)). This might indicate that the NT was suspended inside the contacts, as contact material had grown underneath it. Such a geometry fits the tubular capacitor model used to estimate $C_{S,D}$.

Inspecting the fully measured gate range (see figure A.6), a behaviour different from figure 6.1 is observed. Over the whole gate range of −65 V to 40 V instead of a clear band gap transition, only an increase in a bias gap is observed for voltages $V_G < 20\,V$. With the small α value found here, it seems very likely that the band gap of the device was not reached within the gate voltage range. Additionally, the feature size increases drastically from the charging energies in the range of 0.08 meV to 0.1 meV to several meV. This would be consistent with the QD spanning the devices "breaking" into a series of small QDs with much larger charging energies, an indication that the expected reduction in disorder through suspension of the NTs was not achieved.

7.1.2. Temperature Dependence of Transport

Temperature dependent measurements on the region of (almost) closing CD in figure 7.1 were performed in order to confirm if transport through a single level was reached. Two exemplary gate traces at small bias voltages are shown in figure 7.3(a) and (b). Eight Coulomb peaks with very different widths and heights were measured. Although this could be caused by different tunneling rates for different states in the QD, a more likely cause is the disorder already observed in the previous measurement. It is therefore not clear if the peak shape really follows the ideal equations formulated in section 2.4.2. Nevertheless, a $1/\cosh^2$ fitting is used to extract the width (equation (2.28)) in (c) and height (d) of the peaks.
Similar to results found for NR device 1A in direct contact with SiO_2, the peaks broaden with increasing temperature. This follows the thermal broadening of the leads according to equation (2.28), indicating a good thermal coupling of the QD system. The strong deviations occurring for peak number 6 and 8 above temperatures of about 150 mK are most likely an artifact of the fit, as the peaks start to overlap. Especially, peak 8 merged with a region of minuscule diamonds in figure 7.1 above 175 mK. In the appendix the FWHM of the odd numbered peaks is plotted (figure A.10), which behave very similar to the even numbered peaks with the exception of very erratic jumps of peak 1 below 70 mK. The fit at $T = 33\,mK$ in figure 7.3(a) is not very accurate for this peak, which could be a sign that this is a double peak, that is not clearly resolved at the measurement resolution.
Unlike in figure 6.4, the current maxima do not increase with decreasing temperature. Peaks 2 and 4 (and peaks 3, 5, and 7 in figure A.10) remain almost temperature independent, indicating a classical QD with level spacing smaller than the thermal

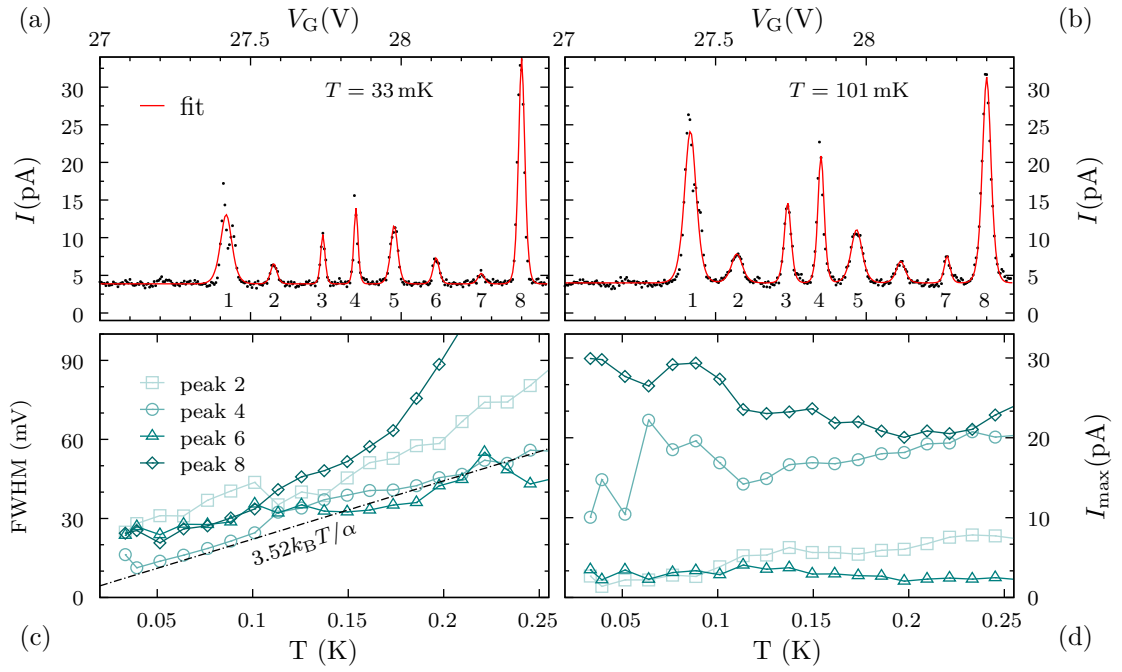


Figure 7.3.: Temperature dependence of the Coulomb peaks in figure 7.1 measured at a low bias voltage ($|V_{SD}| \leq 0.06$ mV) of device 15A. In (a) and (b) the data is plotted along a combined fit of eight $1/cosh^2$ peaks with a constant background for two different temperatures. (c) Shows the evolution of the FWHM of the even numbered peaks as a function of the temperature. The black dashed line shows the thermal broadening of the leads according to equation (2.28). (d) Displays the maximum current I_{max} of the even peaks as a function of temperature. The data of the odd peaks can be found in Appendix figure A.10.

energy at base temperature. Peak 1 also appears temperature independent down to 100 mK, followed by an irregular reduction in maximum current below. As the fit fails to reproduce the peak shape at low temperatures, it is unsurprising that the current maximum does not follow a consistent trend.

A different trend is observed for peaks 6 and 8, where the maximal current slightly increases with decreasing temperature. Peak 8 increases monotonically toward lower temperatures, though with a smaller slope than observed for device 1A with confirmed single-level transport. It remains possible that this peak corresponds to a single-level transition within the multidot system. Peak 6, by contrast, displays mixed behavior: between 0.06 K to 0.11 K an inverse trend is followed by a discontinuous transition to reduced maximal current. From the FWHM it is evident that peak 4 is the smallest, suggesting the measurement resolution may have been insufficient for reliable fitting.

Overall, it cannot be confirmed that the QDs measured in device 15A are in the single level transport regime. Even though there are some indications that parts of the disordered multi-QD system are small enough to exhibit a large enough level spacing, a QD with $\delta_S < k_B T$ spanning the active device area can be ruled out.

7.1.3. Signs of a Charge Trap

Figure 7.4 shows CB patterns at higher gate voltages than displayed in figure 7.1. In contrast to the CD observed so far, distinct extra "teeth" (extra peaks) are visible and marked with white arrows. The resulting double saw pattern is reminiscent of the measurements performed by [Hofheinz et al., 2006] (see section 2.4.5). There a charge trap close to the measured nanowire was switching between two charge states, effectively shifting the measured diamond with each switching event. In the figure two possible shifted diamonds are outlined (light and dark blue dashed lines) and the shift voltages are marked. The overall gap between the positive and negative bias diamonds closes with increasing gate voltage (white dashed lines). This behaviour indicates that both energy states of the trap get closer with increasing gate voltage and are almost identical at $V_G = 36\,\mathrm{V}$.

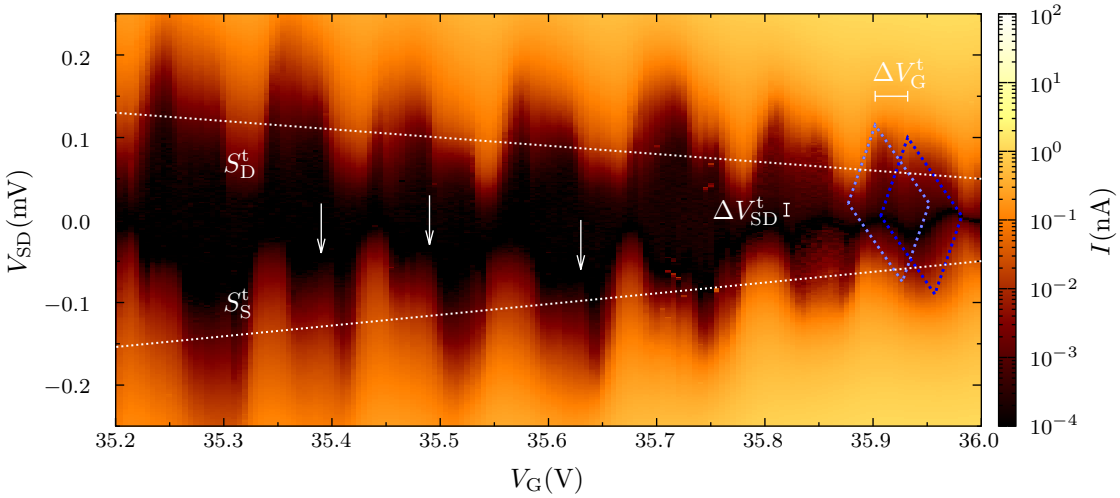


Figure 7.4.: Transport measurement of device 15A at base temperature. CB is visible with a distinct extra peak inside the CDs (white arrows). Two possible diamonds are outlined in light- and darkblue together with the gate V_G^t and bias V_{SD}^t shift. The decreasing bias gaps of the double saw patterns are marked with white the dotted lines S_S^t and S_D^t.

From the distance between two Coulomb peaks, e.g the width of a single diamond, of about $\Delta V_G = (75 \pm 5)\,\mathrm{mV}$ and the shift caused by the trap $\Delta V_G^t = (30 \pm 5)\,\mathrm{mV}$ the lever between trap and QD can be estimated $\beta^t = \Delta V_G^t / \Delta V_G \approx 0.40 \pm 0.09$. As a second approach, the slopes of the bias gap caused by the trap can be used. With equation (2.19) β_t is determined to be about 0.50 ± 0.07, which is in good agreement with the value from the CD shift. Additionally, these slopes can be used to extract the gate lever arm of the trap $\alpha_t = (7.5 \pm 1.0) \cdot 10^{-5}$.

From β_t the position of the charge relative to the QD and the contacts can be estimated. A value of $\beta^t \approx 0$ would indicate a trap close to the source or drain, where as a value of about 1 would indicate a close proximity to the main QD. Additionally, a trap close to the source would give rise to "teeth" on the positive side of the diamond while "teeth" on the negative side corresponds to a trap at the drain side [Hofheinz et al., 2006]. Therefore, a trap half way between the dot and drain contact is determined.

7.1.4. Cause of Residual Disorder in Shallow Suspended NTs

Temperature-dependent measurements indicate that the device was either too large or contained too many electrons to reach the single-level transport regime. Furthermore, disorder as well as signatures from a charge trap observed in the measurements suggests that the suspension did not totally achieve the intended reduction in potential fluctuations. A possible reason for this could be the relatively small suspension height compared to the channel length. This might have been insufficient to fully lift the NT along its entire length or effectively smoothen the random potential of the underlying amorphous SiO_2. Although evidence was found for possible contact material located beneath the NT, it remains unclear whether it was completely embedded within the contact region. If not, residual contact with the substrate surface could persist, with the resulting van-der-Waals forces likely pulling the NT closer to the surface and thereby introducing additional disorder. Nevertheless, a full contact between the NT and the SiO_2 appears unlikely, as the strongly reduced α and the corresponding gate capacitance still indicate at least a partial suspension. To further eliminate the possibility of substrate contact, subsequent measurements were carried out on devices with significantly larger suspension heights.

7.2. High-Aspect Ratio Suspension

Building on the observations from the shallow-suspension devices, the subsequent fabrication rounds were aimed to minimize substrate interaction and thereby further reduce disorder. To this end, the first resist layer was increased to approximately 200 nm by using PMMA 200k dissolved in 9 % anisole. This greater separation between the NTs and the disordered SiO_2 was intended to ensure that the NTs remained entirely suspended over the substrate along their full length.
This approach initially resulted in devices with either high ($> 10\,M\Omega$) room-temperature resistances or no detectable contact at all. SEM inspection (see figure 5.7) revealed that the poor yield originated from a noticeable higher incidence of *torn-out* NTs. On some chips, almost all NTs appeared to have been ripped out of their contact pads during the lift-off process. Although a frustrating outcome, this nevertheless provided evidence for a fully suspended geometry, in contrast to the suspected partial suspension for the previous devices.
In this configuration, the large bottom resist thickness prevents the NTs from bending towards the substrate in the contact regions. Under typical conditions, strong van-der-Waals forces between the NTs and the SiO_2 keep the NTs anchored in place, even during spin-coating and washing steps. As discussed in section 5.4, the presence of a thin film discontinuity between the metal in direct contact with the nanodevice and the surrounding film is suspected. With the increased suspension height, such discontinuities are expected to be more common, particularly when the total contact metal thickness is smaller than that of the bottom resist. In the absence of both the van-der-Waals interaction and a continuous metal film engulfing the NT, the NTs are held only by the resist and are therefore vulnerable to being washed away during lift-off.
These challenges where overcome by a combination of increased layer thickness and angled evaporation of the contact material. The appropriate steps are mentioned in section 3.1.3 and build the basis for the enhanced fabrication scheme in section 3.1.5 together with the crosslinked resist “welding” spots.

7.2.1. Low-Temperature Transport Measurements

Low temperature transport measurement confirm the formation of QDs in multiple devices. Figure 7.5 shows typical result of these measurements. Similar to the observations of all other Bi-contacted devices, closing CD with touching SET tips in

(b) confirm that no traps remain isolated underneath the contacts. However, a high level of disorder was still observed for all these devices, manifesting as a disordered CB pattern originating from multiple QDs of very different charging energies in (a).

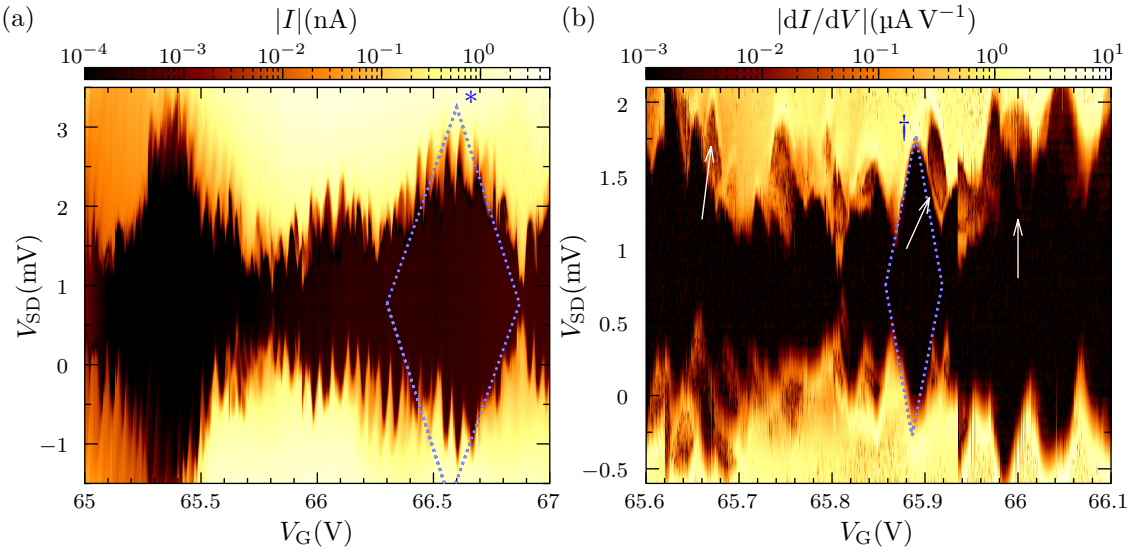


Figure 7.5.: Low temperature measurements on device 16A. (a) Logarithmic plot of the absolute current as a function of bias and gate voltage. Disorder CB can be observed, the largest features are outlined with a blue dotted line and marked with the label ∗. (b) Stability diagram of the region in (a) where the CD almost touch. A possible small CD is outlined and labeled with the label †. Additinally, white arrows highlight conductance lines.

From the outlined features in figure 7.5, the corresponding charging energies and gate capacitances (see table 7.2) are estimated. Remarkably, the values are very different from the ones found for the shallow-suspension devices (see table 7.1). Here the results indicate a much smaller confinement and for the smallest features a remarkably increased ratio of gate to contact capacitance as α is larger. However, the overall measurements were dominated by disorder, both in the form of disordered CB as well as strong switching behavior. The left side of the stability diagram in (b) is dominated by instability and jumps in the conductance. Therefore it is most likely that the measured device still consists of a system of multiple QDs. Based on the sum capacitance and the estimated radii, larger confinements are suspected and point like defects, such as vacancies, can be excluded.

Nonetheless, white arrows in the stability diagram (figure 7.5(b)) show some distinct conductance lines. These might indicate that at least some of the QDs are in the

Table 7.2.: Estimated values for the CD marked in figure 7.5.

Device	CD	α	E_C(meV)	C_G(aF)	C_Σ(fF)	r_{disc}(µm)
16A	*	$4(1) \cdot 10^{-3}$	2(1)	0.28(5)	0.06(3)	0.2(1)
	†	0.016(2)	1.0(2)	2.6(3)	0.17(3)	0.6(1)

single level transport regime. Owing to disorder, it is not possible to single out a CD corresponding to these QDs and therefore neither the charging energy nor the dimension can be estimated.
Similar to the results found for the device 15A, a clear band gap transition is absent from the measurements over the whole gate range (see figure A.7). Rather a slow increase of a V_{SD} gap up to values of 20 mV is again observed. If this would be caused only by a disordered system alone, a similar charging energy of 20 meV would be needed (based on equation (2.20)). This seems unlikely as such large charging energies would exceed that of confinement on an atomic scale. Therefore a QD, which is only weekly coupled to the gate and gradually enters the band gap seems more plausible.

7.2.2. Current Annealing

Another device on chip 16 (device 16B) displayed a very large bias gap (see figure 7.6(a)), a behavior persistent over a large gate range. This is very similar to the bias gap observed for the scandium contacted devices shown in figure 4.1. It is very well possible that here again a series of QDs have formed in the contacted region, rendering measurements in the linear CB regime impossible. As bismuth contacts have so far been proven to be of a higher transparency than Ti or scandium, a similar mechanism creating these additional QDs seems unlikely. Instead of disorder introduced by the reactive nature of the contact metal, this could be an artifact of the cap formation process that leads to the nanogaps (see discussion in section 5.4). From the SEM images in figure 5.7 it can be seen, that the Bi/Au layers predominantly grow in grains rather than a continuous layer. If a single grain is only weakly contacted to the other grains, yielding a poor resistance that "freezes out" at cryogenic temperatures, it would only be in contact with the NT acting as either a potential barrier or an additional charge trap. Therefore, this could lead to a similar effect as was observed for the scandium contacts [Reinhardt et al., 2019].

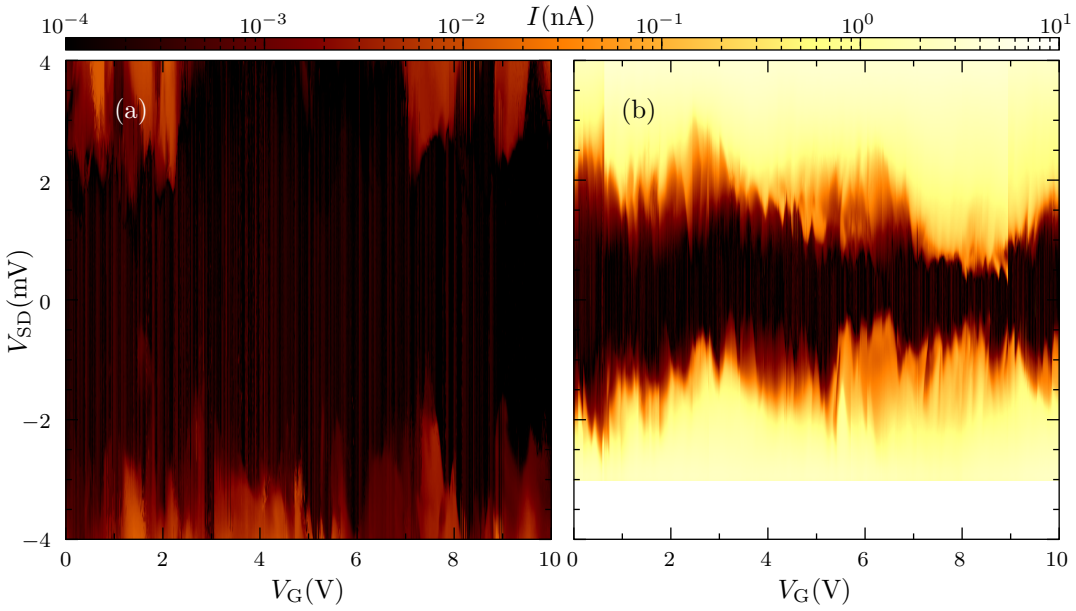


Figure 7.6.: CB measurements of device 16B (a) before and (b) after current annealing (see figure 7.7). In both graphs the absolutes current $|I_{SD}(V_G, V_{SD})|$ is plotted with a logarithmic scale as function of the gate V_G and the bias V_{SD} voltage. Prior to the current annealing, a large V_{SD} gap is visible and the current in the conducting regions is small compared to other measurements. After annealing the gap is strongly reduced and the overall transparency is increased.

Localized electrothermal annealing (or current annealing) is a known technique for improving output performance of FETs after device fabrication. A sufficiently large current is fed through the device in order to locally anneal it with the heat generated by the current. In doped SCs, this can lead to a growth of grains or thermal activation of dopants [Park et al., 2018, Bae et al., 2021, Sameshima et al., 2001]. If applied directly inside a cryostat, it was shown that the high current densities can reduce the level of contamination on the channel [Moser et al., 2007, Tanaka et al., 2010]. Similar, for planar MoS_2 transistors current annealing led to enhanced channel and contact properties [Han et al., 2018]. However, it is worth mentioning that also an accumulation of contaminants was found on some graphene devices after current annealing [Tanaka et al., 2010].

For devices on chip 16 this technique was tested *in situ* at base temperature in order to enhance transport properties and reduce the bias gap. To this end, the bias voltage was step wise increased up to value of 10 V (figure 7.7(a)), which resulted in a high current through the device. For both devices 16A and 16B a sharp increase

of the saturation current at $t = 0\,\mathrm{s}$ beyond the previous values can be observed at 9.5 V and 6.5 V, respectively. This indicates that the procedure was successful.
The source–drain characteristics shown in figure 7.7(b) further illustrate the effect of the current annealing. Prior to the treatment, a saturation current of $I_{\mathrm{sat}} \approx 35\,\mu\mathrm{A}$ (for device 16A) and 40 µA (for device 16B) as well as an ohmic behavior up to a bias threshold of 2 V for 16A were measured. After the procedure, these values increased to $I_{\mathrm{sat}} \approx 40\,\mu\mathrm{A}$ and $\approx 50\,\mathrm{V}$ for 16A and 16B, respectively, while the $V_{\mathrm{SD,\,threshold}}$ of 16A increased to $\approx 2.5\,\mathrm{V}$, confirming the success of the current annealing and suggesting an enhanced contact transparency of the devices.

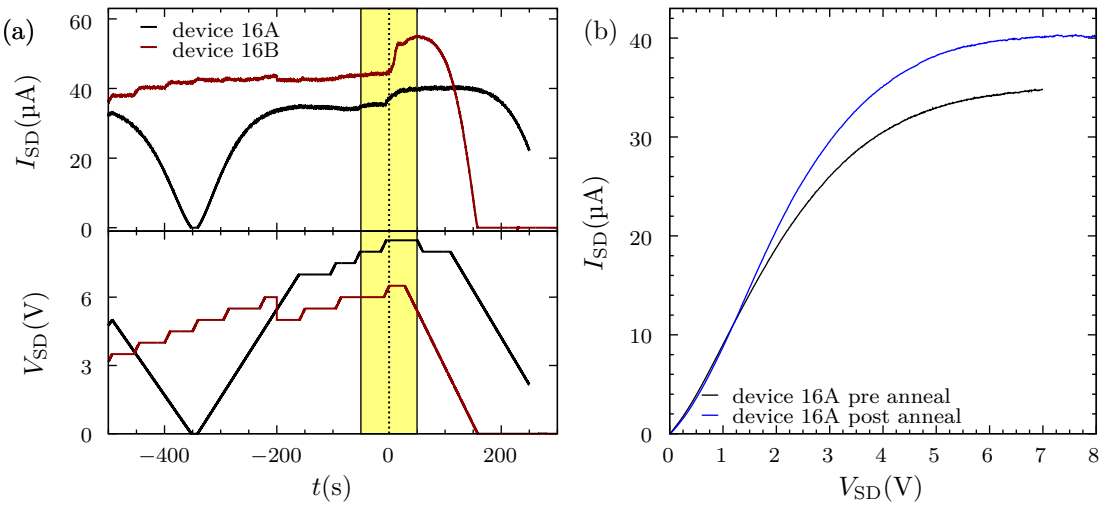


Figure 7.7.: Current annealing of devices 16A and 16B. (a) The top graph shows the source to drain current measured as the bias voltage in the bottom graph was applied. The time is shifted to the annealing event $t = 0\,\mathrm{s}$. (b) The source-drain characteristic of device 16A before and after annealing.

In figure 7.6(b), the measurements after current annealing show a strong reduction in the V_{SD} gap. At at even higher gate voltages of $V_{\mathrm{G}} = 20.3\,\mathrm{V}$ regions without any gaps are observed (see figure A.13). This clearly demonstrates the enhanced transparency through current annealing. In both measurements, the overall conductance values are strongly increased and the stability diagram shows distinct lines, which might indicate transport through single levels and possible excited states. However, the disorder as well as the strong current fluctuations, renders a quantitative assessment of the properties of the QD system impossible.
In figure 7.8, the effect of annealing on device 16A is shown. The contacts were already transparent, and a current annealing procedure was therefore not strictly

required. However, significant disorder and pronounced gate shifts were observed, which strongly limited the amount of extractable information. Consequently, current annealing was nonetheless performed in the expectation that the device characteristics might improve.

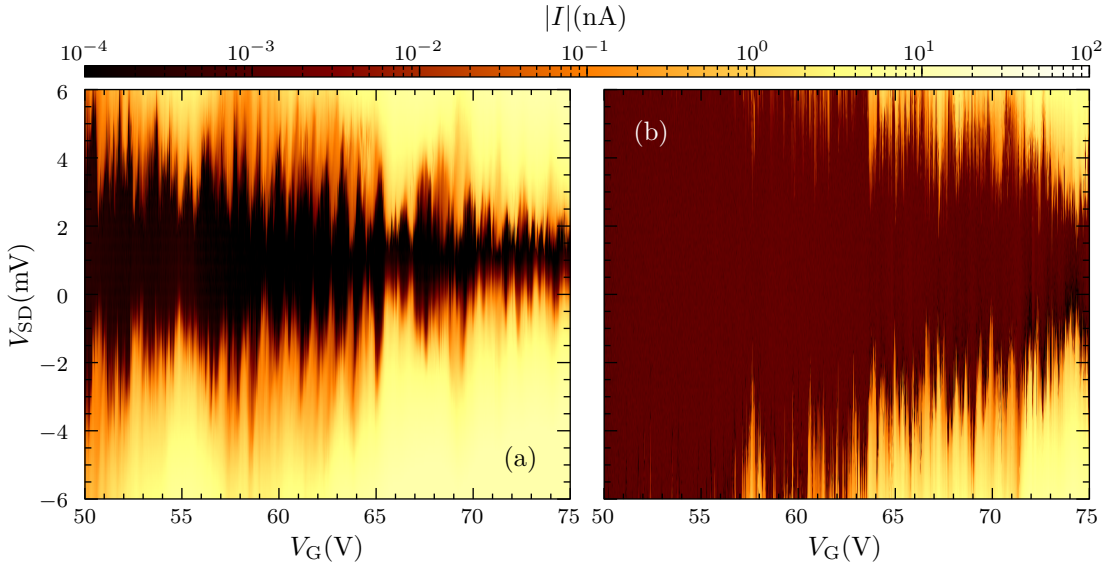


Figure 7.8.: CB-measurements performed at base temperature of device 16A before (a) and after (b) current annealing (see figure 7.7). In both graphs the absolute current $|I_{SD}|$ is logarithmically encoded in the color and plotted as a function of gate V_G and bias voltage V_{SD}. Before the current annealing, a small V_{SD} gap was observed, which slightly increased with lowering gate voltage. After the current annealing a typical band gap like feature is observed, where the bias gap increases drastically with lowering gate voltage.

Previously, the tips of the CD were coming closer together as the gate voltage was increased with a slow but steady rate (see figure A.7), indicating a band gap. After annealing the rate has drastically changed and a much faster increase of the V_{SD} gap (see figure 7.8(b)) can be observed. As previously inferred, the slow rate of increasing bias gap could be caused by a QD entering the gap with a low coupling to the gate. Therefore a steeper onset of the band gap could be an sign of an enhanced coupling between the back gate and the QD system.

In the gate range where previously nearly closing CDs were found, now a large V_{SD} gap persisted throughout the tested gate range. A representative stability diagram is in the appendix (figure A.12). Despite indications of single level transport, in the form of discrete lines, a large amount of disorder is clearly visible. Compared to the

prior measurement, the QDs inside the device seem to be of a similar size as the previously observed large scale features are no longer present.

7.3. Conclusion: Remaining Sources of Disorder

In this chapter, the successful confinement of QDs in highly suspended NTs is shown. Together with the increased fabrication yield, these results provide further evidence that the use of thicker contacts and larger metal layers can effectively mitigate the nanogap formation. In some devices, signs of single-level transport were observed. However, the measurements also revealed a persistent degree of disorder.
To address low contact quality of some devices, manifested as gaps in V_{SD}, an *in situ* current annealing technique was tested. While this approach can improve contact transparency, it seems not to resolve fundamental limitations imposed by disorder in otherwise functional devices.
When combined with the observations from the shallow-suspension devices, these findings suggest that increasing the suspension height does not by itself eliminate the disorder that limits device performance. The use of higher bottom resist layer in order to achieve even further suspension is likely to pose more challenges for successful fabrication. In view of these observations, reduction of disorder via suspension is abandoned. A possible route for further improvement is to increase the gate lever arm α and employ a more homogeneous gating environment, for example by using FLG gates. To achieve this, fabrication efforts are directed towards building NT devices on van-der-Waals heterostructures.

8. QDs in NTs on 2D Heterostructures

This chapter presents low-temperature measurements of devices on chip 7, where all devices were fabricated as 2D heterostructures, with FLG and hBN stacked using PDMS (see section 3.1.4), followed by the transfer of MoS_2 nanomaterial with anthracene crystals (see section 3.1.4). As indicated by the room-temperature resistance values, the improved fabrication process yielded predominantly low-resistance contacts (figure 5.9). This contact quality was further confirmed by cryogenic measurements, where most devices remained conducting at $V_g = 0\,V$ (see figure 8.1). However, nearly all devices exhibited leakage currents from the FLG back gates, caused either by lithographic misalignment leading to contact–back gate overlap or by damage to the hBN dielectric layers during testing. All results presented in this chapter are from device 7A, shown in figure 8.4(a), while the parameters of the other devices are listed in table A.2.

8.1. Band Gap Signature in a Nanotube-Device

Prior to a full cool-down of the dilution refrigerator (section 3.2.3), initial measurements at liquid helium temperature were performed (figure 8.1(a)). Here a region of high conductance was found above gate voltages of $V_G = 1.7\,V$, where the device was highly transparent with CB below absolute bias voltage of 10 mV. At lower gate voltages, larger blockade features start dominating the transport, with approximate charging energies up to 25 meV. After a last Coulomb peak at about $V_g = 1.45\,V$, the devices seems to enter the band gap.

The observations are similar to the ones obtain at base temperature for the NR device 1A, see figure 6.1. The main deviation is the large difference in feature size and a obvious thermal broadening. A second measurement performed during the cool-down, with temperatures below 1 K is shown in figure 8.1(b). There, a similar

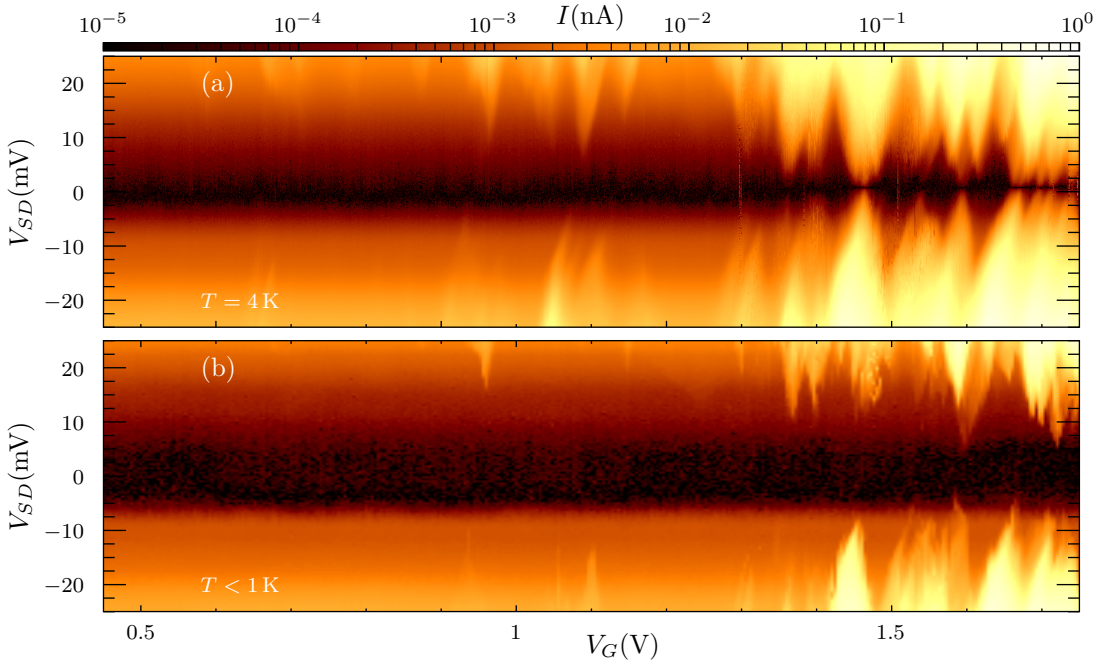


Figure 8.1.: Low temperature measurements of device 7A with the absolute current $|I_{\mathrm{SD}}(V_{\mathrm{G}}, V_{\mathrm{SD}})|$ as a function of the FLG gate voltage and the bias voltage V_{SD} logarithmically color coded. (a) Measurements at liquid helium temperature (4 K). Clear signs of CB are visible. (b) Subsequent measurement performed during the initial phase of the ^{3}He and ^{4}He mixture cooling ($T_{\mathrm{sample}} < 1\,\mathrm{K}$). The CDs previously observed are now larger and sharper. Both plots show a transition indicating the band gap cutoff voltage to be around 1.5 V.

picture is observed with disordered CDs. However, as expected the features are much sharper at lower temperatures and a change in the onset of the band gap is apparent. In the prior measurements at 4 K no bias gap was observed for $V_{\mathrm{G}} > 1.45\,\mathrm{V}$, while in this measurements it extends beyond $V_{\mathrm{G}} > 1.7\,\mathrm{V}$. It is suspected that disorder is the primary cause, since neither impurity traps would disappear at lower temperatures nor that the position of the CBM could shift. Therefore the thermal energy at 4 K is enough to overcome internal potential barriers in the NT's electronic system, while below 1 K these barriers cause a separation into a higher number of potential minima. Then a bias voltage is need to overcome the difference in chemical potentials between them.

From this difference, a very rough estimation of the energy barriers within the system can be made. Based on the thermal energy of both temperatures, these barriers are estimated to lie between 0.1 meV and 0.3 meV for 1 K and 4 K respectively. They

are thus several orders of magnitude smaller than the bias gaps that emerge at lower temperatures. This behaviour can be explained by the subdivision of the system into a larger number of shallow individual QDs once the thermal energy becomes insufficient for electrons to overcome the barriers. In this regime, each QD has its own chemical potential, and transport through the system is governed by a complex network of capacitive couplings. As a result, a larger bias voltage is required to enable conduction across the entire device.

This estimation can be used to assess possible origins of the barriers. One potential cause could be grain boundaries in the outer wall of the NT. However, for planar MoS_2, grain-boundary-induced barriers have been reported to lie in the range of 0.15 eV to 0.5 eV [Ly et al., 2016], which is roughly three orders of magnitude larger than the values found here. More likely explanations are surface contamination or inter-wall coupling effects. The precise impact of these phenomena is unknown.

These measurements demonstrate the successfully creation of a QD inside a NT on top of a 2D heterostructure. Additionally, clear signs of a band gap in a NT device were observed. Theoretical calculations have predicted a complete suppression of the band gap in MoS_2 NTs below a certain NT diameter [Seifert et al., 2000]. For double walled NTs an additional squeezing of the inner shell was also predicted to suppress the band gap [Vadseth et al., 2024]. Based upon the findings so far, where NT devices exhibited no clear band gap transition, it was suspected that this could stem from a curvature induced suppression of the band gap. However, this results clearly shows that the bang gap is still present and therefore the diameters of the MoS_2 NTs used here are to large for any curvature induced effects on the overall existence of the band gap.

8.2. Transport Properties at Base Temperature

At base temperature, the gate voltage range was increased up to 3.4 V. The measurement is displayed in figure 8.2, while figure 8.3(a) and (b) present high-resolution measurements of two selected regions. The evolution of the transport characteristics across the entire gate range reveals a gradual reduction in the size and complexity of the CB features. At low gate voltages, the spectrum is dominated by large, irregular structures and disordered CB, consistent with transport through a disordered multi-dot network. As V_G increases, these fragmented features progressively merge into more regular and smaller CDs, indicating that electrostatic barriers isolating smaller

potential minima are gradually overcome. This merging of charge islands reflects an increase in the average QD size, a corresponding decrease in the charging energy, and eventually the onset of transport at zero bias in the highest gate-voltage regime.

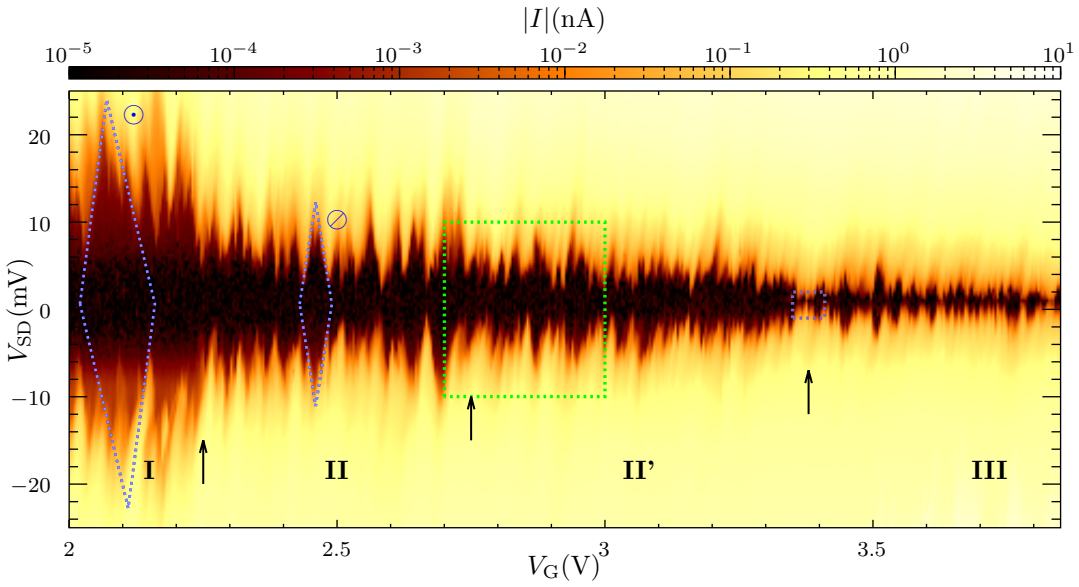


Figure 8.2.: Large gate range transport measurements of the NT device 7A. CB is clearly visible over the whole gate range. Gate voltage regions with different bias gap and feature size can be distinguished (black arrows): **I** Below $V_G = 2.25\,V$ a bias gap of about $V_{gap} = 15\,mV$ and a medium charging energy of $E_C \approx 20\,meV$. **II** Between 2.25 V and 3.4 V the gap is noticeable reduced to $\approx 4\,mV$, accompanied by a lower charging energy of $\approx 12\,meV$. **II'** Up to a gate voltage of 3.4 V the charging energy is again reduced to $\approx 9\,meV$. **III** In the last segment the V_{gap} is completely suppressed and single electron tunneling is observed at zero bias. The green and purple dashed lines mark the detail measurements displayed in figure 8.3 (a) and (b) respectively.

This behavior is similar to that observed for the device 2A (figure A.5), a NT with a similar diameter which was not placed on a 2D heterostack. Both measurements indicate a disordered QDs system with varying feature size and points where the single electron tunneling is found a zero bias voltages. The main differences between the measurement here and the one performed on device 17A are the clear observation of the band gap and the significantly larger gate lever arm α.

While the increased α is predominately caused by the much thinner dielectric, both NTs should exhibit a band gap independent of the substrate. In section 6.2 this raised the question whether the gap is suppressed by the strong NT curvature or

that the transition was merely outside the measured gate voltage range. Using the respective α values, the effective gate-induced energy shifts of both measurements can be compared. For the heterostack device a shift of $e\alpha\delta V_G \approx 0.8\,\text{meV}$ is obtained, which is only larger by a factor of 2 than the shift of $\approx 0.4\,\text{meV}$ for device 2A. The measured gate ranges are therefore comparable. Considering that the heterostack device is already inside the gap at zero gate voltage and that the effective energy shift was twice as large, it is very likely that the band gap was outside the measured gate range for device 2A.

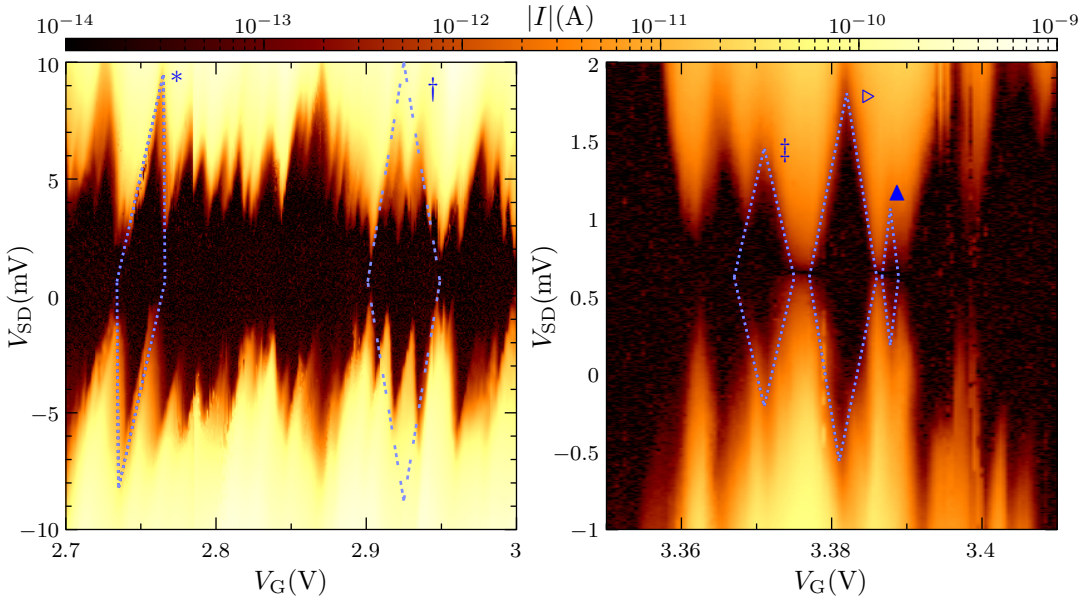


Figure 8.3.: Low-temperature ($T < 20\,\text{mK}$) transport measurements through the NT device 7A. Both panels show the absolute current $|I_{SD}(V_G, V_{SD})|$ as a function of source–drain bias V_{SD} and FLG gate voltage V_{SD} on a logarithmic color scale. (a) Overview of a broad gate range revealing CB with varying charging energies, indicative of multiple disorder-induced QDs. (b) High-resolution scan of a selected gate region where the CDs nearly close at zero bias. Representative CDs in both gate ranges are outlined by blue dotted lines with the extracted values in table 8.1.

Based on the varying feature size and bias gap, the measurement in figure 8.2 can be divided into four regions (marked with black arrows).

In the first regions, labeled **I**, the features and bias gap match the ones previously observed below $V_G \leq 1.4\,\text{V}$ of figure 8.1. From the blue outlines marked with ⊙, a charging energy of $(23 \pm 9)\,\text{meV}$ and a gate capacitance of $(1.1 \pm 0.2)\,\text{aF}$ can be estimated (see table 8.1). A bias gap of about 10 mV is found for this region.

The second region, **II**, exhibits a bis gap below 3 mV and can be further subdivided into two regions with differing feature size and a similar bias gap. While at first a characteristic charging energy of approximately (12 ± 4) meV is found this seems to be slightly reduced in the region **II'** to about (9 ± 4) meV (see marked regions in figure 8.3(a)).
Finally in the last segment, **III**, the bias gap is completely reduced and single electron tunneling is observed in irregular intervals at zero bias. Also CDs corresponding to much smaller charging energies of 0.4 meV to 1.2 meV are found in figure 8.3(b).

Table 8.1.: Estimated QD parameters based on the CD marked in figure 8.2 and figure 8.3.

region	CD	α	E_c(meV)	C_G(aF)	C_Σ(fF)	R(µm)
I	⊙	0.17(4)	23(9)	1.1(2)	0.007(2)	0.025(9)
II	⊘	0.19(4)	12(4)	2.7(4)	0.014(5)	0.05(2)
II'	∗	0.28(5)	9(4)	5(2)	0.018(9)	0.07(3)
	†	0.20(4)	9(4)	3.3(7)	0.017(7)	0.06(3)
III	‡	0.10(3)	0.8(4)	20(5)	0.2(1)	0.7(4)
	▷	0.13(3)	1.2(5)	18(4)	0.13(6)	0.5(2)
	▲	0.2(1)	0.4(4)	70(30)	0.4(3)	1(1)

Based on SEM images taken after the measurements and AFM measurements performed prior to contact deposition (figure 8.4) the device geometry is estimated. The AFM data confirm the device to be a NT of diameter $d_{NT} \approx (40 \pm 4)$ nm, while the contact-defined channel length is $L_{Channel} = (155 \pm 10)$ nm. For the heterostructure, a thickness of $d_{hBN} = (13.1 \pm 3.0)$ nm and $d_{FLG} = (15.8 \pm 3.2)$ nm for the hBN dielectric and the FLG gate respectively is determined. From these dimensions, the gate capacitances can be estimated to be $C_G^w = (14 \pm 6)$ aF and $C_G^p = (11 \pm 5)$ aF for the wire and plate model respectively (section 6.1).
Comparing the expected gate capacitance to the values extracted from the features in regions **I** and **II**, much smaller values are found. This indicates that the transport in this region is dominated by QDs with a smaller size then the actual device dimensions. However, based upon the estimated radius, atomistic defects seem again unlikely as a host for these QDs. This is further supported by an estimation of a 1 nm × 1 nm plate capacitor yielding about 0.04 aF, which is two orders of magnitude smaller then the features indicate.

In the last region (**III**), most of the diamonds exhibit gate capacitances that are comparable to the expected ones. Most likely the energy shift through the higher gate voltage was sufficient to merge the QDs into one or multiple QDs of a size similar to the active area. Unfortunately, the persistent disorder in this region also shows that still multiple QDs are present. Only the diamond marked with ▲ exceeds the calculated gate capacitances by a factor of 5. This could either indicate a QD of a much larger size then the actual devices area, probably extending both in multiple walls and underneath the contacts, or an artifact caused by the disordered CB pattern. As figure 2.25 showed, the dimensions of the emerging pattern of a multi-dot system can become arbitrary small, based upon the unknown coupling between all QDs.

In addition to the variation in diamond sizes, a significant broadening of the Coulomb peaks is visible in figure 8.2(b). Such broadening could arise from the disorder as well as charge fluctuations, which could effectively smear out the peak in a direct current measurement [Shimada et al., 1996, Isawa and Hatano, 1996]. The observed structure is also similar to measurements were, based on the Kondo effect, neighboring peaks merge into each other [Jarillo-Herrero et al., 2005, Niklas et al., 2016, Götz et al., 2019]. However, further investigations would be necessary to confirm a possible Kondo effect here. Another potential cause is leakage from the FLG back gate to a contact of a different segment of the same NT, which was grounded during these measurements. There, a leak current of about 1 nA at similar gate voltages was detected. While this corresponds to a heating power of only about 3.30 nW, such localized dissipation could be sufficient to induce measurable heating within the device.

Following the measurements shown in figure 8.3, the device failed due to a dielectric breakdown, most likely occurring within the hBN layer. Despite this, the data obtained prior to breakdown already shows the enhanced properties in terms of gate capacitance and the resulting α of 2D heterostructure devices. While the single electron tunneling at zero bias is more evidence to the transparency and quality of bismuth contacts, similar signatures of substantial disorder as for the previous suspended and unsuspended devices were found. Additionally, an absence of any sign of single level transport in the form of discrete lines in the differential conductance is observed. These observations point to further sources of disorder beyond the suspected amorphous SiO_2 surface.

8.3. Remaining Sources of Disorder

Figure 8.4 shows an optical image of the measured chip 7, combined with both pre-fabrication AFM images of the NT (a,b) and post-measurement SEM images of the devices 7A (c) and 7B (d). No surface contamination was visible in the AFM images acquired before the EBL processing, opposed to the SEM image (d) that indicates surface contamination on the exposed NT surface. It is possible that the observed bright spots correspond to residues of size below the resolution of the AFM and might only be detectable in the SEM through charging effects. As no SEM images of this particular device were taken before EBL processing this cannot be entirely ruled out. However, similar bright spots were not detected on *Scotch tape* transferred but unprocessed NT. While residues of the anthracene transfer agent are possible, this seems unlikely due to the reported levels of cleanliness [Otsuka et al., 2021]. Further SEM images prior to contact definition and deposition would be need to fully confirm these process to lead to the contamination.

Additionally, the SEM images reveal contact material protruding over the active device area. Although it cannot be fully excluded that the contact material protruding over the channel was caused by the gate breakdown that occurred during the measurements, this appears unlikely. It is therefore plausible that the metal overlap was already present prior to the breakdown and formed during the contact material deposition on the side of the resist. Instead of a complete removal by the lift-off, it probably remained attached to the contact pads and bend towards the open channel as the chip was dried. If material remains in close contact to the NT, a significant alteration of the local electrostatic potential is very likely. This could lead to the observed chaotic transport behavior.

Although the disorder in this device could be caused by metal protrusions, similar signs of disorder have been observed in most measurements performed during this project. These observations appear largely independent of the specific device type and fabrication method. This persistence suggests that the disorder is not primarily caused by the SiO_2 substrate. It is instead more likely intrinsic to the MoS_2 NTs, or at least induced by contamination during common fabrication steps. Several possible microscopic origins of such disorder are discussed in the following.

First, the **multi-wall** nature of the NTs and NRs used in this thesis is considered. It is possible that the electronic system hosting the QDs is neither confined to the outer shell nor extends continuously over multiple walls. Such a configuration

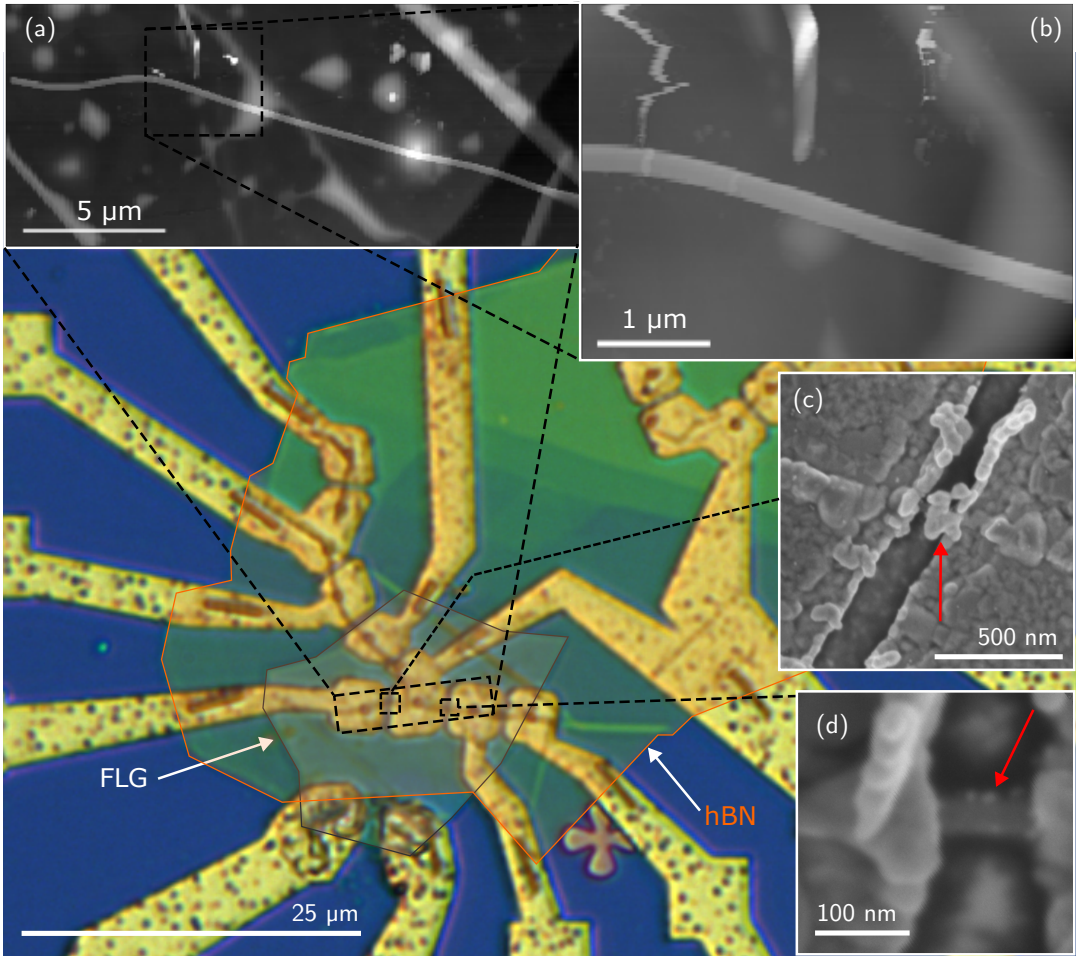


Figure 8.4.: Images of NT devices on the 2D heterostucture of chip 7. An optical micrograph, taken after the lift-off was performed, is combined with AFM images from before the contact deposition (a,b) and SEM images after measurements in the cryostat (c,d). The SEM images correspond to the devices 7A and 7B respectively. Red arrows mark contact material protruding over the NT and surface contamination on the NT surface. The outlines of the hBN and FLG flakes are marked in orange and black respectively.

could lead to separated QDs on individual layers, resulting in the observed disorder. However, this scenario would require sufficiently strong interlayer coupling at low temperatures to allow transport between the shells. For planar MoS_2, the interlayer conductance has been reported to be approximately one order of magnitude smaller than that of graphite [Das and Appenzeller, 2013]. Consequently, the coupling may be too weak to enable significant intershell transport at cryogenic temperatures. Moreover, [Vadseth et al., 2024] found larger interwall distances than the planar van-der-Waals gap for the most stable simulated configurations, suggesting an even smaller conductance between shells. Without direct measurements of the interwall conductance, however, this possibility cannot be entirely excluded.

Additionally, **Moiré patterns**, superlattice structures created between two rotationally misaligned layers, could arise between walls of different chirality. These patterns, with characteristic length scales of a few to several hundred nanometers, generate potential minima ranging from a few to several hundred meV, depending on the twist angle and material combination [Dandu et al., 2022, Zhang et al., 2021a, Tran et al., 2020]. Moiré patterns in NRs originating from mutually rotated walls have recently been observed in TEM measurements [Malok et al., 2025]. Although the reported potential depths exceed the temperature based estimates (section 8.1), the latter represent only a simple approximation, and the actual barrier height in Moiré lattices depends strongly on the twist angle. In the SEM images of a NT on SiO_2 (figure 8.5(e)), regions of varying contrast are visible, which could indicate the presence of such superlattices. However, the expected periodicity of a Moiré pattern is not observed. The disordered contrast might result from locally varying twist angles [Kazmierczak et al., 2021, Kapfer et al., 2023]. Since Moiré lattice formation in TMDC NTs remains largely unexplored, the occurrence of irregular or disordered Moiré patterns cannot be excluded. Alternatively, substrate interactions could also account for the observed features.

Structural defects within the NTs are an additional possible source of disorder. Based on the observed feature sizes and corresponding gate capacitances, sulfur vacancies can be excluded as a likely origin. Grain boundaries between different crystalline domains are also improbable given the estimated barrier heights and the reported high structural quality of NTs grown by CVT. Growth of nanostructures inside the hollow core of the NTs has been reported in the literature [Remškar et al., 2007] and cannot be excluded. Similarly, complex networks of entangled NTs could cause a disordered potential landscape. Some examples of these types of structures were

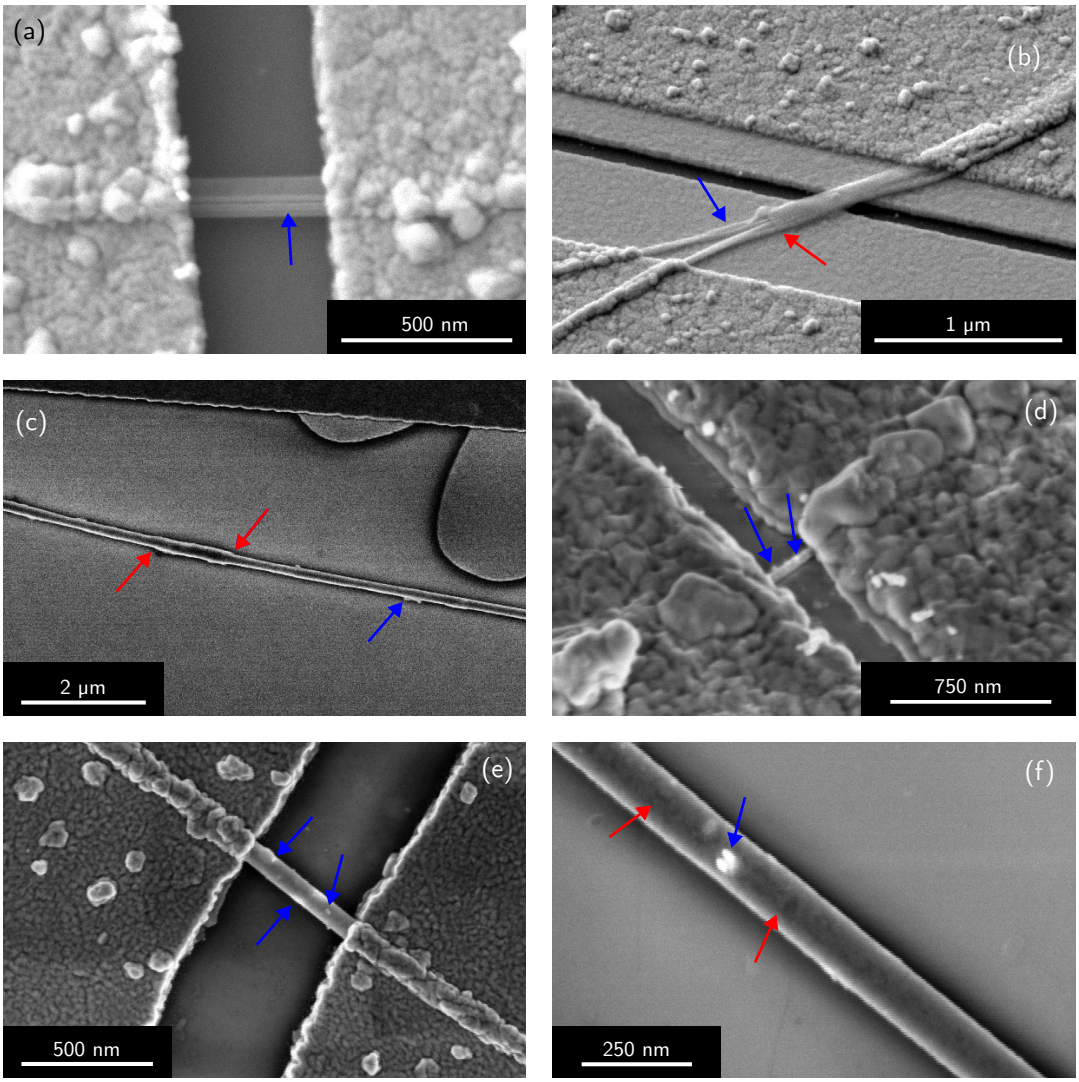


Figure 8.5.: SEM images of types of defects and contamination, which could cause disorder in low temperature transport spectroscopy. (a) Contacted NR with a region of varying contrast along the its axis highlighted with a blue arrow. (b) Bundled NTs structure transferred on gold contacts with anthracene. Highlighted is an "indent" in the smaller NT (blue) as well as the merging of both NT with a larger outer NT (red). A larger overview of this bundle can be found in figure A.14. In (c) a NT with varying diameter (red) and contamination on the surface (blue) is shown. Similar types of contamination can be seen in (d) and (e) on the active channel area of two contacted NTs. (f) Same NT as (e) in a region without contacts. It displays similar contaminations (blue) and regions of varying contrast (red). Further images can be found in Appendix in figure A.14.

found in different devices (see figure 8.5 and figure A.14). Similarly, variations in the NT thickness, as illustrated in figure 8.5(c), indicate a varying number of walls along the NT. If a shell terminates within the active device region, significant disorder may arise. However, neither entangled nanostructures nor changes in the NT thickness were observed for majority of devices measured at low temperatures.

Finally, **surface contamination**, as found in figure 8.4(d), is yet another possible source of disorder. Further such contamintaions are marked with blue arrows in figure 8.5(c), (d), and (f), and in figure A.14. These could be attributed to adsorbed or bound nanostructures, residual resist from processing, or small particles of contact material remaining after fabrication. Due to the similarity between the observed structures on the NT surface for all fabrication procedures, residues from anthracene suspected for device 7B can be ruled out.

While all of the above are potentially sources of disorder, **strategies to mitigate** their effects are very different. The **multi-wall** nature, the possible resulting **Moiré patterns**, and interlayer interactions cannot be resolved without a finding a new growth process that would yield single wall MoS_2 NTs. Additionally, the electronic configuration of multi-wall NTs itself is highly interesting and analyzing their effect on the transport properties could in turn give insights into their respective structure. Therefore a more detailed characterization of the employed NTs, including their electronic structure and possible interlayer effects, could help to better understand possible origins of disorder.

Structural defects, such as entangled NT or discontinues shells could be avoided by further SEM analysis of devices before fabrication. Thereby, these can be either excluded as sources of disorder or the effect on the transport properties can be specifically investigated.

Lastly, **surface contamination** could be reduced through further optimization of the fabrication process. A suitable post-processing step might allow the removal of surface residues without damaging the atomic structure of the NTs. One possible approach is the treatment with H_2S gas, which has been shown to heal oxygen defects in CVD-grown planar MoS_2 [Pető et al., 2018] and to improve FET performance by removing adsorbed O_2 [Byeon et al., 2024]. Similarly, H_2 plasma treatments have been reported to restore sulfur vacancies in 2D WS_2 [Marinov et al., 2021], while oxygen plasma can repair structural defects in planar MoS_2 [Nan et al., 2017]. Another promising strategy is the encapsulation of the NT between two hBN layers, which would protect the surface from contamination during wet-chemical

processing. For planar materials, such encapsulation has proven to be highly effective in mitigating contamination and providing a cleaner dielectric environment [Mayorov et al., 2011, Petrone et al., 2015, Lee et al., 2015]. Specific implementations and further strategies are discussed in chapter 10.

9. NTs in Parallel and Perpendicular Magnetic Fields

This chapter discusses transport spectroscopy measurements performed in the presence of magnetic fields. The first part focuses on measurements on device 1A, a NR fabricated on bare SiO_2 and previously introduced in chapter 6. This device exhibits a clear band gap transition and QDs operating in the single-level transport regime. The focus then shifts to device 3A, a NT likewise measured on a bare SiO_2 substrate, which shows indications of excited states in its transport characteristics. The chapter concludes with excited-state spectroscopy performed in both parallel and perpendicular magnetic fields.

9.1. Single Level Transport in Perpendicular Fields

In chapter 6, devices directly transferred onto bare SiO_2 via *Scotch tape* method were measured at cryogenic temperatures. For several devices CB was observed with features sizes indicating QD dimensions similar to the active device area. In particular device 1A, a NR with physical dimension of $270(10)\,\mathrm{nm} \times 500(10)\,\mathrm{nm} \times 18(1)\,\mathrm{nm}$ (length $\times$ width $\times$ height), displayed a temperature dependence consistent with transport through a single level (see figure 6.4). As this proves well separated energy levels inside the QD, the direct effect of a magnetic field on the energy states should be measurable. Therefore a field perpendicular to the chip surface and thereby also the NR axis is applied. In figure 9.1, the absolute current at a fixed bias voltage $V_{\mathrm{SD}} \leq 0.02\,\mathrm{mV}$ was measured as a function of the applied gate voltage at constant magnetic field values. After each gate trace, the field is incremented at a fixed rate of $50\,\mathrm{mT\,min^{-1}}$ and after a stabilizing time of 20 min the next trace is measured. This ensured a temperature of about 140 mK at the mixing chamber throughout the measurements.

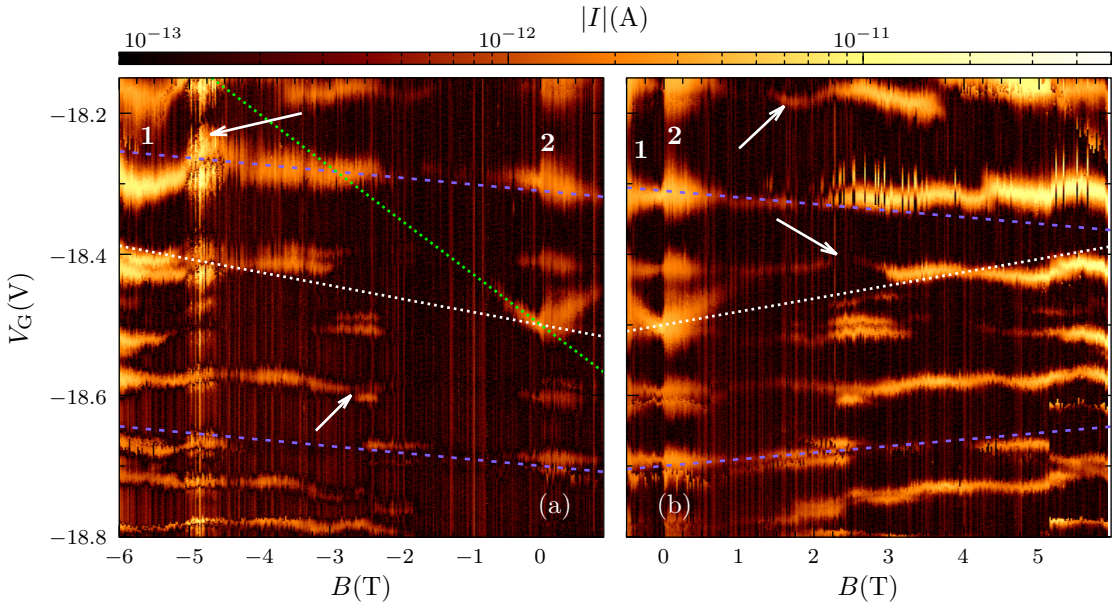


Figure 9.1.: Low-temperature transport measurement of device 1A with the absolute current $|I_{SD}(V_G, B)|$ as a function of gate and magnetic field at a fixed bias voltage $V_{SD} \leq 0.02\,\mathrm{mV}$. The current is logarithmically color coded. The magnetic field was orientated perpendicular to the NR surface with negative values being parallel and positive values antiparallel to the chip surface vector. After the first measurement (a), where the field was ramped from $-6\,\mathrm{T}$ to $1\,\mathrm{T}$, the field was ramped back to $-0.5\,\mathrm{T}$ and the measurement was continued up to $6\,\mathrm{T}$ (b). Dotted lines show the slopes of a Zeeman shift (equation (2.31)) on the Coulomb peak position for different Landé factors. (blue $g = \pm 1$, white $g = \pm 2$, green $g = 8$). White arrows mark some of the points where the slope $\mathrm{d}V_G/\mathrm{d}B$ changes sign and the label **1** and **2** mark regions of peak broadening.

From the distance to the band gap in figure 6.1, the number of electrons residing in the QD can be approximated. Using the charging energy, the gate lever arm (table 6.1), and the band gap offset of $V_{G,gap} = 21.5\,\mathrm{V}$, about 40 electrons are estimated at the Coulomb peak near $-18.5\,\mathrm{V}$. With the comparatively large number of confined charges in the NR device, a complex interplay of spin and orbital effects is expected to determine the magnetic-field dependence of the energy levels. Consequently, the levels should evolve similarly to the highest states shown in figure 2.27(b) and should even exceed the number of states displayed there, resulting in a nontrivial field dependence. Indeed, the experimentally observed peak positions in figure 9.1 display a similarly complex behavior.

Firstly, some broadening effects are obvious. For both (a) and (b) the peaks are strongly increased in width at the start of the measurements (marked with **1** in figure 9.1). This effect decays fast with the magnetic field and is suspected to be an artifact, caused by a relatively quick ramping up of the magnetic field from zero to the starting value. This increased sweep rate, which was used in order to minimize measurement time, probably heated the copper of the cold finger through eddy currents. Then, an insufficient settling time before the start of the measurement left the system thermally broadened. A second broadening effect appears with the field crossing the zero magnetic field value (marked with **2** in figure 9.1). There, a sudden increase in the line width is observed. This might also be caused by the used power supply of the magnet at the polarity switch at 0 T. However, the exact source of this broadening could not be determined. In order to mitigate these effects in later measurements, the sweep rates are reduced, settling times after reaching the starting field are increased, and additional settling time is added at zero field transitions.

Because the complexity of this measurement exceeds what can reasonably be analyzed using quantitative models, only a basic Zeeman shift following equation (2.31) is plotted alongside the data (dotted lines in figure 9.1). Most observed energy shifts follow slopes corresponding to effective g-factors of approximately 1 and 2 (blue and white dotted lines). A value of $g = 2$ is consistent with a pure electron-spin splitting and agrees with the theoretical prediction of an out-of-plane $g_\perp \approx 2$ for planar MoS_2 QDs by [Kormányos et al., 2014], as well as with several experimental reports for MoS_2 [Krishnan et al., 2023] and other TMDCs [Davari et al., 2020, Devidas et al., 2021]. In contrast, most shifts observed here follow a $g \approx 1$ trend. To the author's knowledge, such a reduced out-of-plane Landé factor has not been predicted theoretically, though values below 2 have been observed experimentally and attributed to sulfur vacancies [Krishnan et al., 2023]. Since the estimated QD size exceeds that expected for confinement at a single defect, this explanation appears unlikely. The variation in apparent g-factors may instead reflect the multi-dot nature of the device: given the extracted gate lever arms in the range of 0.0018 to 0.0037 (see table 6.1), each line in figure 9.1 could originate from a distinct QD with a different α value.

The only exception here seems to be the peak at $-18.5\,\mathrm{V}$, which seems to follow a trend corresponding to effective g-factor of 8 or larger (green dotted line). Higher then 2 factors have repeatedly been reported and attribute to a dominating effect of orbital moments [Krishnan et al., 2023, Kumar et al., 2023]. Further evidence of an interplay between spin and orbital effects are found in several kinks in many of

the lines (hinted with white arrows), which could result from a energy crossing of states with different spin alignment or angular momentum.

Some of the observed features (e.g., at $V_G = -18.5\,V$ and $B = \pm 3\,T$) appear as double peaks. A similar splitting can occur in SETs under low-frequency alternating current (AC) excitation, where rectification effects modulate the absolute current [Weis et al., 1995]. However, since both peaks exhibit the same current polarity, this mechanism can be ruled out. Given that the two peaks follow identical trends, their origin is nevertheless likely a measurement artifact.

Another noteworthy observation is that some conductance peaks exhibit a symmetric response to positive and negative magnetic fields (e.g., at $-18.5\,V$), whereas others appear clearly asymmetric (e.g., at $-18.31\,V$). In planar MoS_2, a symmetric evolution is expected, since the energy levels shift according to the state with lower Zeeman energy. This behavior was confirmed by [Krishnan et al., 2023], who reported comparable effective g-factors for magnetic fields oriented parallel and antiparallel to the normal of MoS_2 flakes. The asymmetric response observed here therefore suggests a breaking of time-reversal symmetry, possibly induced by residual magnetic moments at the contacts or by localized spins at defect sites. At cryogenic temperatures, such moments could become frozen, acting as static magnetizations that locally polarize the transport channel. Alternatively, a chirality-induced imbalance of spin–valley coupling in the nanotube geometry could lift the equivalence between opposite field directions, leading to the observed asymmetry. However, the complexity of the transport spectrum prevents a clear identification of the asymmetry's origin.

9.2. Excited State Spectroscopy in Magnetic Fields

In 2024, for the chip socket of the dilution refrigerator an *AttoCube ANRv51* rotator was installed (figure 3.11), with a rotation axis such that measurements in magnetic fields both perpendicular and parallel to the NT could be performed. This subsequently allowed for transport measurements of device 3A with fields pointing along the NT axis as opposed to the pure out-of-plane fields in prior measurements. This device was a 25 nm diameter NT contacted following the enhanced fabrication method described in section 5.5 with SiO_2 as a substrate. Due to its primary purpose of testing the new fabrication method, no attempts were made to reduce disorder by suspending the NTs or transferring them onto a heterostructures.

In figure 9.2, the stability diagram of the device at base temperature is shown. Two prominent features are immediately apparent: a transport gap of approximately $\Delta V_{SD} = 1\,\text{mV}$ and distinct line features within the conducting CDs. The large bias gap is attributed to disorder, which also leads to the irregular CB pattern. As discussed in the previous chapters, such disorder is likely introduced either by fabrication-related contamination or by intrinsic properties of the multi-wall NTs.

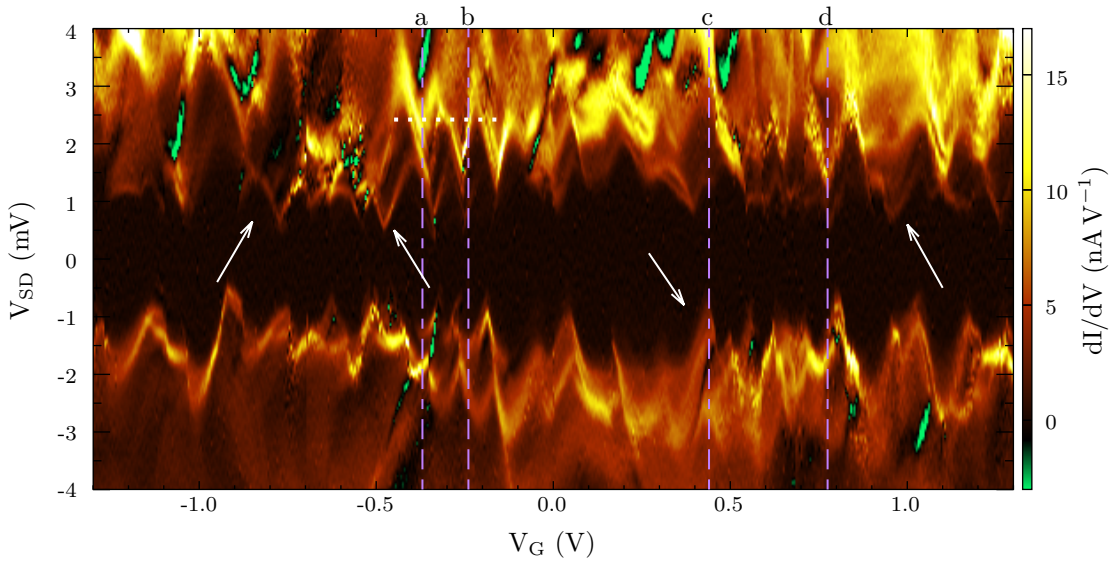


Figure 9.2.: Measurement of device 3A at $T < 30\,\text{mK}$. The numerically derived differential conductance is plotted as a function of gate V_G and bias voltage V_{SD}. Typical patterns of disordered CB are visible. The white arrows highlight additional lines inside the conducting region, indicating transfer through excited states. The purple dashed lines labeled a, b, c, and d mark the gate voltage cuts used for the bias and gate sweeps measured in figure 9.5. The white dotted line marks the fixed V_{SD} cuts displayed in figure 9.5.

In contrast to the previous chapters, the line features within the conducting diamonds indicate that at least some of the QDs in the system have entered the single-level transport regime. In several cases, transport through excited states is observable, further supporting the interpretation that a subset of the QDs is sufficiently small confined and has a level spacing larger then the thermal energy.

Based on the slopes of the diamond region edges around $V_G = -0.23\,\text{V}$ (purple dashed line labeled b), $\alpha = 0.0097 \pm 0.0020$ is estimated. Over the whole measurement range, the charging energy seems to be in the range of 0.5 meV to 2.0 meV and the gate capacitance between 0.4 aF to 1.6 aF. These values are similar to the ones found for

other NT devices with SiO_2 as the dielectric substrate (see table 6.1). Unfortunately, the gate range for this devices was limited, as a gate leak to a adjacent segment of the NT caused severe heating of the devices at higher voltages. Therefore, neither the onset of the band gap nor possible regions of zero bias gap at higher gate voltages could be tested.

9.2.1. Temperature Dependent Measurements

In order to test the transport regime, temperature dependent measurements were performed similar to section 6.3. In contrast to the measurements then, the device temperature is now also monitored through a probe directly at the sample holder. The results are shown in figure 9.3. As no Coulomb peaks were observed at zero bias voltage, the evolution of bias sweeps at a fixed gate voltage are studied ($V_G = -234\,\mathrm{mV}$, puple line b). In (a) the bias sweeps for each temperature are shown, fitted with a Fermi function to capture the thermal broadening of the carrier distribution in the leads.

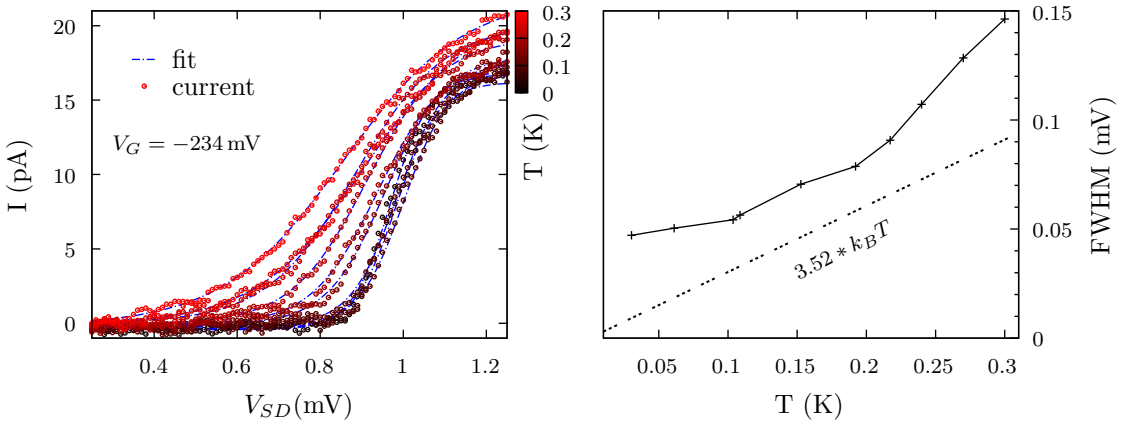


Figure 9.3.: Temperature dependence source-drain characteristic of the NT device 3A. (a) The drain current as a function of the applied bias voltage at different cold finger temperatures is indicated by color. A Fermi function is used to fit the bias traces, in order to extract the FWHM of each trace. (b) The FWHM as a function of cold finger temperature. The black dashed line indicates the thermal broadening from the leads expected from equation (2.28).

Figure 9.3(b) presents the temperature dependence of the FWHM of the CD edge, which decreases as the temperature is lowered. The dashed line marks the expected thermal broadening of the leads, calculated from equation (2.28). The experimental

data follow this trend, with deviations appearing below 100 mK and above 220 mK. On the high-temperature side, a second current step was located just outside the measurement window. As this step becomes increasingly broadened with rising temperature, the main and second current step begin to overlap, which leads to an apparent increase in the FWHM extracted from the fit. The saturation observed at the lowest temperatures might be attributed to a transition from thermal broadening to a lifetime-broadened regime, indicating that transport takes place through a single discrete level. This allows for a rough estimation of the tunneling energy of about $\hbar\Gamma \approx (0.05 \pm 0.02)$ meV. On the other hand, the device temperature could also saturate above the probe thermometer leading to the observed stagnation of the FWHM.
However, since the temperature-dependent peak broadening mechanisms discussed in section 2.4.3 are considered in the linear transport regime (i.e., at 0 V bias), the derived constants might be different at higher bias voltages. Therefore the interpretations presented here remain speculative.

9.2.2. Perpendicular and Parallel Magnetic Fields

CB measurements were performed at magnetic fields of 6 T, applied in the chip surface plane but both parallel and perpendicular to the NT axis. The results are presented in figure 9.4, together with a reference plot at zero magnetic field. While the transport characteristics remain similar under parallel magnetic fields, the application of a perpendicular field leads to a pronounced increase of the bias gap. In addition, the conductance at negative bias voltages is almost completely suppressed within the measured bias range.
This behavior is unexpected, as one would anticipate a response similar to that reported for CNTs. There, the direction with the largest magnetic field response is typically parallel to the NT axis, whereas perpendicular fields only have a weak impact [Minot et al., 2004]. Due to the tubular geometry and corresponding symmetry, the electrons "orbit" around the circumference, allowing the angular momentum to efficiently couple to the axial magnetic field. A similar effect has been anticipated for TMDC NTs, and [Milivojević et al., 2020] predicted a spin polarization oriented along the NT axis.
To investigate this further, magnetic field sweeps were carried out at fixed gate voltages, with the field applied both parallel and perpendicular to the NT as shown in figure 9.5. All resonances under parallel magnetic fields exhibit only a relatively

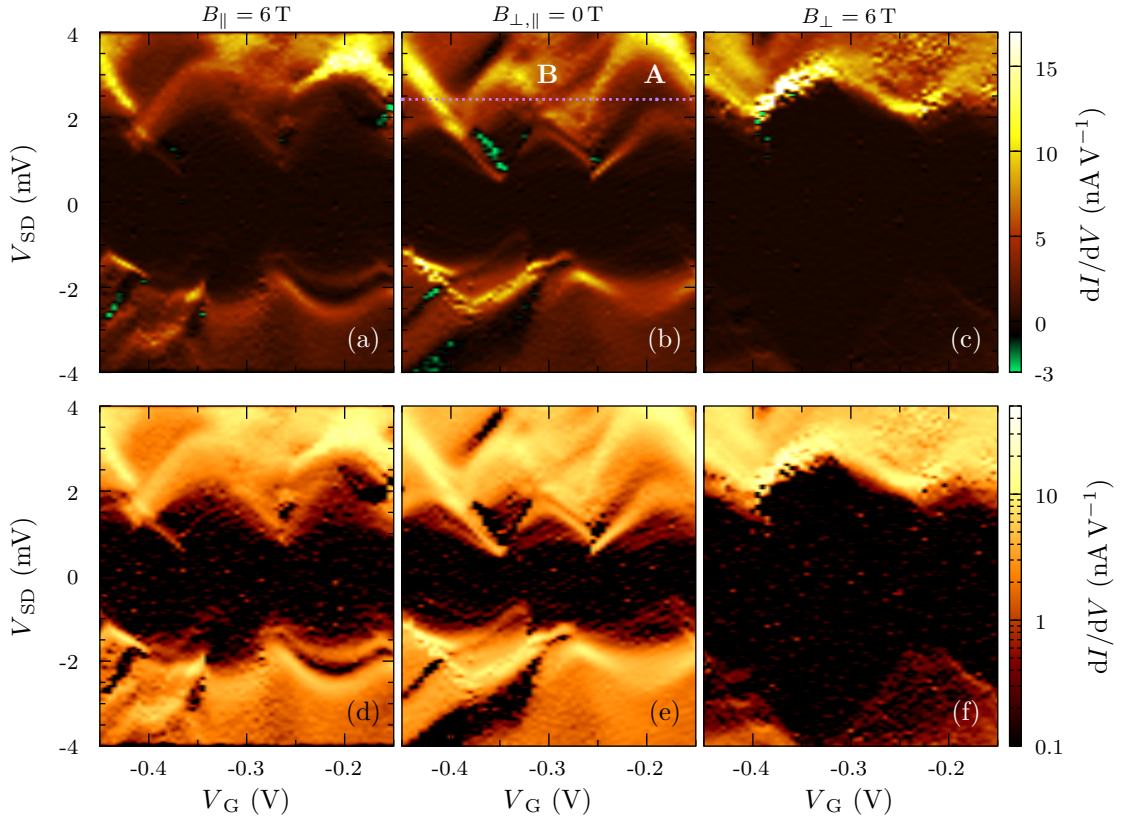


Figure 9.4.: Magneto-transport measurement of device 3A at (a) 6 T parallel, (b) 0 T, and (c) 6 T perpendicular field linearly color coded and logarithmically color coded in (d, e, f) respectively. The numerically derived differential conductance is plotted as a function of gate V_G and bias voltage V_{SD}. The measurement range of figure 9.6 is marked with a purple dashed line together with the points **A** and **B**.

small response to the magnetic field. In contrast, perpendicular magnetic fields lead to both weakly and strongly field-dependent features, indicating that for different levels in the spectrum different coupling mechanism may exist.

A recurring feature in the perpendicular field sweeps is the strong suppression of conductance at negative bias voltages. This behavior typically sets in at magnetic fields between 1 T to 2 T, corresponding to a magnetic length of $l = 25\,\mathrm{nm}$ to 18 nm, which is comparable to the diameter of the NT. When the magnetic length approaches the spatial extent of the electronic system, the field can modify the wave function of the electrons [Fock, 1928, Kouwenhoven et al., 2001]. The fact that the suppression occurs for both positive and negative perpendicular fields and that it consistently switches from the negative to the positive bias side when source and

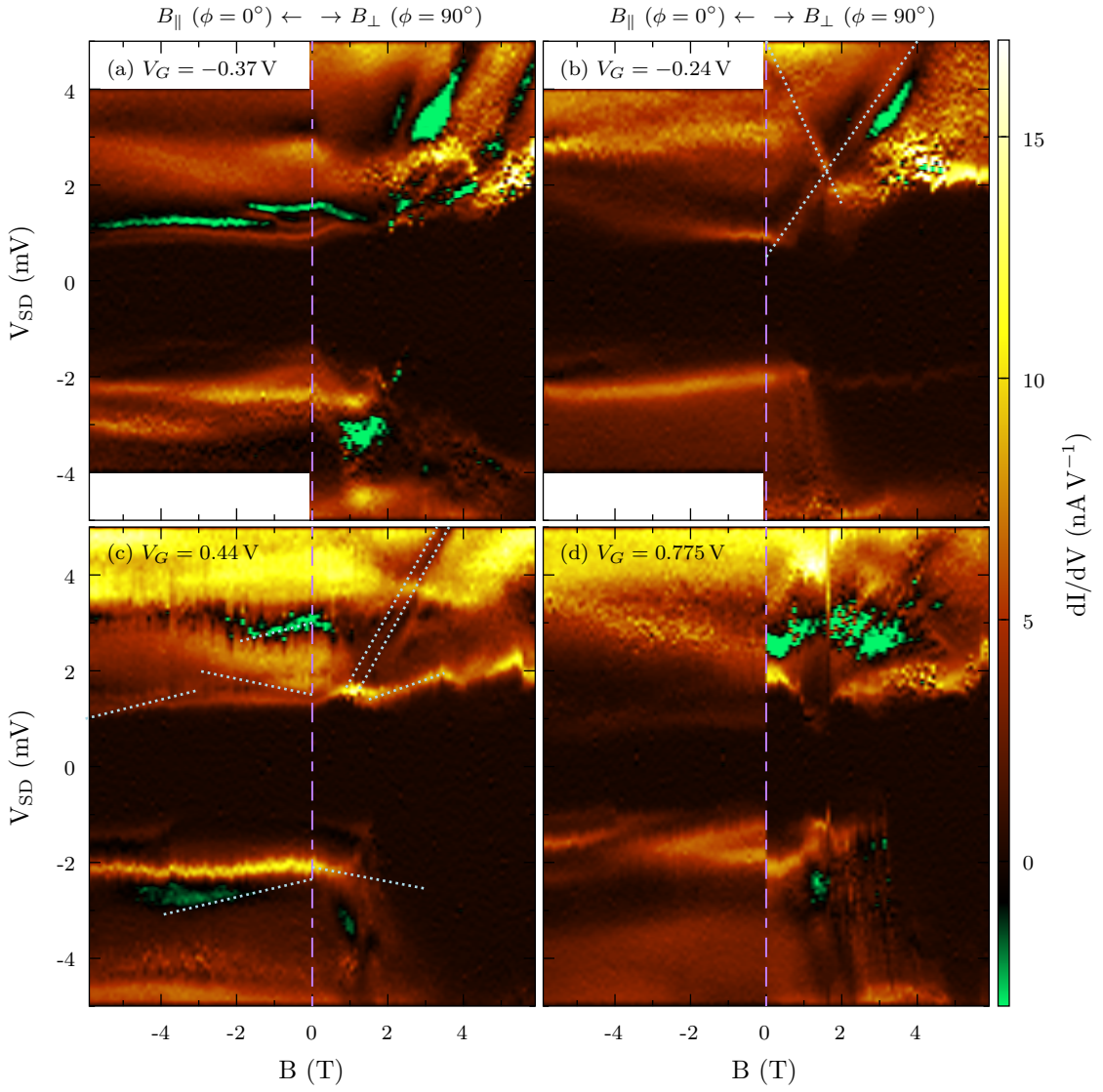


Figure 9.5.: Magneto-transport measurements at the fixed gate voltages marked with a, b, c, and d in figure 9.2 corresponding to the figures (a), (b), (c), and (d). Plotted is the numerically derived differential conductance as a function of bias voltage V_{SD} as well as the parallel and perpendicular field for $B < 0$ and $B > 0$, respectively. At the purple dashed lines the measurements performed with the magnetic field parallel to the NT ($B < 0$) and perpendicular to the NT ($B > 0$) are stitched together. In (b) and (c) some exemplary conductance lines are marked with white and blue dotted lines.

drain contacts are interchanged, indicates that it is caused by an inherent property of the measured device.

The observed asymmetry could originate from a mechanism analogous to the *Pauli blockade* [Ono et al., 2002, Johnson et al., 2005]. In such a process, the current through a double QD is suppressed depending on the spin configuration of the involved charge carriers. If, for instance, the second QD is already occupied by an electron, only another electron with opposite spin can tunnel from the first to the second QD. An electron with the same spin orientation is blocked from entering the second QD. Since spin relaxation processes within the first QD typically occur at rates much lower than the electron tunneling rates in the conducting state, the blocked electron remains trapped in the first QD for a comparatively long time, resulting in current suppression. In the reverse bias direction, such suppression is not expected, since the tunneling occurs first in to the selective level from which the electron with a fixed spin orientation can freely tunnel into the second QD.

To quantitatively assess the field dependence, the slopes of the resonances marked with dotted lines in figure 9.5(c) are analyzed as a representative example. For this region, a conversion factor of $(0.33 \pm 0.04)\,\mathrm{eV\,V^{-1}}$ between the bias voltage and the level spacing can be extracted, which is used to estimate the magnetic-field-induced energy shifts. In the case of a parallel field this yields predominantly slopes of $(0.10 \pm 0.03)\,\mathrm{meV\,T^{-1}}$ and $(0.05 \pm 0.02)\,\mathrm{meV\,T^{-1}}$, corresponding to g-factors of 0.9 ± 0.4 and 1.7 ± 0.7, respectively. The relatively large uncertainties reflect the broad distribution of slopes observed. It is possible that not all of the features originate from the same QD and therefore should not share a single conversion factor.

For perpendicular magnetic fields slopes of $(0.11 \pm 0.03)\,\mathrm{meV\,T^{-1}}$ and $(0.40 \pm 0.05)\,\mathrm{meV\,T^{-1}}$ are found, corresponding to Landé g-factors of 1.9 ± 0.7 and 6.9 ± 0.5, respectively. These values are comparable to those reported by [Krishnan et al., 2023] for in-plane and out-of-plane fields in planar MoS_2. [Krishnan et al., 2023] ascribe their confinement to S-vacancies. Here, however, the gate capacitances, magnetic-length-based size estimates, and charging energies observed render vacancy-induced confinement in the NTs unlikely.

9.2.3. Estimation of the Spin-Orbit-Coupling

Another feature observed in figure 9.5(b) is a pair of lines (β and γ) with opposite slope signs that intersect at approximately 2 T. Following the analysis

of [Kuemmeth et al., 2008] (see figure A.15), a similar crossing appears in the $V_{SD} = 2.42\,\mathrm{mV}$ plane (see figure 9.6). Since the lines shift collectively along V_G when the applied bias is increased (see figure A.16), while their mutual spacing and slopes remain constant, a disorder-induced origin appears unlikely. This behavior instead suggests that all lines originate from the same electronic system.

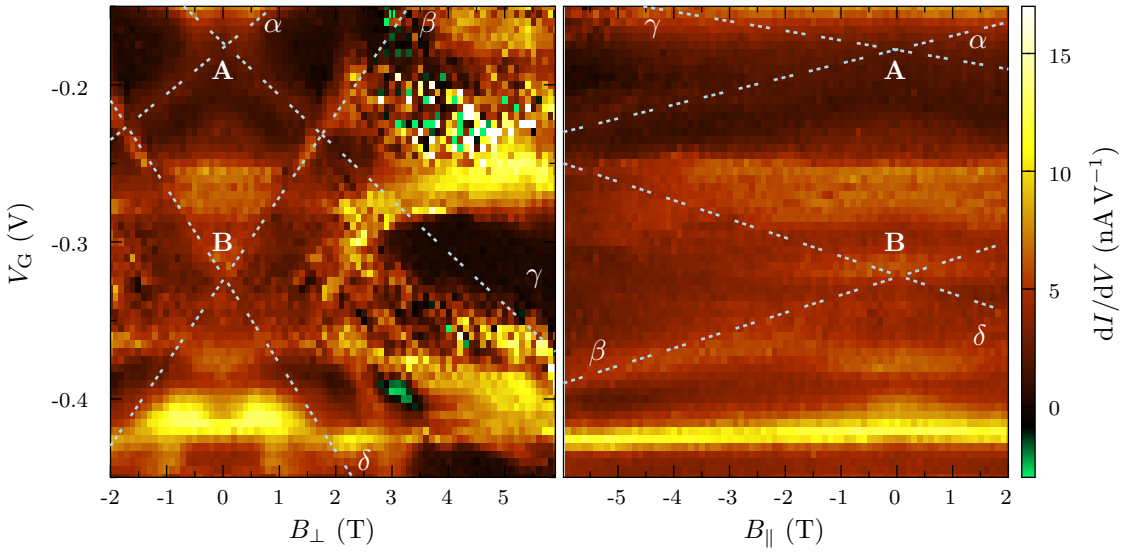


Figure 9.6.: Magneto-transport measurements of the NT device 3A at a fixed bias voltage of $V_{SD} = 2.42\,\mathrm{mV}$ for (a) perpendicular and (b) parallel magnetic fields. The numerically derived differential conductance is plotted as a function of V_G and V_{SD}. The dashed lines denoted with α, β, γ, and δ highlight transport through excited states. **A** and **B** mark the crossing points of the lines at zero field located at the same gate voltage for both field directions. Measurements at different bias voltages are shown in figure A.16 and figure A.17 for perpendicular and parallel fields, respectively.

In the case of a CNT, [Kuemmeth et al., 2008] demonstrated that the excited states of the first electron occupation correspond to the spin and valley degrees of freedom. The four lines observed in the stability diagram therefore arise from the four possible spin–valley combinations. In the absence of SOC, these states are degenerate at zero magnetic field (see figure A.15(a)), and their energy shifts depend on whether the applied field is parallel or antiparallel to the electron spin and to the magnetic moment associated with the valley circulation around the NT (see figure 2.9). When SOC is present, this zero-field degeneracy is lifted (see figure A.15(b)). Depending on whether the spin and valley moments are aligned or opposed, the respective configurations become energetically more or less favorable. While the slopes of the

transitions remain unchanged compared to the case without SOC, two crossing points appear at 0 T. A new degeneracy emerges at finite magnetic field, here $B = 2\,\mathrm{T}$, where the external field compensates the effective magnetic field induced by SOC for the opposite spin states within the same valley.

In the present measurements, the precise electron occupation cannot be determined due to the underlying disorder. Nevertheless, a similar picture as described above appears applicable to the situation in MoS_2. In planar TMDCs, optical transitions between the valence and conduction bands are valley-selective and can be driven by circularly polarized light at the K and K' points [Xiao et al., 2012]. An external magnetic field introduces an additional Zeeman splitting between these transitions [Li et al., 2014, Wu et al., 2018]. Consequently, the energy levels in a MoS_2-based QD are expected to shift with magnetic field in a manner analogous to the CNT case, depending on the spin and valley orientation. For QDs a twofold valley degenerate energy spectrum is expected, with the same Kramers doublets due to time reversal symmetry as in CNTs [Széchenyi et al., 2018, Bieniek et al., 2020]. In MoS_2 NTs, the spins are predicted to align along the NT axis [Milivojević et al., 2020], suggesting an almost identical field dependence as for CNTs. When combined with the theoretically predicted SOC in planar MoS_2 QDs [Kormányos et al., 2014] and for chiral NTs [Milivojević et al., 2020], the features observed in figure 9.5 could indeed reflect the same underlying physical mechanisms [Shandilya et al., 2024]. Based on this similarity to the measurements of [Kuemmeth et al., 2008], the data are therefore analyzed to extract the spin–orbit coupling Δ_{SO} and the effective g-factor.

To extract the energy difference the gate lever arm mentioned above ($\alpha \approx 0.0097 \pm 0.0020$) is used. In accordance with [Kuemmeth et al., 2008], states with different angular momentum and parallel spin are expected to be degenerate in the absence of a magnetic field. The SOC causes a splitting of the antiparallel spin states. From the gap at $B = 0\,\mathrm{T}$, a value of $\Delta \approx (1.5 \pm 0.3)\,\mathrm{meV}$ is extracted. For small valley mixing ($\Delta_{KK'} \ll \Delta_{\mathrm{SO}}$) the splitting would be dominated by SOC and $\Delta \approx \Delta_{\mathrm{SO}}$, which gives a value consistent with the scale of the spin splitting of the conduction band of a QD in planar MoS_2 [Kormányos et al., 2014]. Based on the energy difference between lines of similar inclination, a Landè factor of $g = 2.2 \pm 0.3$ is calculated, which is in good agreement with the predicted value of 2 [Kormányos et al., 2014].

For magnetic fields applied parallel to the nanotube axis (figure 9.6(b)), the features are notably less distinct. As it was previously observed, the overall response to the magnetic field is reduced compared to the perpendicular configuration. Nevertheless,

several features appear at increasing bias voltages, exhibiting constant slopes and a fixed spacing between them (figure A.17). The outlines shown in figure 9.6(b) are based on these features and were used for a tentative analysis. From this, a spin–orbit coupling comparable to that extracted at zero field and an effective g-factor of 0.8 ± 0.4 were obtained.

9.2.4. Interpretation Related to the Microscopic Confinement

While the observed features are qualitatively similar to those reported for CNTs by [Kuemmeth et al., 2008], a key difference is that the most pronounced response in this measurement occurs for perpendicular rather than parallel magnetic fields. As illustrated in figure 2.10, a perpendicular magnetic field in CNTs induces a Zeeman shift of the parallel and anti-parallel spin–valley states, but no additional splitting, if the valley mixing $\Delta_{KK'}$ vanishes. In the present data, such behavior is not observed for either field direction. Instead, both field directions exhibit a splitting into four states. In CNTs, a finite $\Delta_{KK'}$ is known to give rise to a Zeeman splitting in perpendicular fields, with an effective g-factor ranging from 0 for $\Delta_{KK'} \ll \Delta_{\mathrm{SO}}$ and 2 in the opposite limit. For planar MoS_2, an in-plane $g_\parallel = 0$ is expected, although disorder can introduce valley mixing that leads to $g_\parallel > 0$ [Széchenyi et al., 2018, Krishnan et al., 2023]. Therefore, such valley mixing may also occur in the NT device 3A investigated here, giving rise to finite g-factor for both perpendicular and parallel fields as

$$g_\parallel = g_\perp \frac{\Delta_{KK'}}{\Delta_{\mathrm{SO}}}.$$

Together with $\Delta_{\mathrm{SO}} \approx (1.5 \pm 0.3)\,\mathrm{meV}$ this would give a valley mixing of about $(0.5 \pm 0.4)\,\mathrm{meV}$. This value is similar to theoretical calculations of intervalley mixing caused by impurities (Mo-, S-vacancy, adatoms) of 0.15 meV to 1.5 meV [Széchenyi et al., 2018]. At this stage, the impurity that could lead to this mixing cannot be explicitly determined.

Even though disorder can explain the observation of a finite g-factor in both directions, it is surprising that the MoS_2 NT behaves more like a MoS_2 planar layer and less like a CNT with its tubular symmetry, where the effective g in axial direction is larger. From theory, both a SOC in the CBM and a spin polarization in chiral NTs are expected, but with a highly irregular diameter dependent Δ_{SO}

[Milivojević et al., 2020]. Nonetheless, this should lead to a stronger response in the in-axis direction. This discrepancy can be explained by two possible mechanisms:

- The observed disorder alters the system such that it no longer represents an electronic state extending over the entire NT, suppressing tubular symmetry.
- The spin orientation in MoS_2 NTs fundamentally different from the anticipated orientation.

In figure 9.2 a high level of disorder was already apparent and therefore a disorder based explanation seems very plausible. Additionally to the suspected valley mixing term, the data suggests an interplay of multiple QDs. In section 8.3, surface contaminates and disordered Moiré patterns were discussed as the most likely sources of disorder. This raises the question of the exact location of these QDs in or on the NT. Under the assumption that coupling between the walls of the NT is indeed small enough, the QDs should exist in the outer shell. As strain induced by curvature reduces the band gap in MoS_2 NTs [Seifert et al., 2000], and substrate interaction seems to flatten the NTs (see figure 2.14), the NT sides could host states with a reduced band gap compared to top and bottom. This is in accordance with experimental observations using contact current imaging microscopy of a semi-metallic state at the high curvature edges of the pancake like NRs [Malok et al., 2025]. These sites, located near the edges of the flattened NT (see figure 9.7), could provide favorable conditions for QD localization. Confinement may then arise either from a local reduction in strain or from additional barrier-forming mechanisms, such as the previously discussed Moiré patterns. A schematic illustration of the possible QD locations is presented in figure 9.8.
Such a localization mechanism would also naturally account for the observed magnetic response. When the external field is aligned with the NT axis, all QDs localized in small portions of the NT wall experience it as an in-plane orientation. By contrast, for a field applied perpendicular to the axis (but in-plane relative to the chip surface), QDs at the flanks of the NT are subject to an out-of-plane component, while those at the top or bottom still experience an in-plane configuration. In this picture, the measurements cannot be interpreted as the response of a coherent tubular state, but rather as that of a collection of quasi-planar QDs with different orientations. As each individual QD would then represent a quasi planar MoS_2 QD no angular moment can arise from movement around the NT. Therefore, the usual out-of-plane

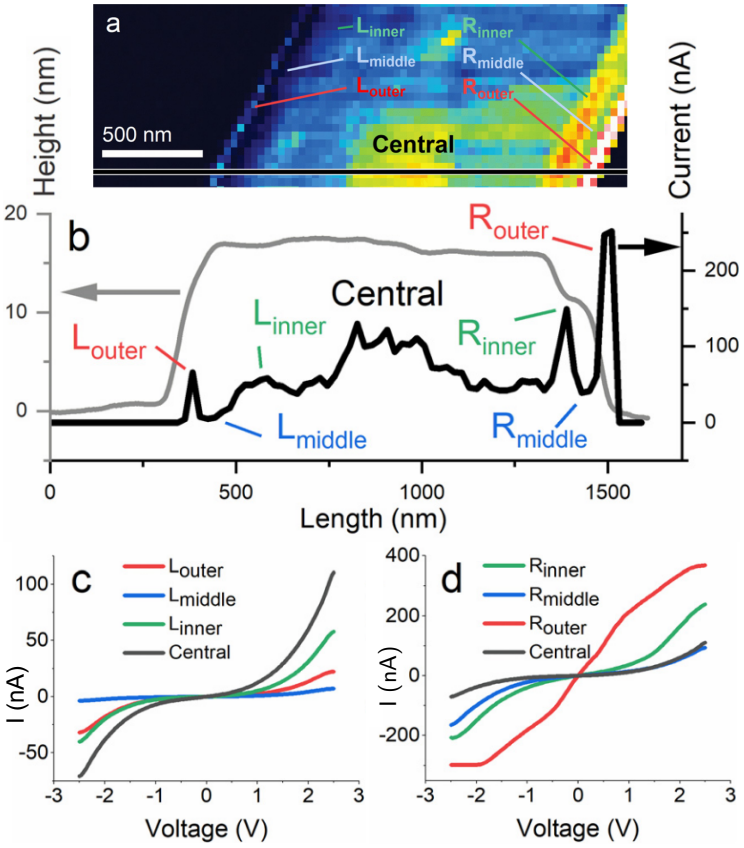


Figure 9.7: Room-temperature contact current imaging microscopy of a MoS_2 NR. (a) Full image taken at 1.6 V over the complete width of the measured device. (b) Topography (grey) and current (black) along the black line in (a). (c and d) Averaged current over bias voltage graphs of the left and right edges, respectively. Figure from [Malok et al., 2025].

spin polarization should be expected. This scenario is consistent with the distinct g-factors observed for the two alignments, as well as with the pronounced differences in the slopes obtained for perpendicular orientation. Depending on their position along the nanotube circumference, individual QDs thus experience a varying superposition of in-plane and out-of-plane components.

This hypothesis could in principle be tested by measurements at elevated gate voltages. In this regime, the individual QDs could merge into a single state extending across the entire device, and Coulomb peaks at zero bias voltage should become observable. Under such conditions, the anticipated CNT-like response might emerge. However, due to gate leakage, these measurements could not be carried out on the present devices. Additionally, the strong electronic field could lead to a symmetry breaking due to its direction from the chips surface. In future devices this could be further investigated by comparing devices on a "classical flat" backgate or rotational symmetric gating strategies like NTs suspended in iconic liquid or encapsulated in hBN and CNT shells.

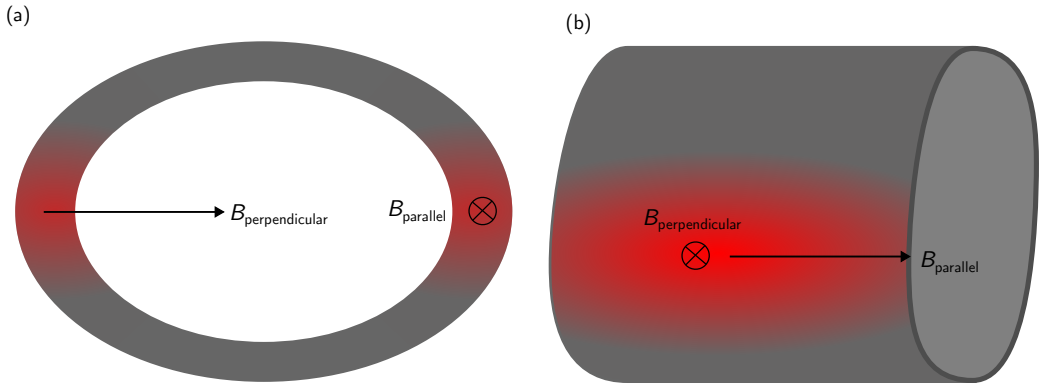


Figure 9.8.: A possible configuration of the QDs inside the NT measured in sample 3A. (a) View in NT axis direction. (b) Side view of the NT. The red regions mark possible locations of QDs.

On the other hand, it cannot be ruled out that the measured devices behave differently from theoretical expectations. So far, the models used for calculating the bandstructure of TMDC NTs were not tested as extensively as for the CNTs, but predicted optical spectral match experimental data [Milosevic et al., 2007]. Therefore, it seems reasonable that the previous assumptions about the electronic configuration are valid and comparable to the CNTs. The direction of the spin polarization, however, might be a different story. Considering the movement of electrons in a NT, the periodic boundary condition along the circumference should naturally give rise to a quantized angular momentum around the NT. This causes a magnetic moment in the NT direction. In the case of CNTs, where its flat counterpart graphene has almost no SOC, this leads to the emergence of the Kramers doublets with a spin polarization along the NT axis [Minot et al., 2004, Flensberg and Marcus, 2010]. While a similar processes could be possible in a MoS_2 NT, their planar counterparts already exhibit SOC, which locks the spins into the out-of-plane direction. Based upon the symmetry, [Milivojević et al., 2020] expected a spin polarization along the NT axis, however they only considered NTs of diameters below 10 nm.

In a simplified picture, two limiting cases can be considered: a NT with an infinite and one with a very small radius. In the infinite-radius limit, the properties of planar 2D MoS_2 are recovered, as curvature effects vanish and the periodic boundary condition effectively moves to infinity. In contrast, for very small radii, the behavior is expected to follow the discussion above, where curvature plays a dominant role. Between these two limits, a transition must occur at a characteris-

tic radius. This crossover is expected when the nanotube circumference becomes comparable to the electronic mean free path or the coherence length. Estimates from electrostatically defined QDs and superconducting MoS_2 yield characteristic lengths of approximately $l \approx 150\,\text{nm}$ [Pisoni et al., 2018] or $\approx 1\,\text{nm}$ to $30\,\text{nm}$ [Saito et al., 2016, Zheliuk et al., 2019], respectively. The 25 nm-diameter NT studied here thus lies within the regime where such a crossover may occur. In this range, competing effects are expected: the SOC locks the spin orientation out-of-plane of the side wall, while the cylindrical symmetry of the NT favors alignment along the NT axis. With decreasing radius, the latter interaction should become increasingly dominant. Figure 9.5 suggests, that the out-of-plane locking of planar MoS_2 still seems to exceed the effect of tubular geometry.

A comparable behavior has been reported for superconducting WS_2 NTs. As shown in figure 2.4, superconductivity is strongly suppressed by perpendicular magnetic fields, whereas it persists for parallel fields with a breakdown field exceeding the Pauli limit [Qin et al., 2017]. This resembles the case of odd-layer 2D TMDC systems with broken inversion symmetry, where superconductivity is protected against in-plane but not out-of-plane fields [Saito et al., 2016, Zheliuk et al., 2019]. In the planar case, the SOC induces an effective out-of-plane magnetic field that locks the spins parallel or antiparallel to it, enabling Cooper pairing between electrons in opposite valleys. While an out-of-plane field readily flips the spins, an in-plane field must first overcome $B_{\perp,\text{eff}}$ to destroy the pairs. By analogy, this suggests that the spins in WS_2 NTs are predominantly oriented out-of-plane, i.e., in a radial direction.

[Qin et al., 2018] further observed that the critical temperature decreases with decreasing nanotube radius, which they attributed to curvature-induced modifications of the phonon coupling [Qin et al., 2018]. However, this trend could also indicate a gradual weakening of the out-of-plane spin locking as the curvature increases, thereby reducing the likelihood of Cooper pairing at higher temperatures. Their study was limited to outer radii down to 70 nm, for which the critical temperature decreased inversely with radius. Whether superconductivity reemerges at even smaller radii remains speculative.

The results of [Qin et al., 2018] together with those presented here may indicate that the dominant spin polarization in MoS_2 NTs still points out-of-plane, with spins oriented radially relative to the NT axis. The persistent disorder in devices 3A prevents a conclusive verification of this hypothesis. Further experiments on cleaner devices, or on NTs with controlled chirality and smaller diameters, are required to

test whether the spin polarization eventually rotates into the NT axis. The diameter studied here might still be too large for such a transition to be observable.

10. Summary and Outlook

The miniaturization of classical semiconductor devices is approaching fundamental limits, where short-channel effects and power dissipation prevent further scaling. At the same time, quantum information processing requires materials that allow robust confinement and control of quantum states. A promising platform which could both overcome limitations of in classical computers and serve as a platform for QDs is the 2D-semiconductor MoS_2. Its relatively large electron mass, however, demands very short confinement lengths, a challenge that is solved in this work through the use of quasi-one-dimensional NTs, where only a single dimension requires lithographic definition.

As for most two-dimensional semiconductors, achieving low-resistance and non-invasive contacts to MoS_2 NTs has proven difficult. Conventional metal deposition frequently introduces disorder and Schottky barriers, leaving contact resistance as a major bottleneck for quantum transport studies. In this work, the successful fabrication of non-destructive, transparent, and reliable contacts using the semimetal bismuth, which had been found to create ohmic contacts to planar MoS_2 [Shen et al., 2021], is demonstrated. Substantial evidence indicates that bismuth is the most suitable of the materials investigated, and the regime in which the contact resistance no longer dominates the total device resistance has been accessed. A newly implemented device-preparation and deposition method enables robust contacting of arbitrarily shaped and sized NTs and NRs.

A possible next step would be a systematic assessment of the contact resistance through the transfer length method. By patterning contact pads with consecutively increased spacings along a single device, the contact resistance can be quantified by extracting the resistance of section with zero length via linear regression. A comparison of such measurements across different NTs and NRs could provide further insight into their respective electronic properties.

Following the implementation of four-terminal measurements on the final devices, a direct determination of the intrinsic device resistance becomes possible. With this

post-fabrication treatments could be compared without contributions from variations in contact properties through annealing or aging effects.

The results further show that bismuth contacts remain sufficiently transparent for CB measurements at millikelvin temperatures. Well-defined Coulomb peaks in the linear-transport regime indicate the absence of charge traps underneath the contacts—an effect previously reported for highly reactive metals such as scandium [Reinhardt et al., 2019]. The reproducibility of these features across multiple devices underscores the non-destructive and transparent character of bismuth as a contact material for MoS_2. In addition, the confinement of QDs with sizes comparable to the active device area in the single-level transport regime was achieved in MoS_2 NTs. However, irregular CB patterns point to disorder-induced multi-QD behavior that is present across devices.

Improvements in fabrication enabled both the suspension of NTs between contacts and their integration into hBN–FLG heterostructures. Although neither strategy eliminated disorder observed in measurements at cryogenic temperatures, both are important steps toward fully controllable QDs in MoS_2 devices. First measurements on heterostructures devices already show a significantly enhanced gate coupling, a prerequisite for more detailed transport studies.

Finally, magneto-transport measurements yielded Landé g-factors ranging from 0.6 to 2.0 for magnetic fields parallel to the NT axis and from 1.8 to 7.0 for perpendicular fields. These values are consistent with reports for the in-plane and out-of-plane g-factors of planar MoS_2 [Krishnan et al., 2023, Kumar et al., 2023] when assuming that a magnetic field applied along the NT axis effectively acts as an in-plane field. However, they contradict the expected spin and orbital momentum alignment along the NT axis [Milivojević et al., 2020] and differ fundamentally from the magnetic-field anisotropy observed in CNTs. This discrepancy indicates that either the QDs form at different positions on the NT shell and should therefore be considered as QDs in a quasi-planar material or that the NTs have an unexpected radially outwards spin orientation. In the former case, the interaction between the magnetic field and the electronic states becomes strongly position dependent: for charge confinement at the top or bottom of the shell, both parallel and perpendicular fields effectively act as in-plane fields, whereas at the sides they correspond to in-plane and out-of-plane fields, respectively. In the latter case, a QD extending over the full circumference would exist, but with spins constrained to point out-of-plane, i.e. perpendicular to the NT axis. The deviation from theoretical expectations could originate from the

larger NT diameters compared to those considered in theoretical models. For such diameters, the SOC responsible for out-of-plane spin polarization may still dominate. However, due to device disorder, it was not possible to unambiguously identify which of these effects caused the observed magnetic-field response.

These results further emphasize the necessity of reducing disorder. To unambiguously identify the impact of the NT geometry on the electronic properties of MoS_2, the formation of a QD spanning the entire circumference of the shell is required.

As the analysis of SEM in section 8.3 revealed, contamination on the channel region can be found on many of the devices investigated. The type of particles observed could not be established, but either resist residues or small metal particles created during the lift-off are likely candidates. To mitigate this two strategies are possible: Contamination removal prior to the measurement or encapsulation of the NTs during stamping.

In order to remove the contamination a process would be required that specifically targets the adhesive residues. Depending on whether these are primarily organic materials or metallic ones, an adapted process would be required. A very general approach would be the use of a weak argon plasma treatment. If for example a *Kaufmann* ion beam source is used, as described in section 3.1.2, with beam voltages low enough to deal no significant damage to the MoS_2 lattice, loosely attached residues could be removed. The specific energy required to remove a sulfur atom could be estimated through *Monte Carlo* simulations [Ziegler et al., 2010] and choosing a kinetic energy well below still limit should ensure the integrity of MoS_2. Specifically targeting polymer residues of PMMA, ozone treatment has been reported to be effective in the removal, but it can also lead to oxidization of MoS_2 [Huang et al., 2018, Freedy et al., 2019]. Another option would be the use of H_2S, where a reverse process was reported removing incorporated oxide from CVD grown MoS_2 which oxidized under long term storage conditions [Pető et al., 2018, Marinov et al., 2021]. Additionally, H_2S treatment was found to improve the channel characteristic of finished devices [Byeon et al., 2024].

Instead of cleaning the channel region, the prevention of such contamination could also be achieved by encapsulating the NTs already during stamping. Using a thin hBN layer on top of the NT, the devices would be protected from residues of the wet-chemical processing [Mayorov et al., 2011, Petrone et al., 2015, Lee et al., 2015]. However, the major challenge in this approach is the contact definition. A common approach is etching through both materials and the subsequent deposition of side

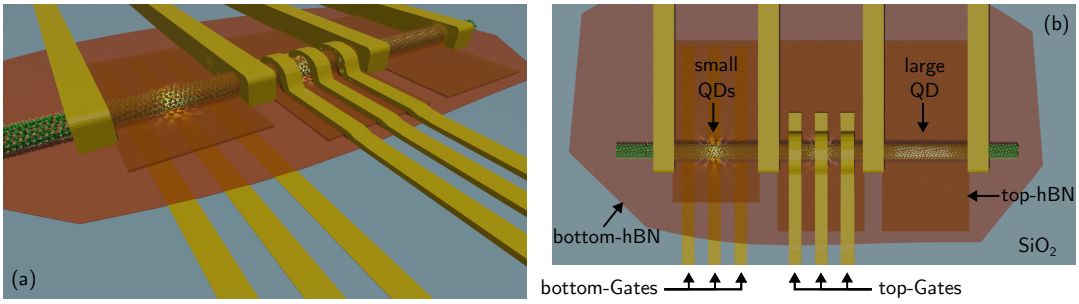


Figure 10.1.: Schematic of a NT device encapsulated in hBN with finger gates both below the bottom and deposited onto the top hBN flakes. (a) Side view and (b) top view.

contacts [Lee et al., 2024]. In contrast to planar MoS_2, an edge contact to a NT is quasi zero-dimensional, which most probably present a further challenge for the creation of transparent contacts. Alternatively, a processes would be needed which can specifically etch the hBN layer while leaving the MoS_2 unchanged. To the author's knowledge, there is currently no processes that could be used to selectively etch the hBN.

An alternative approach would be to employ narrow hBN ribbons or to pre-etch the hBN flakes prior to transfer. Ribbon widths in the range of 1 µm to 2 µm should be feasible for later transfer. Then these ribbons could be either directly transferred onto the heterostructure and the NT, creating protected regions between the contact pads. Alternatively, the NTs could additionally be picked up using such an array of these insulating ribbons and subsequently transferred onto the bottom stack. This procedure would substantially reduce contamination risk from the transfer agents like anthracene, PC, and PDMS (see figure 10.1). However, the resulting confinement would be relatively wide due to the fixed geometry of the ribbons. A finer control could be achieved by adding finger gates, either underneath a bottom insulator or deposited on top of the hBN ribbons, to locally define the potential landscape. In this configuration, the limitations imposed by closely spaced metal contacts would not apply, and an axial confinement length on the order of 50 nm could be realized.

This work established MoS_2 NTs as a viable platform for QD devices, demonstrated robust low-temperature contacts, and provided first spectroscopic insights into their electronic states. While challenges such as disorder remain, the progress achieved here outlines a clear path toward fully controllable QD devices in TMDC NTs.

The results presented here further support the expected spin–valley structure of MoS_2 QDs, thereby underpinning proposals for spin- and valley-based qubits in TMDC nanostructures [Kormányos et al., 2014, Shandilya et al., 2024]. Electrical intervalley driving in gate-defined QDs could enable single-qubit rotations, provided that a controllable intervalley coupling is available [Pawłowski et al., 2018, Pawłowski et al., 2021]. In a gated double QD operated in the (1,1) charge sector and in the regime of large intrinsic spin–orbit splitting, the low-energy dynamics can be reduced to the two lowest Kramers pairs; in this limit the effective interdot interaction is well approximated by Heisenberg-type exchange, enabling standard two-qubit gates such as CNOT via exchange pulsing [Loss and DiVincenzo, 1998, David et al., 2018]. Readout can be implemented via valley Pauli blockade if tunnelling is predominantly valley conserving [Pawłowski et al., 2018, Pawłowski et al., 2021]. Finally, hybrid TMDC–superconductor devices that combine gate-defined QDs with proximity-induced superconductivity (including possible Ising pairing [Lu et al., 2015, Qin et al., 2017]) offer Andreev-bound-state-based parity readout, gate-tunable Josephson control in a gatemon architecture, and potentially valley-selective Andreev processes [Majidi et al., 2014, Yabuki et al., 2016, Lee et al., 2019, Ramezani et al., 2021]. Taken together, these elements outline a concrete route toward scalable spin–valley qubits possibly with superconducting-circuit readout with MoS_2 NTs.

A. Appendix

A.1. Moores Law Revisited by Burg and Ausubel

Figure 1.1 illustrates the evolution of transistor density in integrated circuits, showing the increase in the number of transistors per chip (a) and its decomposition into individual logistic growth trends (b). [Burg and Ausubel, 2021] revisited Moore's Law and, in contrast to the originally predicted 12–24-month doubling period, identified two distinct growth regimes with doubling times of 17 and 33 months. This refinement was achieved by decoupling chip size from transistor count and analyzing the transistor density, i.e., the number of transistors per unit area (figure A.1(a)).

Further analysis of the data's second derivative revealed several inflection points corresponding to alternating phases of acceleration and saturation in miniaturization. These were modeled as six distinct logistic growth periods, shown in figure 1.1(b) and discussed in chapter 1.

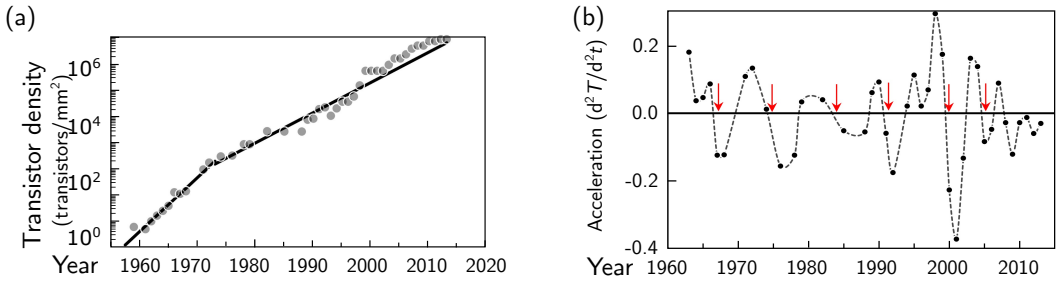


Figure A.1.: Visualization of Moore's law. (a) Number of transistors per unit area over the last five decades. (b) Approximated second derivative (acceleration) of the transistor density. The rad arrows mark inflection points where the growth declines. Figure adapted from [Burg and Ausubel, 2021].

A.2. Dilution Refrigerator

The dilution refrigerator described in section 3.2.3 (optical images in figure A.2) enables continuous operation at base temperatures near 10 mK using a circulating ^{3}He/^{4}He mixture. Measurement lines are thermally anchored and filtered at each stage before reaching the device, which is mounted on a rotator at the mixing chamber for precise magnetic field alignment.

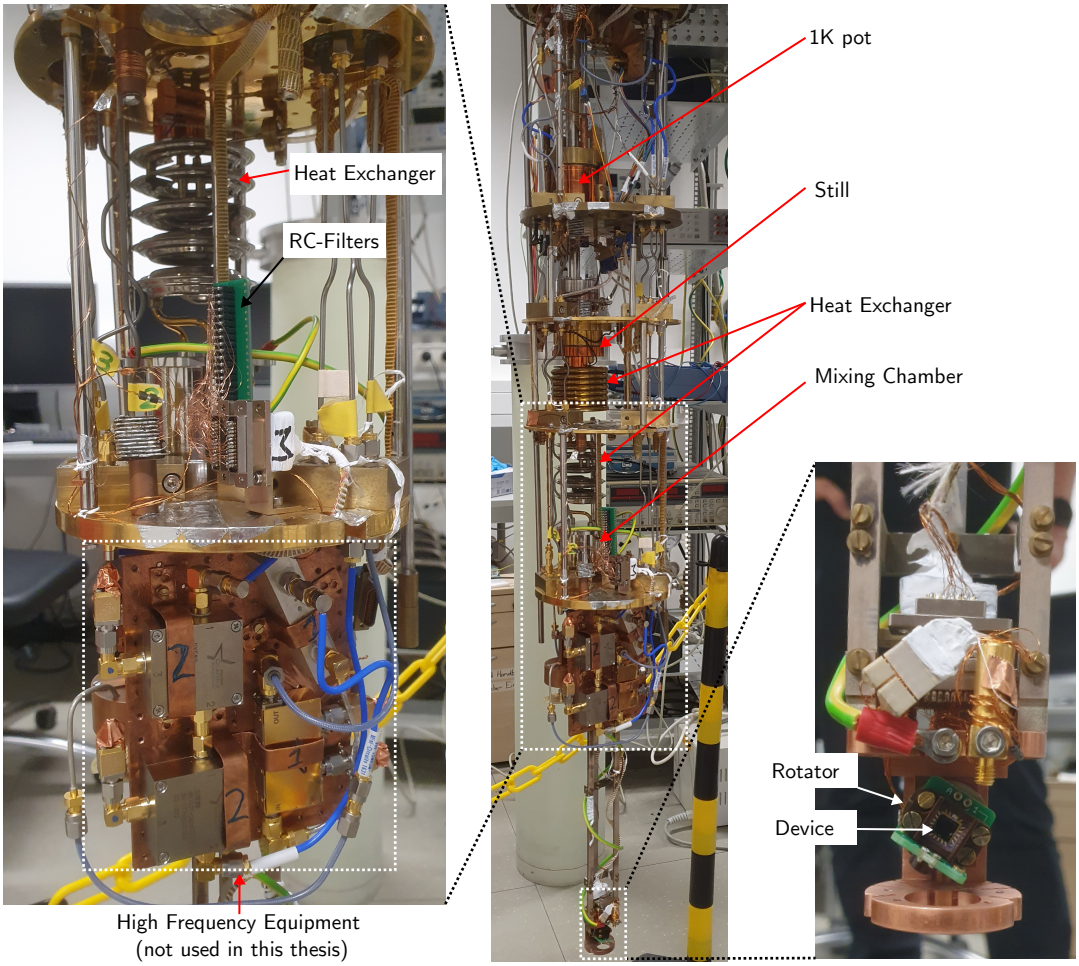


Figure A.2.: Photographic overview of the *Oxford Instruments Kelvinox 400HA* dilution refrigerator used for sub-1.2 K measurements. The central panel shows the main cryostat stages: 1 K pot, still, heat exchangers, and mixing chamber responsible for ^{3}He/^{4}He cooling. The left panel displays the upper section with RC filters and high-frequency components, while the right inset shows the cold finger with the sample rotator and mounted device in the magnet center.

A.3. Series of Multiple QDs under the Contacts

Reinhardt *et. al.* found a series of QDs under the contacts in their MoS_2 NT devices contacted with scandium. In the measurements, a large bias gap was observed for CB, which they attributed to QDs that create a voltage drop between the main QD and the contacts. Due to these being shielded by the contacts the impact of the backgate is minimal and therefore the bias gap remains even for large measurement ranges [Reinhardt et al., 2019]. A schematic of a possible QD configuration is given in figure A.3. There it is shown that in order to pass a current through the whole system a large bias voltage needs to be applied. Then an electron can pass through each QD inside the series. At zero bias and values below the bias gap, current is blocked as there is no available "path" through the system.

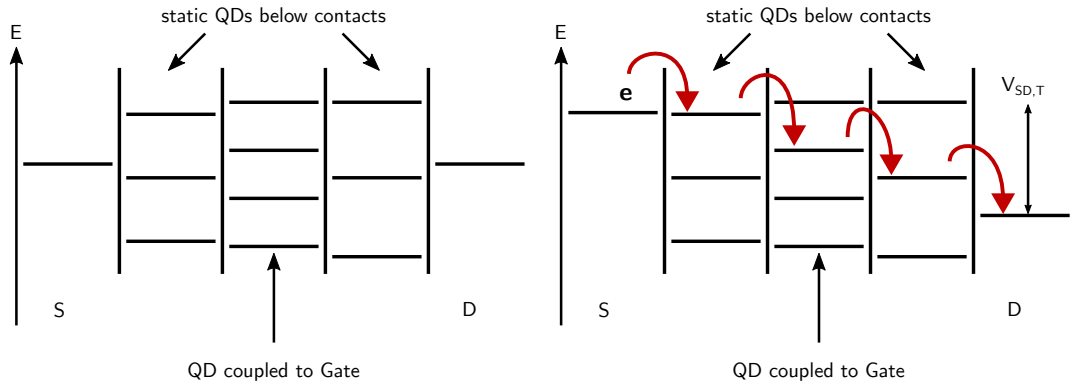


Figure A.3.: Schematics of a multiple QDs system, with the outer QDs under the contact electrodes. (a) The system is in a blocked state independent of an applied gate voltage, as this predominantly shifts the energy levels in the middle QD, while the in-series outer QDs remain off resonance to the leads. (b) A large $V_{SD,T}$ bias voltage is applied to the leads and current can flow through the system.

A.4. Room Temperature Gate Characteristics

Some devices measured throughout this work did not shown a clear gate voltage dependence as depicted in figure 5.4(b) and (c). Instead for about half the devices measured at room temperature, the source-drain current was almost independent of the applied gate voltage. This is shown in figure A.4.

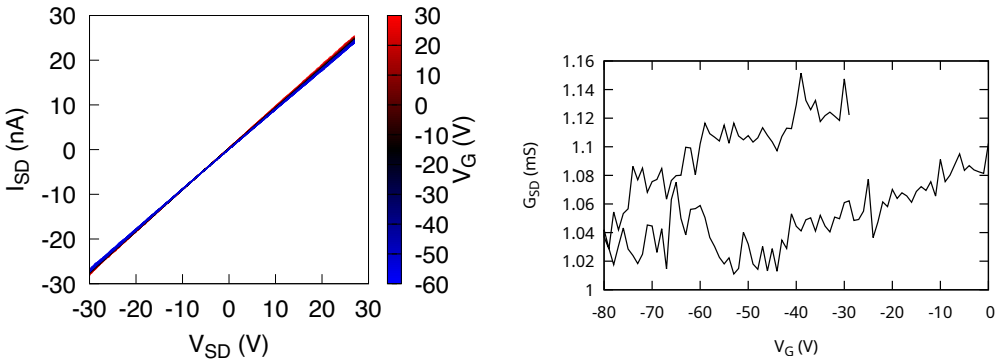


Figure A.4.: Gate characteristics of device 4C measured at room-temperature. (a) Device current as a function of the source-drain voltage for different gate voltages. (b) Differential conductance measured with a lock-in amplifier as a function of the applied gate voltage. Measured at a DC bias voltage of $V_{SD} = 0\,\mathrm{V}$ and an AC bias of $120\,\mu\mathrm{V}$ at a frequency of $416.7\,\mathrm{Hz}$.

A.5. Extended Gate Range Measurements

Large-scale gate sweeps were recorded for several devices to assess the overall electrostatic response and the presence of charge disorder or band gap signatures. These measurements complement the detailed transport data discussed in the main text by providing a broader overview of the accessible gate range and the associated conductance behavior.

Figure A.5 displays data from device 2A, showing that no clear transport gap is observed even at large negative gate voltages, indicating the absence of a well-defined band gap in this device. In contrast, the suspended device 15A (figure A.6) exhibits a pronounced variation in feature size and charging energy with gate voltage, ranging from large V_{SD} gaps at negative V_G to nearly open conduction at positive values.

For device 16A a slight increase with lowering gate voltage was observed (figure A.12). This seems to indicate a band gap edge, but it is not as pronounced as for device 1A (see figure 6.1).

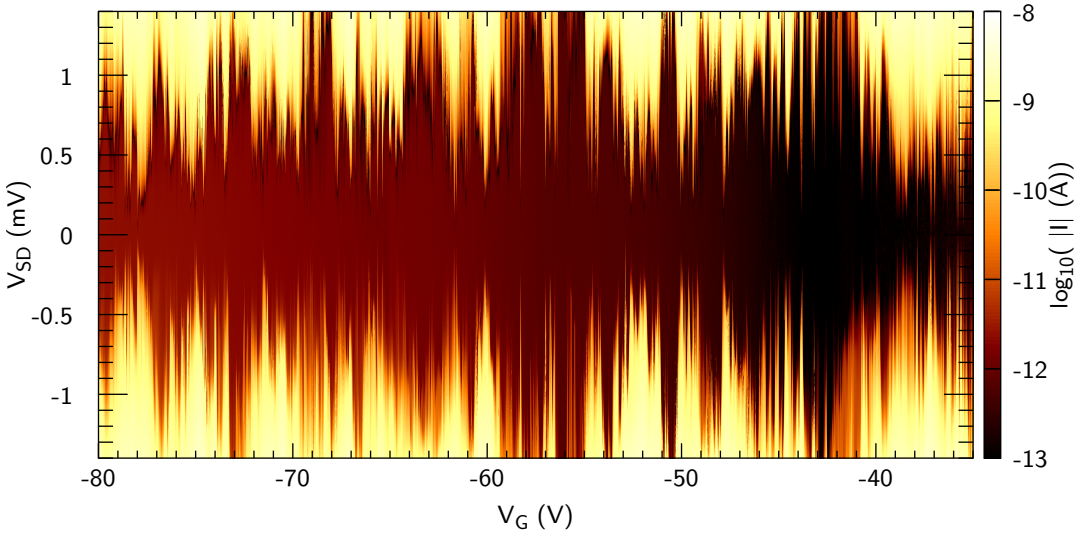


Figure A.5.: Large scale CB measurements performed on device **a** on sample 2A for negative gate voltages. A zoom of a region with positive gate voltages is shown in figure 6.2(a). Over the complete gate range no sign of a band gap is visible and touching CDs are found almost every few V steps.

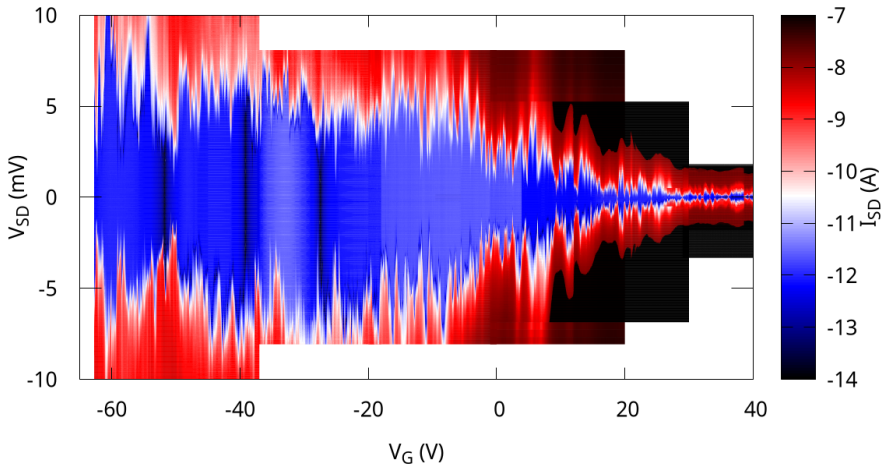


Figure A.6.: Full gate range low temperature measurements of the suspended NT device 15A in section 7.1.1. The color encodes logarithmically the absolute current as a function of V_{SD} and V_G. The feature size vary drastically with the applied gate voltage, at negative V_G a large bias gap and characteristic charging energies in the range of 4 meV to 8 meV are observed opposed to a vanishing V_{SD} gap and E_C below 1 meV.

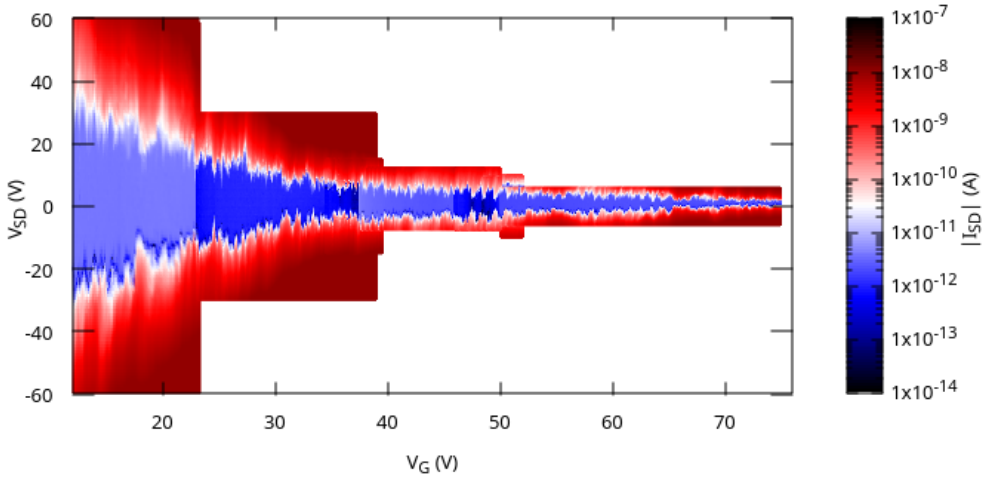


Figure A.7.: Stacked CB measurements performed on 16C device (a) before current annealing (see section 7.2.2) over the large gate range. Plotted is the absolute current as function of gate and bias voltage logarithmically color coded. The bias gap shrinks with increasing gate voltage indicating that the QD is inside the band gap. Especially, below $V_G < 38$ V a almost linear increase of the V_{SD} gap is visible.

A.6. Low Temperature Measurements Enhanced Fabrication Method

In order to test new fabrication method (section 3.1.5), low-temperature measurements at 4 K were preformed on device 13D. The measurements in figure A.8 of the bismuth-contacted NT exhibit Coulomb-blockade pattern around zero bias. This confirms the formation of a confined QD, as well as that the new fabrication methods can still create contacts that confine QDs inside in MoS_2 NT devices.

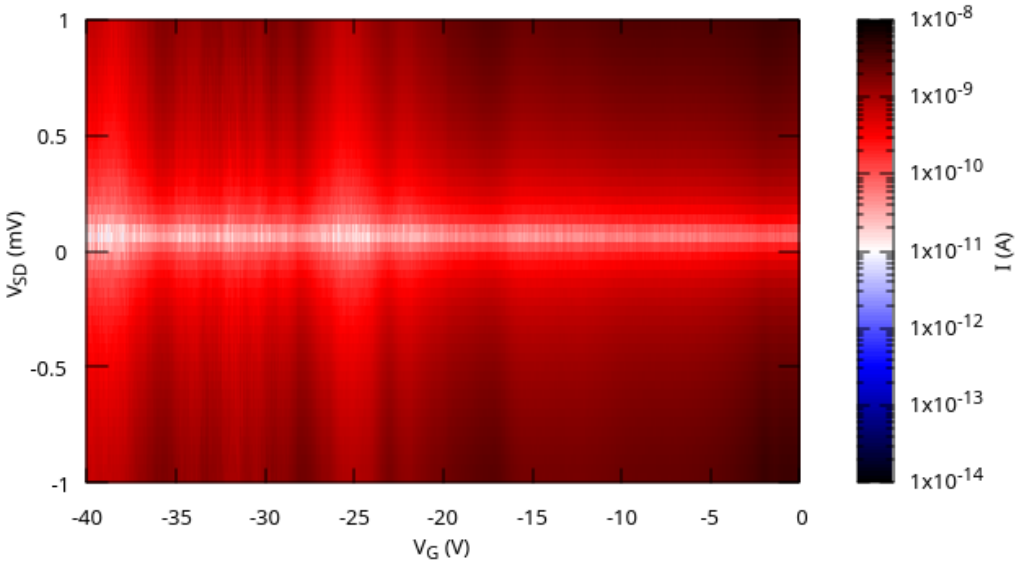


Figure A.8.: Low temperature transport measurements of the NT device 13D contacted with bismuth following the protocol given in section 3.1.5. Plotted is the absolute current as function of gate and bias voltage logarithmically color coded. A clear pattern of CB can be seen around the $V_{SD} = 0$ V line, indication the formation of a QD inside the nanotube. The measurements were performed at 4 K in the 1K-stick (see section 3.2.2).

A.7. Nanogaps between Contacts and Material on Nanotubes

Further examples of discontinuities between the contact metal and the surrounding film are shown in figure A.9. Panel (a) displays a NT that was partially lifted out of the contact region after deposition (11A). In panel (b), the NT has warped out of the metal layer within the channel area, suggesting insufficient adhesion or mechanical stability of the deposited film (12A). Panel (c) shows a device (18A) where a distinct gap is visible between the metal deposited on top of the NT and the adjacent metal on the substrate. These observations illustrate the variability in contact morphology and highlight the tendency of thick evaporated metal films to develop discontinuities at elevated step heights, consistent with the shadowing effects discussed in section 5.4.

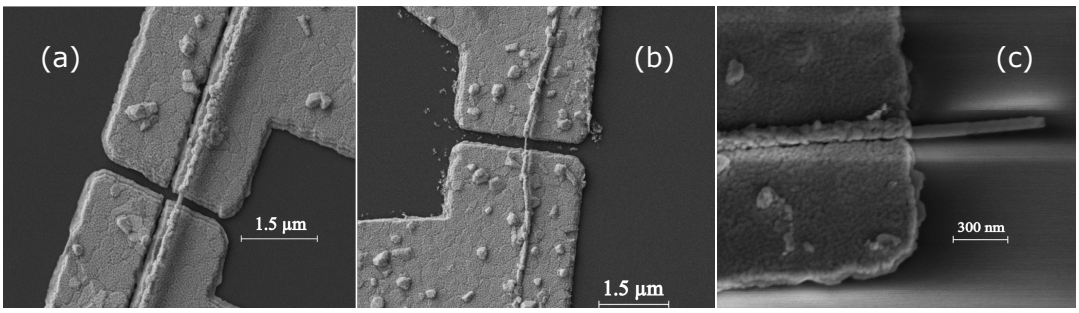


Figure A.9.: More SEM micrographs supplementing figure 5.7. (a) NT lifted out of the contact material (11A). (b) NT warped out of the contact in the channel area indicating poor mechanical stability of the metal layer (12A). (c) NT on 18A with a visible gap between metal on top of the NT and the surrounding metal layer.

A.8. Temperature Dependence of Shallow Suspended NT

Accompanying the temperature measurements shown in figure 7.3 the odd numbered CB peaks are displayed in figure A.10.

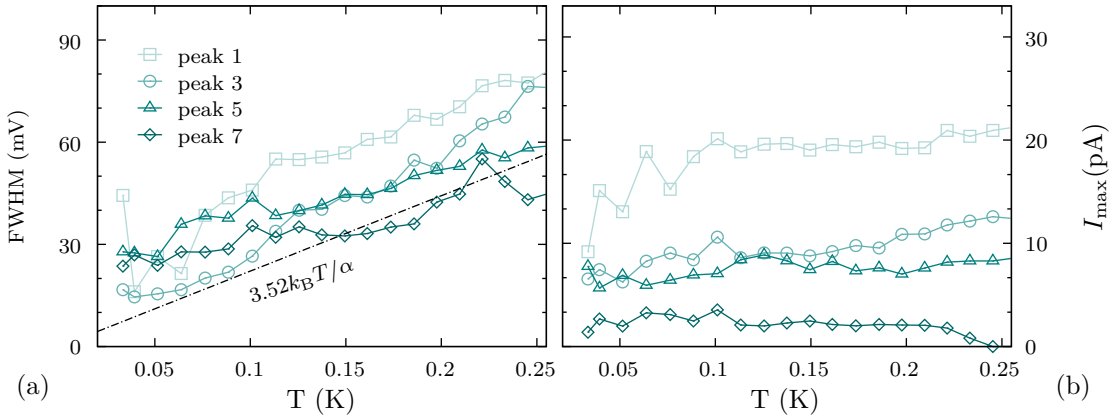


Figure A.10.: FWHM (a) and maximum current (b) of odd numbered peaks from figure 7.3. While the FWHM mostly follows the thermal broadening of the leads, the maximum current is almost independent of the temperature. Only small variations are observed that are most likely caused by an insufficient measurement resolution.

A.9. Transport Measurements after Current Annealing

In section 7.2.2 two devices were insitu current annealed. Device 16A, NT with a diameter of (100 ± 11) nm and a channel length of (200 ± 40) nm (see figure A.11), did chance from the behavior found prior to the annealing. Despite the changes outlined in figure 7.8, also more features indicating transport through excited states was found in figure A.12. However these were found in a region of a large bias gap, indicating a high level of disorder.

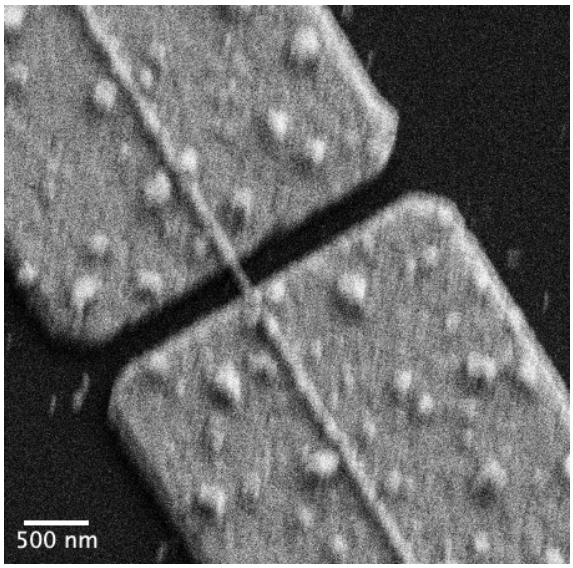


Figure A.11: SEM image of device 16C after the measurement was performed. The device is a NT with a diameter of about (100 ± 11) nm and a channel length of about (200 ± 40) nm.

The device 16D exhibited a decrease in bias gap after annealing (see figure 7.6). In the stability diagram (figure A.13) a region with vanishing V_{SD}gap is found in addition to lines that could indicate transport through excited states. However, a high level of disorder is also observed indicating that still multiple QDs contribute to the transport.

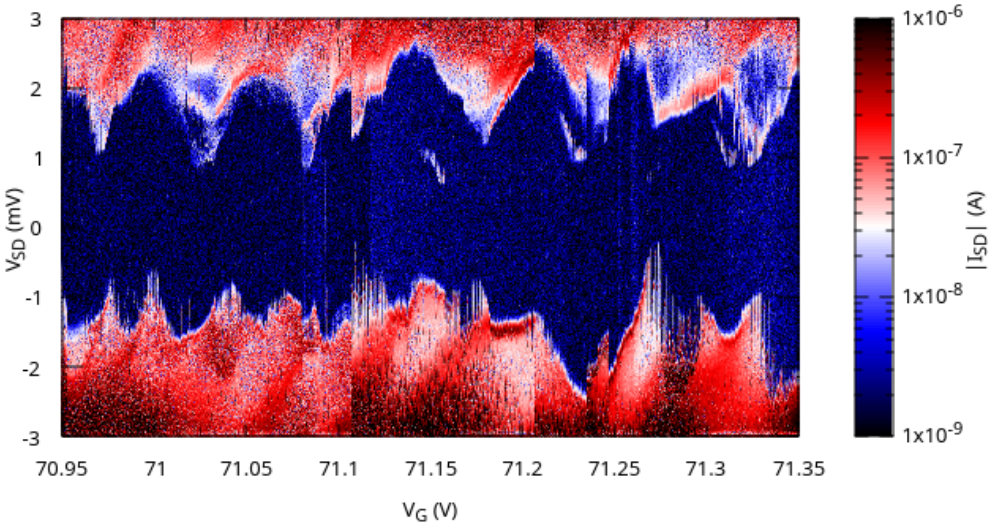


Figure A.12.: Stability diagram of device 16C after current annealing (figure 7.7). Plotted is the absolute numerically derivative of the current after the bias voltage as a function of gate and bias voltage logarithmically color coded. Signs of single level transport and conductance through excited states are visible. The transport is dominated by disorder causing a large $\approx 1\,\mathrm{mV}$ bias gap.

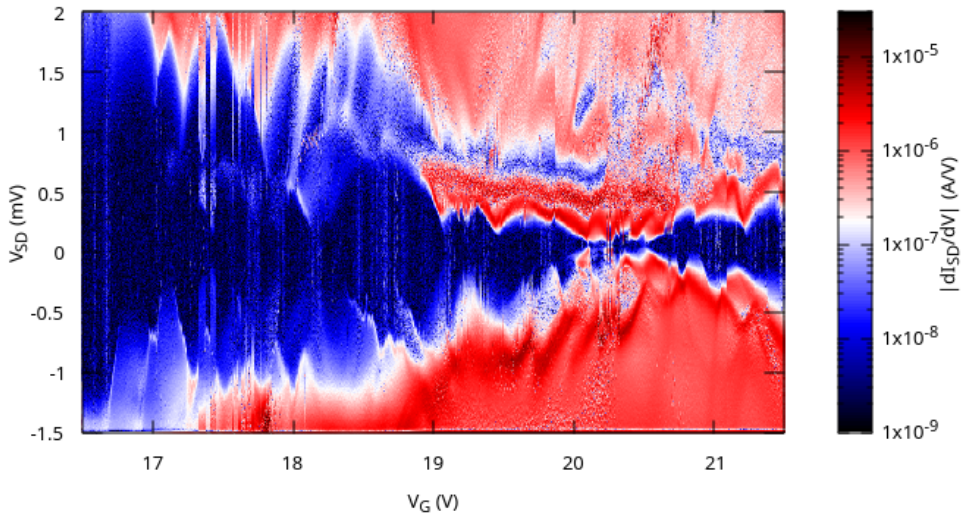


Figure A.13.: CB measurements on device 16C after current annealing (figure 7.7). The plot shows the absolute of the numerically derived conductance as a function of gate and bias voltage with logarithmic color scaling. Features indicative of single-level transport and conductance through excited states are observed, along with signatures of disorder and a possible charge trap.

A.10. Impurities in or at Nanotubes and Contacts

The SEM images in figure 8.5 illustrate common structural imperfections and surface contaminations encountered in MoS_2 NTs. Further images are shown here in figure A.14. Such irregularities can introduce scattering sites or local potential fluctuations that affect charge transport at low temperatures. The presence of multiple walls or bundled structures, as observed in panel (a), may further complicate the formation of well-defined QDs by altering the electrostatic confinement. Additionally, residues or adsorbates on the nanotube surface, as seen in panel (b), can stem from transfer processes or incomplete removal of polymer films, emphasizing the importance of careful surface preparation before device fabrication. This is further discussed in section 8.3.

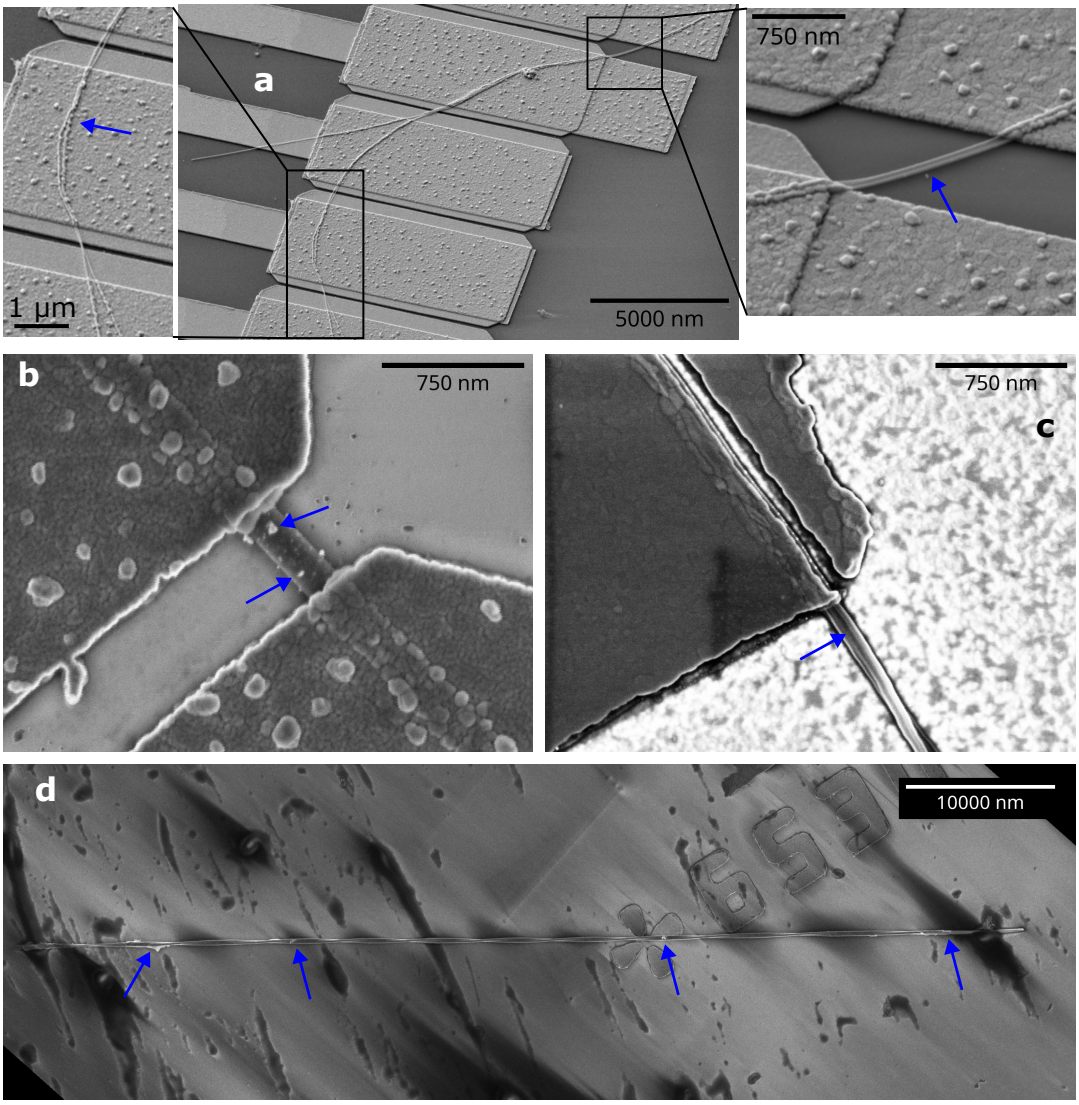


Figure A.14.: SEM micrographs of MoS_2 NTs illustrating various sources of disorder relevant for transport measurements. (a) Large-scale overview of the nanotube bundle shown in figure 8.5. Enlarged regions reveal that the right structure consists of two individual NTs (left zoom), and that the bundle appears to comprise an outer shell wrapped around several inner NTs (right zoom). (b) Surface contamination on a single nanotube, with particle sizes ranging from below 10 nm to approximately 50 nm. (c) A most likely twisted NR device with areas of different contrast. (d) Very long, twisted and thick NR with several defects and contaminations marked with blue arrows.

A.11. Field measurements at Fixed Bias Voltage

In section 9.2.3 measurements were performed at fixed bias voltages. These type of measurements are similar to the ones performed by [Kuemmeth et al., 2008], which are displayed in figure A.15. There they found a magnetic field response that clearly indicated a spin-orbit splitting of the Kramers doublets.

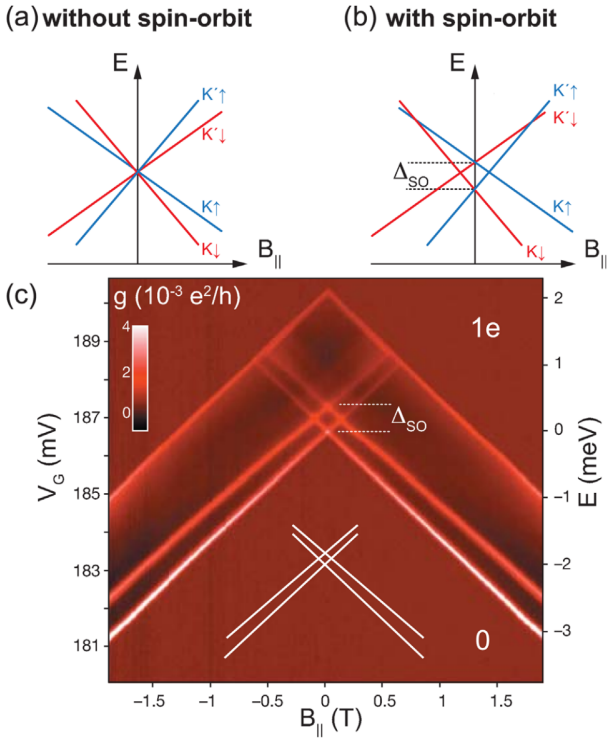


Figure A.15: Measurements of spin-orbit coupling in CNT. The energy spectra **a** with and **b** without spin-orbit coupling. **c** stability diagram as a function of magnetic field at a fixed bias of $V_{SD} = 2\,\mathrm{mV}$ at the transition from zero to one electron. From reference [Kuemmeth et al., 2008].

In addition to the measurements shown in figure 9.5, several other V_G cuts are shown in figure A.16 and figure A.17 both in perpendicular and parallel magnetic fields. This shows that the marked lines in the main text remain the same for different fixed bias voltages and are therefore not just an artifact of the disordered measurements.

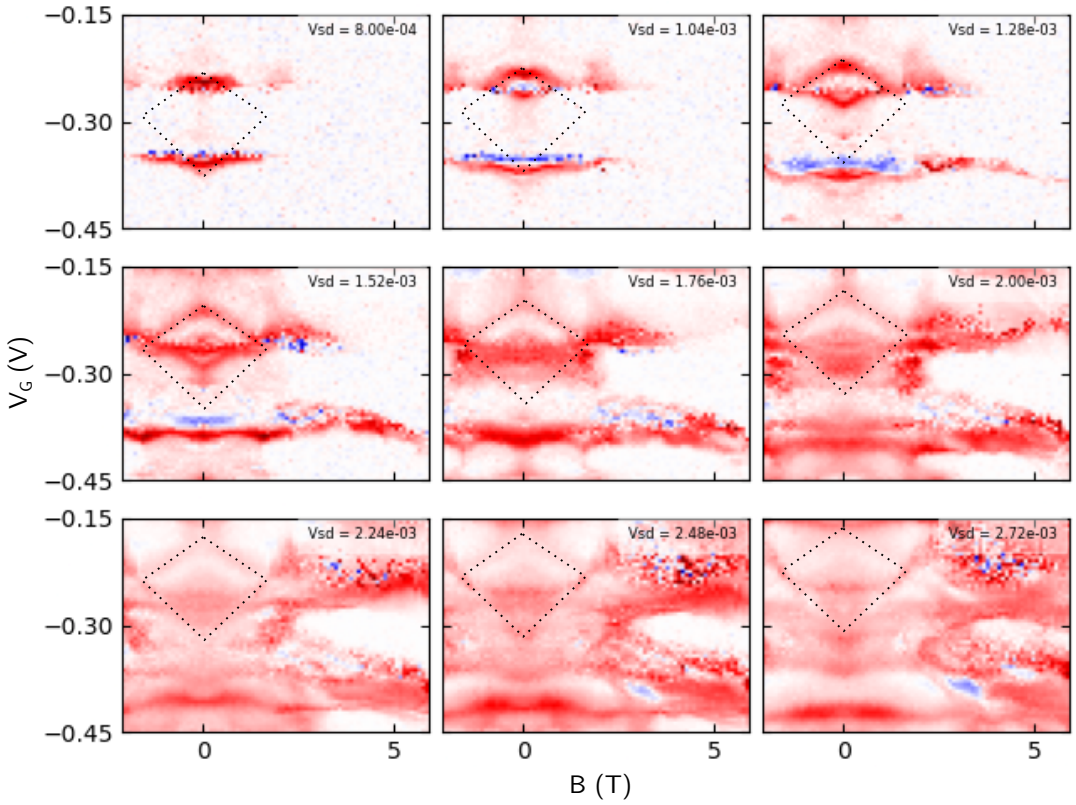


Figure A.16.: Magneto-transport measurements of the NT device 3A at different fixed bias voltages $V_{SD}$for perpendicular magnetic fields. Black dotted outlines mark the lines discussed in section 9.2.3. For each different bias voltage, these shift in gate voltage but their relative positions to each other and slope remain constant.

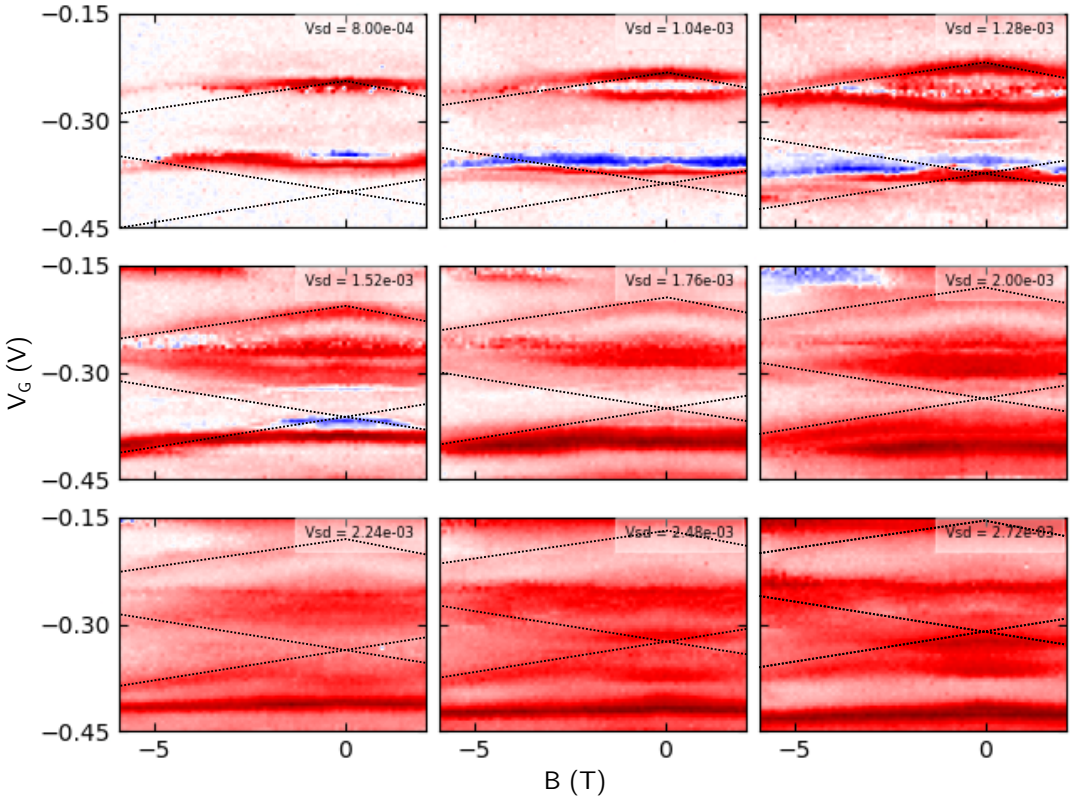


Figure A.17.: Magneto-transport measurements of the NT device 3A at different fixed bias voltages V_{SD} for parallel magnetic fields. Compared to figure A.16 these features are much less distinct, however the black dotted outlines could still match a similar structure here. For each different bias voltage, these shift in gate voltage but their relative positions to each other and slope remain constant. The lines are drawn based on the features observed at $V_{SD} = 2.42\,\text{mV}$ and moved according to the features at zero field around $V_G \approx -0.2\,\text{V}$. The lower lines ($\alpha$, β) are shifted accordingly but sporadically align with the features emerging, e.g. in the range of 1.3 mV to 1.5 mV.

A.12. List of Chips

This section summarizes all processed chips that were characterized during the course of this work. Each chip may contain several devices fabricated under comparable conditions, enabling systematic variation of parameters such as contact metal, substrate, or transfer technique. The table below serves as a reference for the experimental data presented throughout the thesis and provides an overview of the different fabrication routes explored.

Table A.1.: Comprehensive list of all samples measured and analyzed in this thesis. The "Type" column specifies the fabrication approach using the following abbreviations: **ST** – Scotch-tape exfoliation, **SP** – suspended devices, **PC** – heterostructures transferred with PC, **AN** – heterostructures transferred with anthracene, and **CL** – NTs contacted using crosslinks. The "contact" column gives the used materials and thicknesses. The angle column gives the sample holder inclination and T_{evap} temperature during deposition. R is the used deposition rate for the actual contact material.

Chip	**Type**	**Contact** (nm)	**angle** (°)	T_{evap} (°C)	R(Å s^{-1})
1	ST	Bi(30)/Au(100)	0	20	0.5
2	ST	Bi(38)/Au(100)	0	20	0.5
3	CL	Bi(50)/Au(100)	±15	100	0.5
4	ST	Bi(38)/Au(100)	0	20	0.5
5	ST	Ti(30)/Au(50)	0	20	-
6	ST	Bi(25)/Au(100)	0	20	0.5
7	PDMS/AN/CL	Bi(50)/Au(100)	±15	100	0.5
8	SP(200 nm)	Bi(40)/Au(50)	0	20	0.5
9	SP(200 nm)	Bi(50)/Au(100)	0	20	0.5
10	AN	Bi(25)/Au(30)	±10	20	0.5
11	SP(200 nm)	Bi(40)/Au(80)	0	20	0.5
12	SP(200 nm)	Bi(40)/Au(80)	0	20	0.5
13	CL	Bi(50)/Au(100)	±15	100	0.5
14	ST	Bi(45)/Au(100)	0	20	0.5
15	SP(50 nm)	Bi(40)/Au(80)	0	20	0.5
16	SP(200 nm)	Bi(50)/Au(100)	±10	20	0.5

A.13. List of Devices

Table A.2 gives the known parameters of every device measured within this thesis. It is worth mentioning that even though device 7C was on the chip 7 which was used for FLG and hBN devices, this particular devices was off the main FLG flake. Therefore the doped Si back gate was used instead, which explains the large value for the band gap found for this device.

Table A.2.: List of all measured devices, with their respective parameters and properties. Listed are the device geometry (channel length L, width w and height h), device type (T for NT and R for NR), the two terminal room temperature resistance R_{RT}, if a band gap was found in low temperature measurements (**gap**), the charging energy E_C, the measured C_{G} and the simulated gate capacitance with the plate capacitor $C_{\mathrm{G}}^{\mathrm{p}}$ and wire-over-ground model $C_{\mathrm{G}}^{\mathrm{w}}$, respectively.

D.	L (nm)	w (nm)	h (nm)	T/R	R_{RT} (MΩ)	gap (V)	E_{C} (meV)	C_{G} (aF)	$C_{\mathrm{G}}^{\mathrm{p}}$ (aF)	$C_{\mathrm{G}}^{\mathrm{w}}$ (aF)
1A	270(10)	500(10)	18(1)	R	0.10(1)	-21.5	0.25(6)	2.0(2)	9.3(5)	24(2)
2A	150(10)	90(10)	115(2)	T	0.043(4)	n	1.1	0.72	9.3(5)	9(3)
3A	250(20)	30(10)	30(10)	T	0.36(4)	n	1.5(5)	0.72	9.3(5)	9(3)
4A	1500(50)	80(20)	74(5)	T	0.84(8)					
4B	360(50)	140(20)	14(4)	T	2.0(2)					
4C	-	-	-	-	1.0(2)					
5A	-	-	-	-	0.36(4)					
6B	220(30)	360(40)	20(10)	R	0.18(2)	-4	1.2(5)		7.0(5)	6(3)
7A	160(20)	40(10)	32(4)	T	0.45(4)	1.5(3)	1.0(4)	20(5)	1.5(6)	1.4(6)
7D	110(20)	40(10)	32(4)	T	0.59(6)	1.2				
7E	90(20)	39(7)	12(2)	T	11(1)	75				
7F	190(30)	210(10)	15(2)	R	0.71(7)	-				
8A	170(40)	130(30)	120(40)	T						
9A	150(40)	350(20)	20(20)	R						
10A	200(40)	150(30)	140(40)	T	100(10)					
11A	200(40)	100(30)	90(40)	T						
12A	160(40)	130(30)	120(40)	T						
13A	200(30)	50(30)	50(30)	T	0.14(1)					
13B	200(30)	100(40)	100(40)	T	0.29(1)					
13C	200(30)	100(40)	100(40)	T	14(1)					
14A	200(20)	160(30)	20(10)	R	0.25(3)	-4	0.85(8)	0.80(2)	11(2)	2.1(2)
15A	140(10)	38(7)	38(7)	T	0.18(2)	n	0.07(4)	2.0(5)	11(2)	2.1(2)
16A	220(40)	100(10)	-	T	0.60(3)	18(1)	1.0(2)	2.6(3)		
16B	230(30)	160(20)	60(40)	T	0.59(3)	-	-	-		

List of Acronyms

Au gold.

Bi bismuth.

Ti titanium.

2D two-dimensional.

AC alternating current.

ADF annular dark-field.

AFM atomic force microscopy.

CB Coulomb blockade.

CBM conduction band minimum.

CD Coulomb diamond.

CFET Complementary Field-Effect Transistor.

CMOS Complementary Metal–Oxide–Semiconductor.

CNL charge neutrality level.

CNT carbon nanotube.

CVD chemical vapor deposition.

CVT chemical vapour transport.

DC direct current.

DFT density functional theory.

DOS density of states.

EBL electron beam lithography.

EDLT electric double-layer transistor.

eGun electron gun.

FET field effect transistor.

FLG few-layer graphene.

FLP Fermi level pinning.

FWHM full width half maximum.

GS gap states.

hBN hexagonal boron nitride.

LOR lift-off resist.

MBE molecular-beam epitaxy.

MIBK methyl isobutyl ketone.

MIGS Metal induced gap states.

MOS metal-oxide-semiconductor.

MW molecular weight.

NR nanoribbon.

NT nanotube.

PC Poly-Carbonate.

PDMS Polydimethylsiloxane.

PMMA Poly(methyl methacrylate).

QD Quantum Dot.

SB Schottky barrier.

SC Semiconductor.

SEM scanning electron microscopy.

SET single electron transistor.

SOC spin-orbit coupling.

STEM scanning transmission electron microscopy.

SWNT single wall nanotube.

TEM transmission electron microscopy.

TMDC Transition Metal Dichalcogenide.

UHV ultra high vacuum.

VBM valence band maximum.

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List of Publications

Publications in relation to this work:

- **R. T. K. Schock**, M. Malok, M. Remškar, and A. K. Hüttel, *Signatures of Spin-orbital coupling in multiwall MoS_2 nanotubes*, in preparation.
- **R. T. K. Schock**, K. Fink, S. Obloh, J. Neuwald, M. Kronseder, W. Möckel, M. Malok, L. Pirker, M. Remškar, and A. K. Hüttel, *Reproducible bismuth contacts to MoS_2 nanotubes and nanoribbons*, in preparation.
- **R. T. K. Schock**, S. Obloh, J. Neuwald, M. Kronseder, W. Möckel, M. Malok, L. Pirker, M. Remškar, and A. K. Hüttel, *Material transfer and contact optimization in MoS_2 nanotube devices*, Physica Status Solidi (b) **2400366** (2024). DOI: 10.1002/pssb.202400366
- **R. T. K. Schock**, J. Neuwald, W. Möckel, M. Kronseder, L. Pirker, M. Remškar, and A. K. Hüttel, *Non-Destructive Low-Temperature Contacts to MoS_2 Nanoribbon and Nanotube Quantum Dots*, Advanced Materials 35, **2209333** (2023). DOI: 10.1002/adma.202209333

Publications in relation to prior projects:

- M. Hafermann, **R. Schock**, C. Wan, J. Rensberg, M. A. Kats, and C. Ronning, *Fast recovery of ion-irradiation-induced defects in $Ge_2Sb_2Te_5$ thin films at room temperature*, Opt. Mater. Express, OME 11, **3535** (2021). DOI: 10.1364/OME.439146
- Gia Q. Ngo, Antony George, **Robin T. K. Schock**, Falk Eilenberger, et. al., *Scalable functionalization of optical fibers using atomically thin semiconductors.*, *Advanced Materials*, **2003826** (2020). DOI: 10.1002/adma.202003826

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